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RESEARCH ARTICLE - ELECTRICAL ENGINEERING

Design and Modeling of Single-Phase PV-UPQC Scheme for Power Quality Improvement Utilizing a Novel Notch Filter-Based Control Algorithm: An Experimental Approach

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Abstract
This paper deals with grid integration of photovoltaic systems through single-phase unified power quality conditioner (PV-1UPQC) based on notch filter novel control algorithm for its function such as better phase detection, voltage sag/swell, voltage unbalance, voltage and current harmonics eliminations. A notch filter-based control algorithm includes a phase-locked loop (PLL) mechanism which is responsible to avoid multiple zero crossing at the time of highly distorted grid voltage detection. Notch filter PLL-based control algorithm is applied to both series and shunt inverters of PV-tied UPQC. In addition to normalizing voltage and current perturbations, proposed controller has feature of phase detection and perfect grid synchronization. Synchronous reference d-q frame controller and unit vector control algorithm with conventional PLL is also studied, utilized and evaluated for control of PV-1UPQC. Hardware setup is developed in laboratory using DS1103 dSPACE processor. Performance and efficiency of PV-1UPQC are analyzed through simulation and experimentation for various operating conditions.

Keywords PV-tied UPQC · Notch filter PLL · Power quality · Current harmonics · Voltage sags · Voltage swells

1 Introduction

Advanced power electronics-based equipment used at the consumer end results in power system disturbances and gives rise to voltage and current quality issues [1–3]. Furthermore, fast vanishing conventional energy sources force the globe toward the use of renewable energy sources such as wind power generation and solar power. The implementation of small- as well as large-scale solar and wind energy-based system at distribution level has been increased adequately. The grid integration of renewable energy system requires power electronic converters to provide necessary power to grid [4–6]. Therefore, grid-integrated systems are contaminated with current and voltage quality issues. The issues such as current harmonics, voltage harmonics, voltage sags, voltage swells and voltage unbalance are required to be tackled to improve the power quality at distribution level. Sophisticated processors at the automated factories such as microcontrollers and microprocessor-based controllers respond to the voltage quality maintained and delivered to them. Abnormal operation of this sensitive equipment may be noticed or even get damaged due to the presence of poor voltage quality.

On the other hand, power electronics-based devices are employed to deal with the power quality issues. These power electronics-based devices are controlled in a proper manner to eliminate the power quality issues. Active power filters with its various categories like shunt active power filters, series active power filters, hybrid active power filters [7,8] are considered as effective power conditioners. However, these types of power conditioners are used separately to eliminate voltage and current quality problems. The unified power quality conditioners (UPQC) are the combination of series and shunt active power filters connected back to back with a DC-link capacitance in between. The hybrid nature of UPQC is capable to mitigate various voltages and current quality issues simultaneously [2,9,10]. Although various system studies are based primarily on three-phase system and UPQC installed as power conditioners, still single-phase systems need concentration. Power quality issues such as current harmonics, voltage sags, voltage swells and volt-

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age unbalance are more significant for single-phase system [11]. At the same time, various active filtering solutions have been studied for PV grid-connected systems, which are primarily meant for current quality issues [6]. Various topologies are reported from the literature for PV grid integration. However, photovoltaic systems connected to grid through single-phase UPQC have not been reported so far. Therefore, this paper is primarily based on power quality compensation in PV-1UPQC system. Implementation of the UPQC in the distribution system depending on the placements of shunt inverter has classified the UPQC type. In UPQC-L (left shunt UPQC), shunt inverter is placed at the source side and UPQC-R (right shunt UPQC), the shunt inverter is found to be connected at load side [12]. Based on the voltage injection, angle UPQC is also classified, namely UPQC-Q, UPQC-S, UPQC-P. UPQC-Q is responsible for injection of quadrature component of voltage to the grid. In UPQC-P, the series inverter injects voltage in phase with grid voltage [13].

In UPQC-S, both active and reactive power injection to the grid become possible. In comparison with all those UPQC topologies, PV-UPQC has the unique advantage. It has the ability to maintain power quality with voltage and current issues, fault ride through operation [14,15].

The grid-connected PV systems with active conditioners are implemented with various controllers as presented in [5,6]. Those controllers are limited to mitigation of current quality issues. To eliminate both voltage quality and current quality issues, PV system is interfaced with grid through single-phase UPQC. The performance of UPQC in the present system specifically depends on control algorithm and its efficiency. Some of the very popular controllers are instantaneous reactive power theory and synchronous detection algorithm [16]. Unit vector template generation scheme also used for the control of both shunt and series inverter of UPQC. Although it has been used for conventional power system, there is very few papers reported which has implemented these controllers for PV-tied grid systems or PV-tied UPQC system. Synchronous reference frame controller is popular for conventional three-phase system. Its use in single-phase system to control the inverters of PV-tied UPQC is not reported.

In grid-connected PV system and its synchronization with the grid play much important role for detection of phase and frequency. Therefore various phase detection mechanism are installed, represented as phase-locked loops. Enhanced PLL Synchronous reference frames are already in used for conventional systems. It becomes very difficult to detect phase when the grid voltage is highly distorted. It is noticed that the presence of highly distorted elements in the grid, are the major cause of multiple zero crossing. Considering this situation, advancement in PLL technique has increased gradually. The utilization of enhanced PLL and the SRF PLL are reported in literature [17–19]. However the limitations of these PLLs such as multiple zero crossing have been overcome by the proposed method. The notch filter-based PLL scheme is implemented for grid synchronization functionality. For grid phase detection low-pass filter along with low-pass notch filter is employed in [19,20]. In this paper PLL based on time delay is taken into account. The PLL performance as well as efficiency is used by the implementation of notch filter.

By considering all those limitations of control strategies and PLLs schemes, this paper proposes a new control methodology for the single-phase PV-tied UPQC. Notch filter PLL-based controllers are presented for both series and shunt inverters of the system discussed. Proposed single-phase PV-tied UPQC system is presented in Sect. 2. The parameters required for designing the single-phase system is included in Sect. 3. Section 4 presents the conventional control methodologies for PV-tied UPQC. Issues with conventional PLLs and its effect on controllers, notch filter-based controller, design and parameter selection of notch filter PLL is described in detail in Sect. 5. Simulations results and experimental setup and results are presented in Sects. 6 and 7, respectively. Finally Sect. 8 concludes the paper.

2 System Configuration and Parameter Design

2.1 PV-1UPQC System Configuration

The structure of the PV-1UPQC is classified into two categories such as left shunt PV-1UPQC and right shunt PV-1UPQC. In this paper the right shunt PV-1UPQC has been considered for study. This topology allows the position of shunt inverter at the load end, where as the series inverter to be positioned at source side. The shunt APF is employed to work in current control mode and deals with current compensation. It regulates the voltage of DC-link capacitor and provides active power to grid from PV array. The series APF is employed to maintain the voltage quality such as voltage sags/swells. PV array is in grid-connected mode through the DC-link capacitor of single-phase UPQC through a DC–DC converter. The DC–DC converter is regulated by the maximum power point (MPP) algorithm to extract maximum power. The shunt and series APF are interfaced with the power system using interfacing inductors as shown in Fig. 1. To eliminate the presence of higher-order harmonics, a ripple capacitor is used at the ac output of series APF.

2.2 Parameter Design of PV-1UPQC

The design of single-phase PV-UPQC consists of detail design of series inverter, shunt inverter and the PV Array. The parameter design of PV-1UPQC involves the evaluation of DC-bus capacitor voltage, the size of the DC-bus capaci-

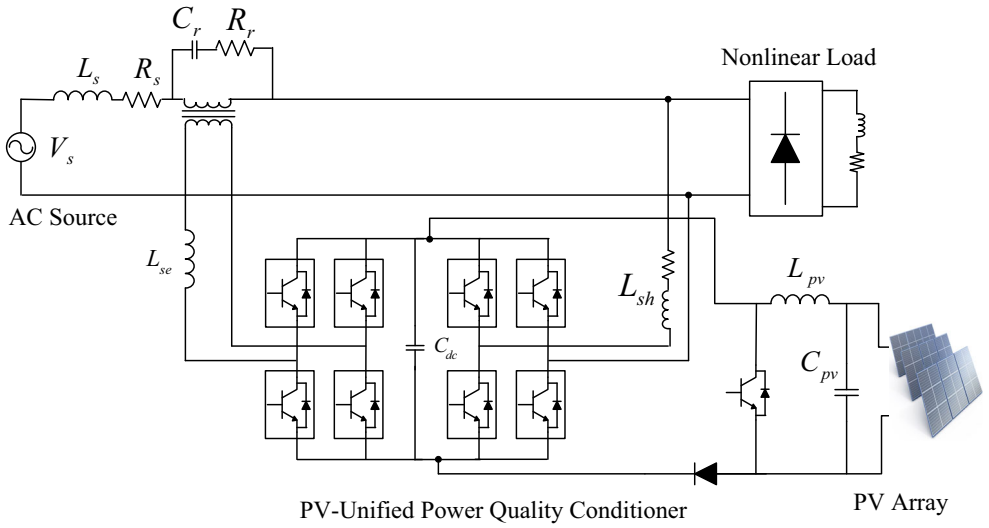


Fig. 1 Single-phase PV-tied UPQC

tor, series inverter turns ratio, interfacing inductor value and the PV array. The detail design procedure is explained and evaluated as follows.

2.2.1 DC Bus Voltage Calculation

For any of the pulse width modulation (PWM)-based voltage source converter (VSC), DC-bus voltage magnitude should be approximately equal to peak value of the grid voltage as presented in [21].

Therefore, magnitude of DC-bus voltage can be evaluated from the peak value of grid voltage and it is required to set the minimum magnitude of DC-bus voltage. The equation for DC-bus voltage calculation can be given as,

$$V_{\mathrm{dc}} = \frac{\sqrt{2}V_s}{m} = \frac{\sqrt{2} \times 230}{1} = 325.2691 \approx 325\,\mathrm{V} \tag{1}$$

where V_s is rms grid voltage, m refers to the modulation index selected as 1. For the system considered with grid voltage of 230 V the magnitude of minimum DC-bus voltage is 325 V. As the source current is highly distorted by the nonlinear loads, a greater value of DC-bus voltage is desired. To regulate the load voltage level and eliminate the voltage spikes/high-voltage condition, DC-bus voltage is selected as 450 V.

2.2.2 DC Bus Capacitor Rating

The sizing of DC-bus capacitor is desired for DC-bus regulation and normal operation of 1PV-UPQC. Evaluation of DC-bus capacitor value depends on instantaneous power flow in the DC-bus capacitor, ripple in DC-bus voltage as given in [21,22]. Therefore, DC-bus capacitor sizing can be evaluated from the given equation:

$$P_{\mathrm{pv-1UPQC}} = C_{\mathrm{dc}}.2\omega.V_{\mathrm{dc}}.\Delta V_{\mathrm{dc}} \tag{2}$$

$$C_{\mathrm{dc}} = \frac{P_{\mathrm{pv-1UPQC}}}{2\omega.V_{\mathrm{dc}}.\Delta V_{\mathrm{dc}}} = \frac{11500}{2 * 314.1 * 450 * 8.5} = 4.7\,\mathrm{mF} \tag{3}$$

where $P_{\mathrm{pv-1UPQC}}$ is the net power dissipated by the system, ω represents the angular frequency, V_{dc} is the DC-bus voltage, ΔV_{dc} is the voltage ripple in DC-bus voltage. The DC-bus voltage is 450 V considered for this system. The ripple voltage can be maximum 2% as considered for the system. The obtained value for the DC-bus capacitor voltage is selected as 4.7 mF.

2.2.3 Series Inverter Rating

The series transformer is utilized for connecting the series inverter of VSC to the grid in series mode. The rating of the transformer can be evaluated by the amount of voltage to be injected as well as the DC voltage. As the series VSC is designed for compensation of maximum ±30% voltage. Therefore, the voltage to be injected can be evaluated as,

$$V_{\mathrm{SE}} = X.V_{\mathrm{VSE}} = 230 \times 0.3 = 69\,\mathrm{V} \tag{4}$$

The series inverter is designed for the elimination of voltage sags/swells pf 0.3 pu and hence, the required voltage to be injected is 69 V.

To keep the modulation index of series inverter near to unity, the turn ratio of series transformer can be computed as,

$$K_{\mathrm{se}} = \frac{V_{\mathrm{VSE}}}{V_{\mathrm{SE}}} = \frac{230}{69} = 3.23 \approx 3 \tag{5}$$

Now the VA rating of the series transformer can be evaluated by the following expression,

$$S_{\text{serise}} = V_{\text{SE}}.I_{\text{series}} = 1.96\,\text{kVA} \tag{6}$$

2.2.4 Interfacing Inductor of Series Inverter

The series inverter of the PV-1UPQC is interfaced with the grid by the utilization of the interfacing inductor. Therefore, the design and parameter estimation of the interfacing inductor is very much necessary. The rating evaluation of interfacing inductor depends upon ripple current, switching frequency, DC-link capacitor voltage, series transformer turns ratio.

$$L_{\text{se}} = \frac{K_{\text{se}}.V_{\text{dc}}.m}{4af_{\text{se}}I_{\text{rp}}} = \frac{3*450*1}{4*1.2*10000*3.1} = 9.07mH \tag{7}$$

where K_{se} refers to transformer turns ratio, V_{dc} is the DC-bus voltage, m is modulation index, f_{se} is the switching frequency of series inverter, I_{rp} is the ripple current, a is the pu for maximum overloading. The depth of modulation is represented as m. In this case, ripple current is selected as 20% of the grid current. For this evaluation $K_{\text{se}} = 3$, $V_{\text{dc}} = 450\,\text{V}$, $m = 1$, $f_{\text{se}} = 10\,\text{kHz}$. The value of interfacing inductor considered for this research is $L_{\text{se}} = 9.2\,\text{mH}$.

2.2.5 Interfacing Inductor of Shunt Inverter

The interfacing inductor of the shunt inverter depends on the converter switching frequency, ripple current and DC-link voltage. Therefore, it is represented as,

$$L_{\text{sh}} = \frac{V_{\text{dc}}.m}{4af_sI_{\text{rp}}} = \frac{450*1}{4*1.2*10000*3.1} = 3.02\,\text{mH} \tag{8}$$

where V_{dc} is the DC-bus voltage, m is modulation index, f_s is the switching frequency of shunt inverter, I_{rp} is the ripple current, and a is the pu for maximum overloading. The ripple current is considered as 5% of the phase current. The values considered here are $V_{\text{dc}} = 450\,\text{V}$, $f_{\text{se}} = 10\,\text{kHz}$, $m = 1$, $a = 1.2$ and $I_{\text{rp}} = 3.1\,\text{A}$. The value selected for shunt inductor is 3 mH.

2.2.6 PV Array

The open circuit voltage of the PV array is necessary to be similar as the DC-link voltage of PV-1UPQC. Therefore, the employed boost converter with the MPPT controller needs to boost the voltage to require DC-link voltage. This voltage of DC link is represented as open circuit voltage of PV array. Various other parameters of PV array are given in Table 1.

Table 1 PV array specification

Parameter	Values
Maximum power	9.5 kW
Open circuit voltage	450 V
Short circuit current	26.5 A
Voltage at MPP	368.9 V
Current at MPP	25.5 A
Parallel string	3
Series module string	12

3 Control of PV-1UPQC System

To evaluate the performance of PV-1UPQC, two conventional control strategies have been considered in this paper. Synchronous reference d-q frame and unit vector template generation controller are discussed here which are applied to PV-1UPQC.

3.1 Single-Phase Synchronous Reference D-Q Frame

Single-phase d-q frame controller is utilized for shunt APF to eliminate the current harmonics and maintain current quality. Figure 2 presents the block diagram of synchronous reference d-q frame (SRF) controller. The load current is captured, and transformation to $\alpha - \beta$ is represented as $I_{L\alpha}$, $I_{L\beta}$; achieved using the following equation:

$$\begin{bmatrix} i_{L\alpha} \\ i_{L\beta} \end{bmatrix} = \begin{bmatrix} i_L(\omega t + \varphi_L) \\ i_L(\omega t + \varphi_L + \pi/2) \end{bmatrix} \tag{9}$$

The load current is represented in synchronous $d - q$ frame (I_{Ld}, I_{Lq}) is given as,

$$i_{\text{Ld}} = i_{L\alpha}(\sin\omega t) - i_{L\beta}(\cos\omega t) = i_{\text{Lda}} + \hat{i}_{\text{Ld}} \tag{10}$$

$$i_{\text{Lq}} = i_{L\alpha}(\cos\omega t) - i_{L\beta}(\sin\omega t) = i_{\text{Lqa}} + \hat{i}_{\text{Lq}} \tag{11}$$

where I_{Lda}, I_{Lqa} are presented as fundamental active and reactive load current; $\hat{I}_{\text{Ld}}$, $\hat{I}_{\text{Lq}}$ are harmonic active and reactive component of load current.

The shunt inverter is forced to maintain ideal source current by eliminating the current harmonics and reactive power component. So the source current component should look like:

$$\begin{bmatrix} i^*_{\text{Ld}} \\ i^*_{\text{Lq}} \end{bmatrix} = \begin{bmatrix} i_{\text{Lda}} + 0 \\ 0 + 0 \end{bmatrix} \tag{12}$$

where I^*_{Ld}, I^*_{Lq} are reference source currents in $d - q$ frame. The reference source current signal in $\alpha - \beta$ frame ($I^*_{s\alpha}$, $I^*_{s\beta}$)

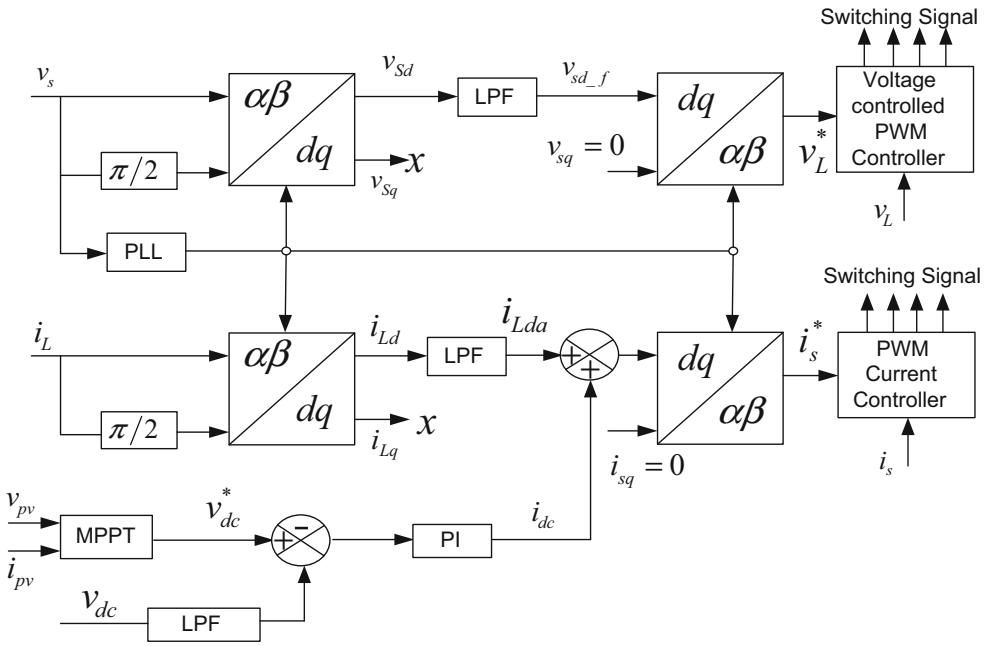


Fig. 2 Synchronous reference d-q frame controller for single-phase PV-tied UPQC

can be given as

$$\begin{bmatrix} i^*_{s\alpha} \\ i^*_{s\beta} \end{bmatrix} = \begin{bmatrix} \sin\omega t & -\cos\omega t \\ \cos\omega t & \sin\omega t \end{bmatrix}^{-1} \begin{bmatrix} i_{\mathrm{Lda}} + i_{\mathrm{dc}} \\ 0 \end{bmatrix} \tag{13}$$

The DC-bus component of the PV-1UPQC is represented as i_{dc}. The imaginary current component of the system $i^*_{s\beta}$ is neglected. Therefore, the reference source current i^*_s can be represented as

$$i^*_s(\omega t) = i^*_{s\alpha}(\omega t) = \sin(\omega t).(i_{\mathrm{Lda}} + i_{\mathrm{dc}}) \tag{14}$$

The reference current generated by the controller is compared with the actually sensed current to provide switching pulse to the shunt inverter.

The way of approach toward adopted for current profile, a similar method has been utilized for voltage profile to generate reference voltage signals for series inverter of PV-1UPQC. The transformation of the source voltage in $\alpha - \beta$ frame ($v_{S\alpha}$, $v_{S\beta}$) can be given as

$$\begin{bmatrix} v_{s\alpha} \\ v_{s\beta} \end{bmatrix} = \begin{bmatrix} v_s(\omega t) \\ v_s(\omega t + \pi/2) \end{bmatrix} \tag{15}$$

The source voltage or the grid voltage can be given in d-q reference frame:

$$v_{sd} = v_{s\alpha}(\sin\omega t) - v_{s\beta}(\cos\omega t) = v_{sdf} + \hat{v}_{sd} \tag{16}$$

$$v_{sq} = v_{s\alpha}(\cos\omega t) - v_{s\beta}(\sin\omega t) = v_{sqf} + \hat{v}_{sq} \tag{17}$$

where v_{Sdf} and v_{Sqf} are source voltage fundamental active and reactive component, $\hat{v}_{Sd}$ and $\hat{v}_{Sq}$ are harmonic active and reactive component. The reference source voltage signal in $d-q$ frame (v^*_{Sd}, v^*_{Sq}) can be represented as

$$\begin{bmatrix} v^*_{sd} \\ v^*_{sq} \end{bmatrix} = \begin{bmatrix} v_{sdf} + 0 \\ 0 + 0 \end{bmatrix} \tag{18}$$

The reference source voltage signal in $\alpha - \beta$ frame ($v^*_{L\alpha}$, $v^*_{L\beta}$) can be given as

$$\begin{bmatrix} v^*_{L\alpha} \\ v^*_{L\beta} \end{bmatrix} = \begin{bmatrix} \sin\omega t & -\cos\omega t \\ \cos\omega t & \sin\omega t \end{bmatrix} \cdot \begin{bmatrix} v_{sdf} \\ 0 \end{bmatrix} \tag{19}$$

The imaginary part of the reference voltage signal $v^*_{L\beta}$ is neglected, and the reference voltage signal is given as:

$$v^*_L(\omega t) = v^*_{L\alpha}(\omega t) = \sin(\omega t).(v_{sdf}) \tag{20}$$

The generated reference voltage signal is compared with actual load voltage signal to provide the pulse width modulated signal for the series inverter. The fundamental active part of the load current (i_{sda}) and load voltage (v_{sdf})is filtered out by the low-pass filter as shown in Fig. 2.

3.2 Single-Phase Unit Vector Controller

The important role of the series inverter of PV-1UPQC is to maintain sinusoidal voltage with ideal magnitude at the load terminal in the presence of distorted supply voltage from

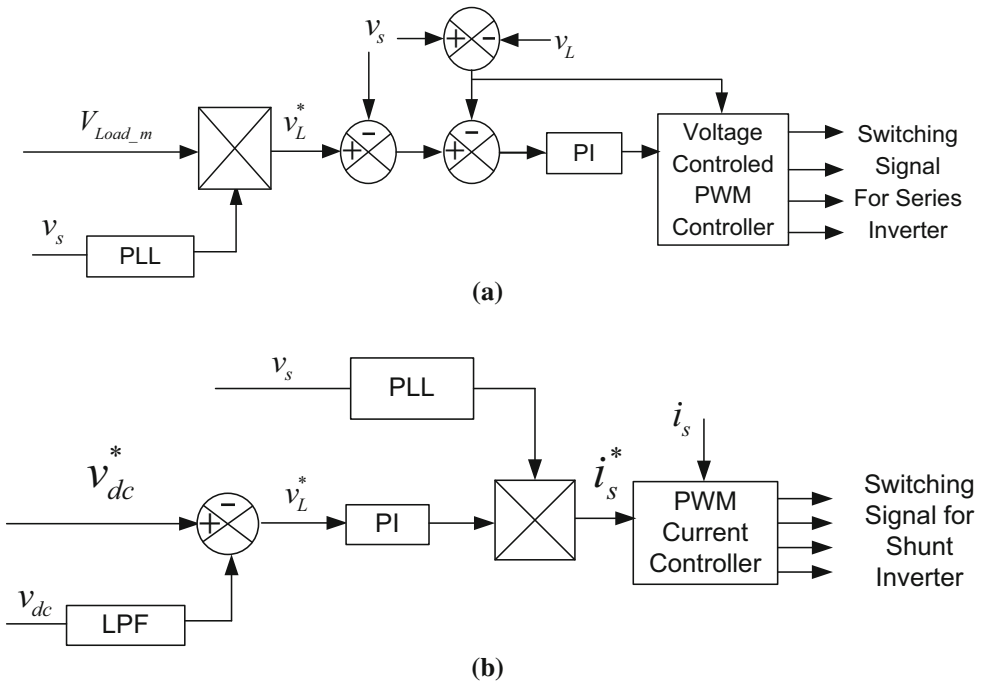


Fig. 3 Unit vector controller for single-phase PV-tied UPQC. **a** Series inverter controller, **b** shunt inverter controller

the grid. The distorted voltage available at the point of common coupling (PCC) consists of fundamental component v_{sf} and distorted harmonics-rich component v_{sd}. To maintain sinusoidal voltage and eliminate the voltage distortions, unit vector template (UVT) controller is applied here. The supply grid voltage is measured and multiplied by the gain of $1/V_m$, where the V_m represents the peak amplitude of the required signal. This method gives an approximated unity grid voltage profile.

For a considered application, it is obvious that the desired voltage magnitude is a known value. Therefore, it is assumed here $V_{\text{Load\_}m}$ be the peak amplitude load voltage at normal condition. By multiplying the value $V_{\text{Load\_}m}$ with the unit vector template U, the desired load voltage profile can be achieved. The desired load voltage reference v_L^* can be given as:

$$v_L^*(\omega t) = V_{\text{Load\_}m} \cdot U = V_{\text{Load\_}m} \cdot \sin(\omega t) \tag{21}$$

Generated reference voltage signal signal is compared with the actual signal to provide the switching pulses for the series inverter of the PV-1UPQC. Figure 3a shows the series inverter unit vector template (UVT) controller.

In a similar way, reference current signals for the shunt inverter are generated by unit vector template controller as shown in Fig. 3b. The shunt inverter of the PV-1UPQC is responsible for elimination of current quality issues. Therefore, to overcome all current quality issues, sinusoidal source current is desired. The grid voltage is sensed with PLL, and the unit template is generated. The measured DC-link voltage v_{dc} is compared with the reference DC-link voltage v_{dc}^* and error generated is passed through the PI controller. The output of the PI controller generates the peak amplitude of the fundamental current I_{peak}. By multiplying peak amplitude of fundamental current value I_{peak}, with the unit template value U, results in reference source current signal i_s^*.

$$i_s^*(\omega t) = I_{\text{peak}} \cdot U = I_{\text{peak}} \cdot \sin(\omega t) \tag{22}$$

The reference source current signal is compared with the actually sensed current to provide the PWM signal for switching of the shunt inverter of PV-1UPQC. This methodology eliminates significant complex transformations and provides easy platform for hardware implementations.

4 Proposed Controller based on Notch Filter PLL

The new methodology adopted in this control algorithm is the notch filter-based PLL mechanism which is employed for grid synchronization and fundamental grid voltage template extraction. Details of the notch filter-based PLL are presented here followed by shunt and series inverter controller.

4.1 Notch Filter-Based PLL

Grid syncronization is important for the control and performance enhancement of grid-connected systems. To achieve

proper grid synchronization for the detection of frequency and phase, various schemes of phase-locked loop have been introduced. The synchronous reference frame PLL is the most frequently used for estimation of phase angle and frequency of grid voltage. The SRF PLL adopts a park transformation to the measured grid voltage and 90° delayed component . The single-phase grid voltage in $\alpha-\beta$ frame $(v_{S\alpha}, v_{S\beta})$ can be represented as

$$v_{S\alpha} = V\cos(\omega t) \tag{23}$$

The 90° delayed signal is given as

$$v_{S\beta} = V\cos(\omega t + 90^\circ) = V\sin(\omega t) \tag{24}$$

Therefore, the park transformation is presented as

$$v_{Sdq} = \begin{bmatrix} \cos(\omega t) & \sin(\omega t) \\ \sin(\omega t) & -\cos(\omega t) \end{bmatrix} v_{S\alpha\beta} \tag{25}$$

where v_{Sdq} is source voltage in $d-q$ frame. Considering that the $\alpha-\beta$ components of the grid voltage have amplitudes of 1p.u, the $\alpha-\beta$ transformation provides a result with $v_{Sq}=0$. In spite of this considered situation, any little change in grid ideal frequency gives rise to nonzero q-axis voltage. Any small change in grid frequency introduces various samples of signals per cycle than N. This change in frequency incorporates phase error ϕ in $\beta-$ component of grid voltage and also affects v_{Sq}, which is given as

$$v_{Sq} = \sin(\omega t)\cos(\omega t) - \cos(\omega t)\sin(\omega t + \phi) \tag{26}$$

For any small change in value of ϕ,
$\sin(\phi) \approx \phi$ and $\cos(\phi) \approx 1$

$$\begin{aligned} v_{Sq} &\approx \cos(\omega t)(\sin(\omega t) - \sin(\omega t) - \cos(\omega t)\phi) \qquad (27)\\ &= -\cos^2(\omega t)\phi \\ &= \frac{-\phi}{2}(1+\cos(2\omega t)) \qquad (28) \end{aligned}$$

Equation (28) clearly reveals the presence of double frequency component in q-axis component of grid voltage, which results in frequency fluctuation in source. Therefore, a low-pass filter which has cutoff frequency $2\omega t$ can significantly boost the PLL response.

For better grid synchronization and to eliminate the issues with SRF PLL (synchronous reference frame-phase-locked loop), a low-pass notch filter with PLL has been introduced. Figure 2 shows the block diagram of low-pass notch filter-based PLL. Similar to previous PLL scheme, single-phase grid voltage is passed through $\alpha\beta - dq$ conversion system to produce direct as well as quadrature axis components. The obtained quadrature component of single-phase input voltage is passed through a low-pass notch filter. In general, low-pass notch filter has the characteristic to cancel any double frequency component or oscillation at the output. Adaptation of LPN-PLL (low-pass notch filter-based PLL) methodology does not affect much to the algorithm hardness and eliminates nonlinearity in the system. The basic second-order notch filter has two zeros and two poles whose transfer function is formulated as (29). It is the simplest notch filter structure presented in [18] can be given as

$$G(s) = K\frac{s^2 + (\omega_{\text{zero}})^2}{s^2 + \left(\frac{\omega_{\text{pole}}}{Q}\right)s + (\omega_{\text{pole}})^2} \tag{29}$$

where ω_{zero} is zero, ω_{pole} represents pole of the transfer function, Q is notch of the system, and K is gain of filter. Selection of zero and pole locations and the use of notch filter can be divided in two different ways. The considered notch filter could be standard notch filter or it can be also considered as low-pass notch filter. Assuming the presence of two states with the notch filters such as x_1 and x_2, state space representation is given below:

$$\begin{bmatrix} \dot{x}_1 \\ \dot{x}_2 \end{bmatrix} = \begin{bmatrix} \frac{-\omega_{\text{pole}}}{Q} & -\omega_p^2 \\ 1 & 0 \end{bmatrix}\begin{bmatrix} x_1 \\ x_2 \end{bmatrix} + \begin{bmatrix} 1 \\ 0 \end{bmatrix}\begin{bmatrix} v_{Sq} \end{bmatrix} \tag{30}$$

The resultant of the LPN filter represented as filtered voltage

$$v_{q\_\text{filter}} = \begin{bmatrix} -K\frac{\omega_{\text{pole}}}{Q} & K\left(\omega_{\text{zero}}^2 - \omega_{\text{pole}}^2\right) \end{bmatrix}\begin{bmatrix} x_1 \\ x_2 \end{bmatrix} + [K]\begin{bmatrix} v_{Sq} \end{bmatrix} \tag{31}$$

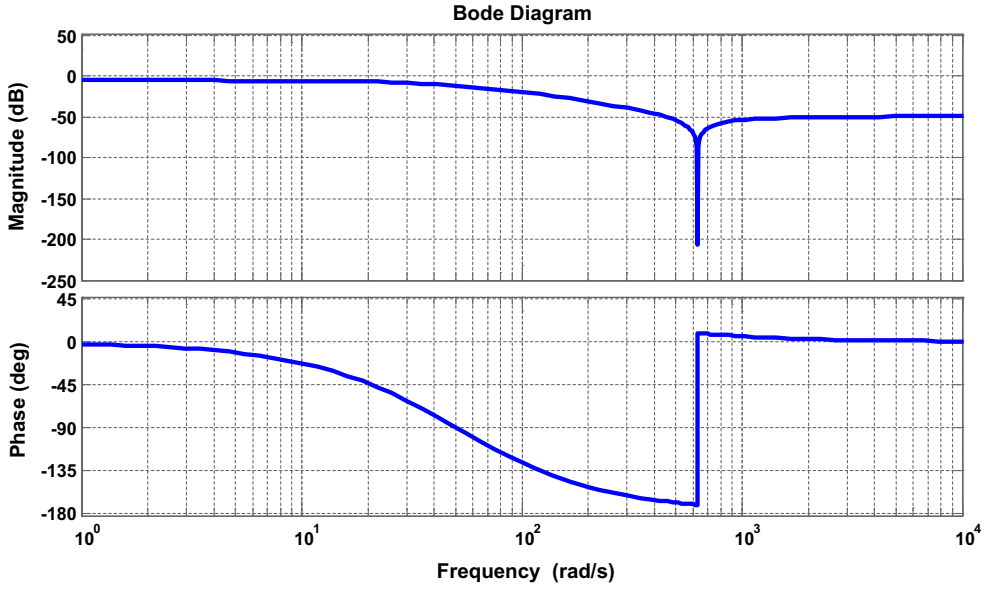
where v_{q_filter} is filtered voltage by LPN filter.

4.2 Parameter Design and Selection of Notch Filter

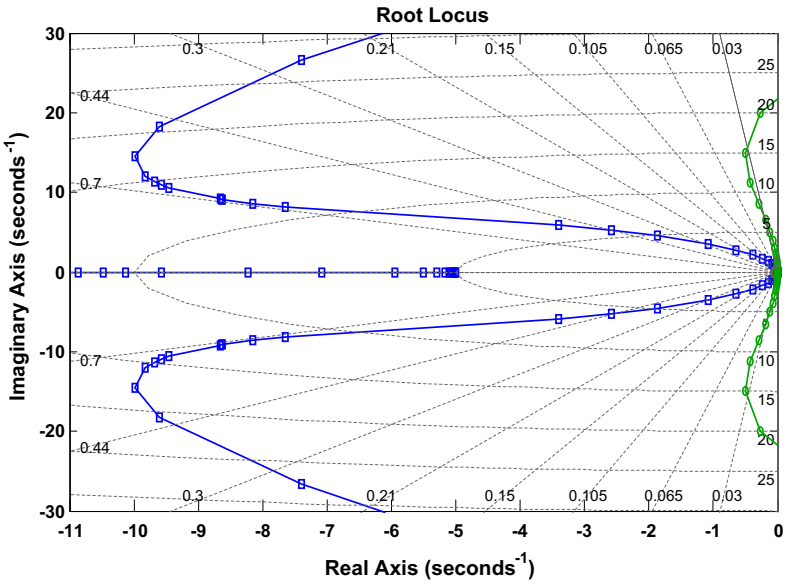
Based on the transfer function of notch filter as given by Eq. (29), essential filter parameters are selected. The low-pass notch filter considered here is achieved on satisfying the following condition:

$$\omega_{\text{zero}} > \omega_{\text{pole}} \tag{32}$$

where ω_{zero} is zero and ω_{pole} represents pole of the transfer function. The notch filter is employed in the PLL to eliminate double frequency harmonics generated as a result of to error in $v_{S\beta}$. Therefore, center frequency is selected twice of grid frequency. So system discussed here with nominal frequency of 50 Hz, the notch filter is tuned at $2\times 2\times\pi\times 50 = 628$ rad/s. The ω_{zero} is selected at 628 rad/s, ω_{pole} is found as 50 rad/s, and gain(K) is 0.0032278. MATLAB SISO tool box is responsible to find the values of ω_{zero}, ω_{pole} and gain(K). The gain controls the pass band magnitude of notch filter.



(a)



(b)

Fig. 4 Notch filter plots: **a** bode plot for notch filter, **b** root locus plot for gain design of notch

For this considered system, notch Q is considered to be 0.5. The stability of transfer function of notch filter is presented in Fig. 4a.

The open-loop transfer function of low-pass notch filter-based PLL is given as

$$H_{\text{open}} = k_p\left(1+\frac{k_i/k_p}{s}\right)\left(K\frac{s^2+(\omega_{\text{zero}})^2}{s^2+(\frac{\omega_{\text{pole}}}{Q})s+(\omega_{\text{pole}})^2}\right)\frac{1}{s} \tag{33}$$

Assigning the parameters if notch filter

$$H_{\text{open}} = k_p\left(1+\frac{k_i/k_p}{s}\right)\left(\frac{(0.0032278)(s^2+628^2)}{s^2+100s+2500}\right)\frac{1}{s} \tag{34}$$

The root locus plots are presented in Fig. 4b. The dynamics of the system is regulated by suitable gain design through root locus. The overshoot lines of 10 and 5% are with damping ratio of 0.59, 0.69. it is shown from the root locus that k_i/k_p ratio of 20 does not cross the desired overshoot lines. The root locus curve obtained from k_i/k_p value of 5 shows that it reaches the damping ratio curves and is found to be

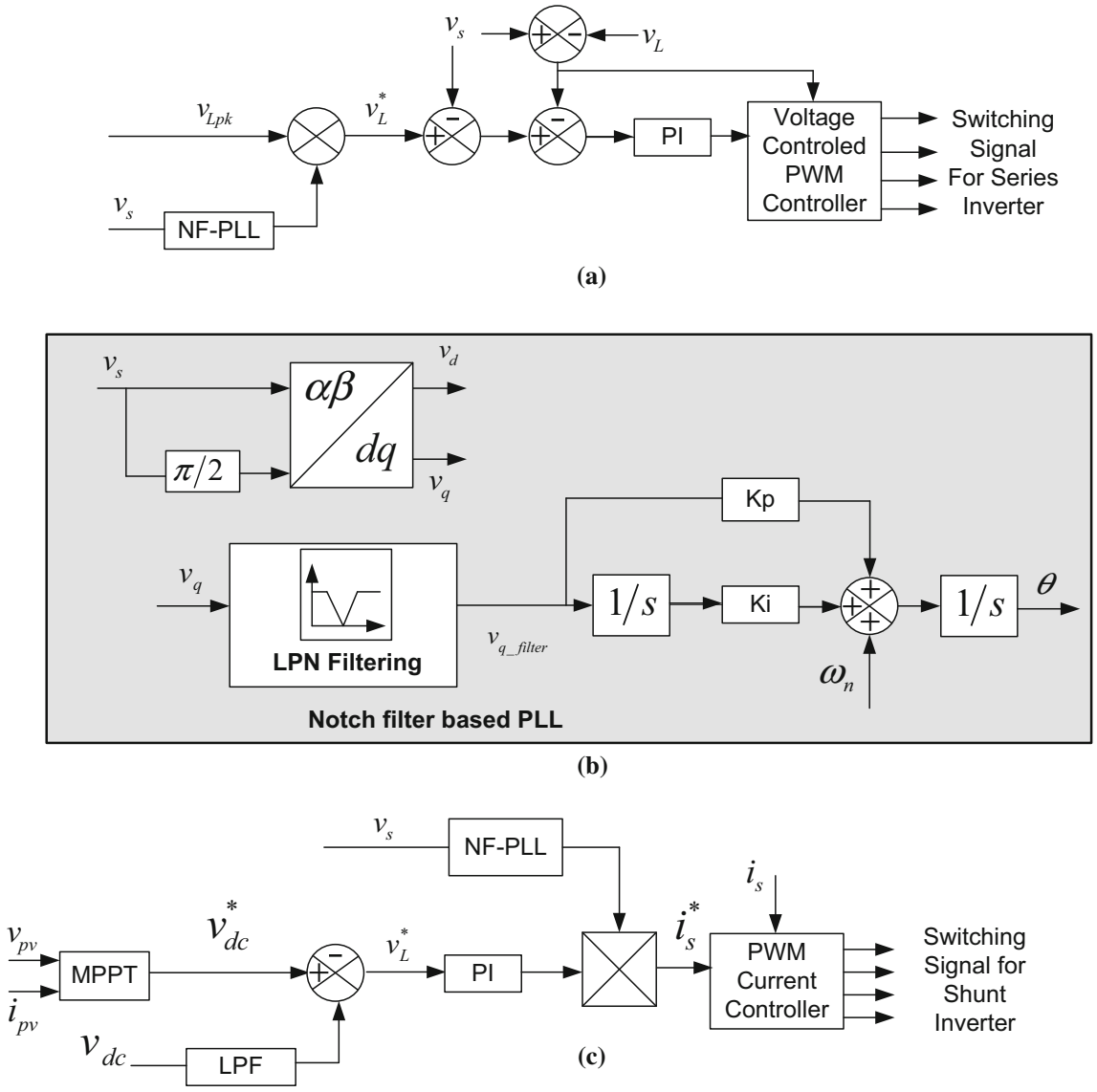


Fig. 5 Block diagram of proposed notch filter PLL-based controller for single-phase PV-tied UPQC: **a** controller for series inverter, **b** block diagram of notch filter-based PLL, **c** controller for shunt inverter

very closer to imaginary axis. An appropriate k_p gain can be obtained which falls between the intersections root locus curves and damping ratio curves. Therefore, a suitable gain of 15.2 is chosen which is found to be closer to the semicircle, imaginary axis and with faster rise time. The gain of 15.2 has a rise time of 6.82 cycles.

5 Notch Filter–PLL-Based Controller

5.1 Proposed Controller for PV-1UPQC

The notch filter-based PLL discussed above is the important modification in the controller of PV-tied UPQC. According to this controller simulation and experimentation, results are presented in the following sections. Voltage perturbations which appear in the grid or in load side are regulated by the series inverter of PV-tied UPQC. The reference peak load voltage which is sensed from the grid is multiplied with the template of fundamental grid voltage which results in generation of reference load voltage. The difference generated by comparing the source grid voltage with load voltage is the voltage error. The detail of the controller is given in Fig. 5. The voltage error generated is again subtracted from the reference series inverter voltage. The output generated is given to PI controller. A voltage controlled PWM generator is employed to generate the necessary switching pulses.

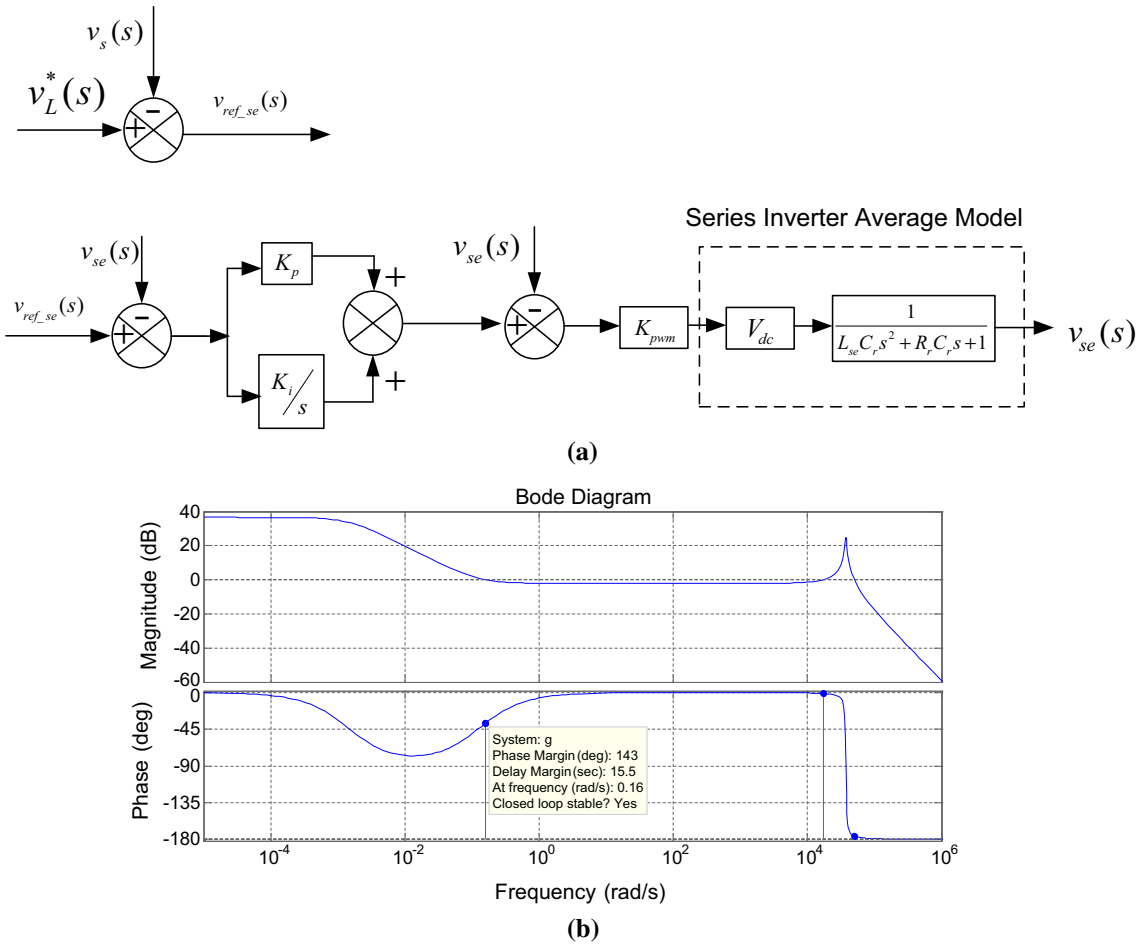


Fig. 6 Proposed Notch filter PLL-based controller for series inverter of PV-tied UPQC: **a** signal flow graph of voltage controller, **b** bode plot of closed loop transfer function of proposed series inverter controller

Shunt inverter of the PV-tied UPQC is engaged to deal with the current harmonics. The shunt inverter is also responsible for injecting the PV power to the grid. The detail control structure of shunt inverter controller is presented in Fig. 5c. The regulation of reference DC-link voltage is based on MPPT algorithm. Perturb and observe technique is applied to extract maximum power from the PV array. The notch filter-based PLL is utilized for the perfect grid synchronization. The DC-link controller implemented generates the equivalent current, which is exactly equal to the loss of power required to regulate DC-link voltage. In similar way as presented in Sect. 3, the controller for shunt inverter acts.

5.2 Stability Analysis of the Proposed Controller

5.2.1 Stability Analysis Through Bode Plot

Signal flow graph of voltage controller is given in Fig. 6a, v_{ref_se} is generated reference for series inverter, and v_{se} is actual voltage of compensator. The constant $K_{\text{pwm}} = 1/P_{\text{pwm}}$ represents the static gain of the series inverter [23], and P_{pwm} is the peak of PWM triangular carrier. K_p and K_i are gain of proportional and integral controller. L_{se}, C_r and R_r are the ripple filter parameters for series inverter of UPQC. From Fig. 6a, the closed loop transfer function can be derived by following steps:

$$\left[\left\{\left(v_{ref\_se}(s) - v_{\text{se}}(s)\right)\left(K_p + \frac{K_i}{s}\right)\right\} - v_{\text{se}}(s)\right]\left(K_{\text{pwm}}.V_{\text{dc}}.\frac{1}{L_{\text{se}}C_r s^2 + R_r C_r s + 1}\right) = v_{\text{se}}(s) \tag{35}$$

$$\Rightarrow \left[\left\{\left(v_{ref\_se}(s) - v_{\text{se}}(s)\right)\left(K_p + \frac{K_i}{s}\right)\right\} - v_{\text{se}}(s)\right]\left(X_1.\frac{1}{L_{\text{se}}C_r s^2 + R_r C_r s + 1}\right) = v_{\text{se}}(s) \tag{36}$$

$$\frac{v_{\text{se}}(s)}{v_{ref\_se}(s)} = \frac{\left(K_p + \frac{K_i}{s}\right).X_1}{L_{\text{se}}C_r s^2 + R_r C_r s + 1 + K_p + \frac{K_i}{s} + X_1} \tag{37}$$

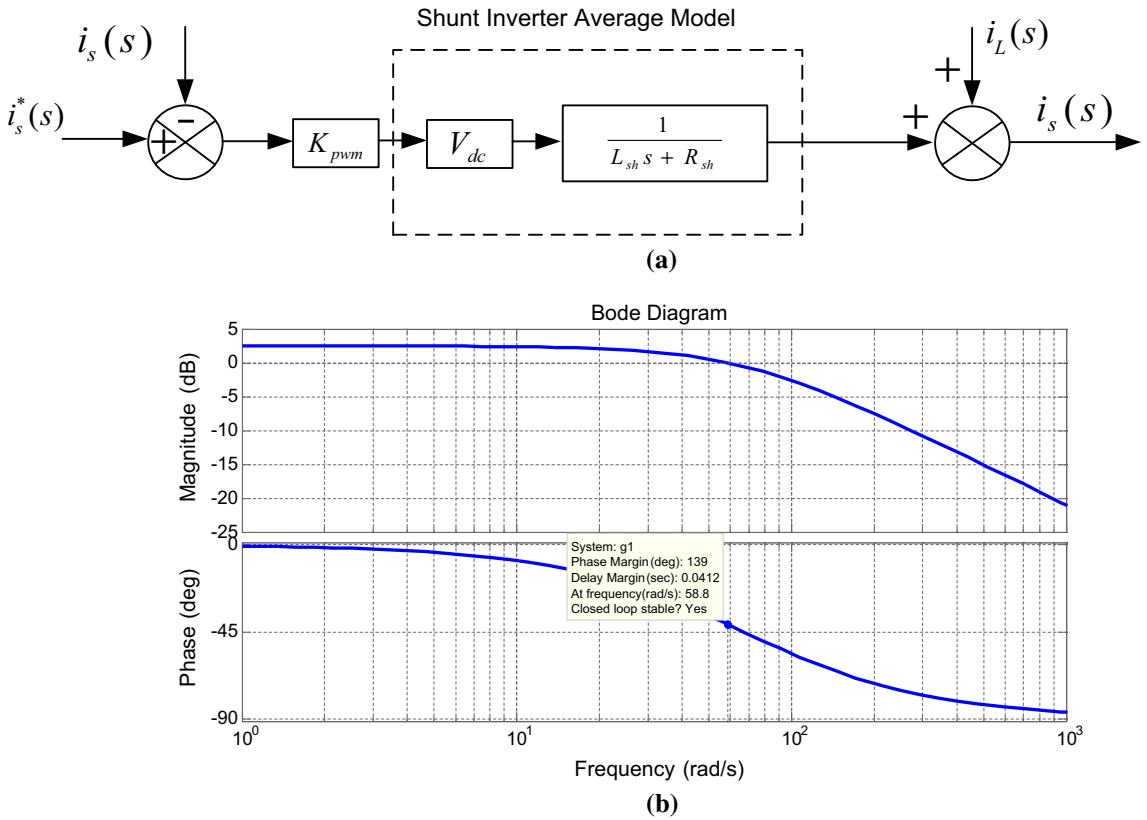


Fig. 7 Proposed notch filter PLL-based controller for shunt inverter of PV-tied UPQC: **a** signal flow graph of current controller, **b** bode plot of closed loop transfer function of proposed shunt inverter controller

$$\Rightarrow \frac{v_{\text{se}}(s)}{v_{ref\_se}(s)} = \frac{K_p X_1 s + K_i X_1}{L_{\text{se}} C_r s^3 + R_r C_r s^2 + \left(1 + K_p + X_1\right) + K_i} \tag{38}$$

By considering various parameters for the closed loop transfer function (39) and tuning the K_p and K_i gains bode diagram of (39) can be achieved, presented in Fig. 6b. It is obvious from the bode diagram that controller is stable at the particular gain of proportional and integral controller. The parameters considered for the closed loop transfer function are $K_p = 0.3$, $K_i = 0.12$, $P_{\text{pwm}} = 4VL_{\text{se}} = 6\,mH$, $C_r = 10\,\mu F$ and $R_r = 2\,\Omega$.

The closed loop transfer function of shunt inverter controller of PV-UPQC is presented in (42), which is obtained by the signal flow graph as presented in Fig. 7a. The sinusoidal source current after compensation is presented as i_s, and the reference source current is denoted as i_s^*. L_{sh}, R_{sh} are the interfacing inductance of shunt inverter side of UPQC. The closed loop transfer function can be achieved by the following steps.

$$\left[\left(i_s^*(s) - i_s(s)\right).K_{\text{pwm}}.V_{\text{dc}}.\frac{1}{L_{\text{sh}}s + R_{\text{sh}}}\right] + i_L(s) = i_s(s) \tag{39}$$

$$\frac{i_s(s)}{i_s^*(s)} = \frac{K_{\text{pwm}}.V_{\text{dc}}.\frac{1}{L_{\text{sh}}s+R_{\text{sh}}}}{1 + K_{\text{pwm}}.V_{\text{dc}}.\frac{1}{L_{\text{sh}}s+R_{\text{sh}}}} \tag{40}$$

$$\frac{i_s(s)}{i_s^*(s)} = \frac{X_2}{L_{\text{sh}}s + R_{\text{sh}} + X_2} \tag{41}$$

The stability analysis of the closed loop transfer function for proposed shunt controller can be achieved through bode diagram of (13) with respect to various parameter configuration for the system controller such as $P_{\text{pwm}} = 4VL_{\text{sh}} = 2.02\,mH$, $R_{\text{sh}} = 1.5\,\Omega$ and $V_{\text{dc}} = 450\text{V}$. It is clearly shown in Fig. 7b that the closed loop transfer function for current controller is stable.

5.2.2 Stability Analysis Using Routh's Stability Criterion

Theoretical analysis of controller stability for the present system has been addressed in this section. As bode plot is a graphical method to determine the system stability as analyzed for the present system in the above section, the theoretical analysis of system stability has been established through Routh's stability criterion. The present stability criterion is applied to the system controller, and information about the absolute stability can be obtained from stepwise satisfying the conditions of considered stability criterion. The

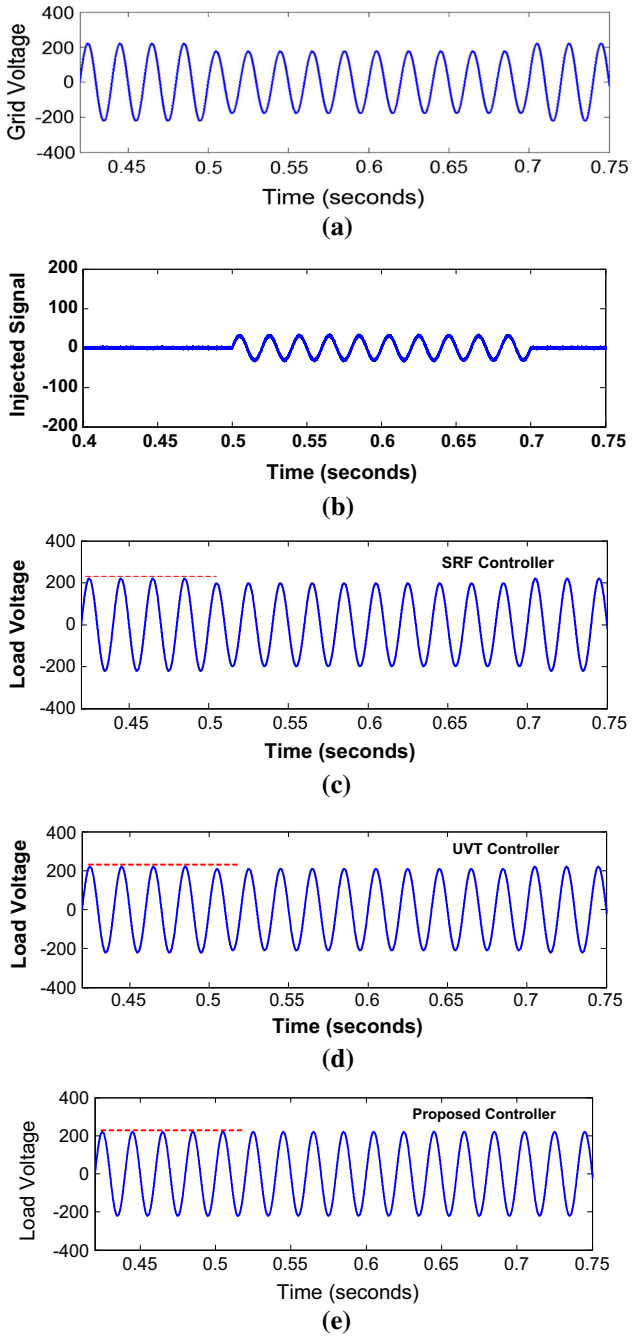


Fig. 8 Voltage sag compensation by PV-1UPQC: **a** grid voltage with sag, **b** injected series inverter voltage, **c** compensated load voltage by SRF controller, **d** load voltage with UVT controller, **e** load voltage with proposed method

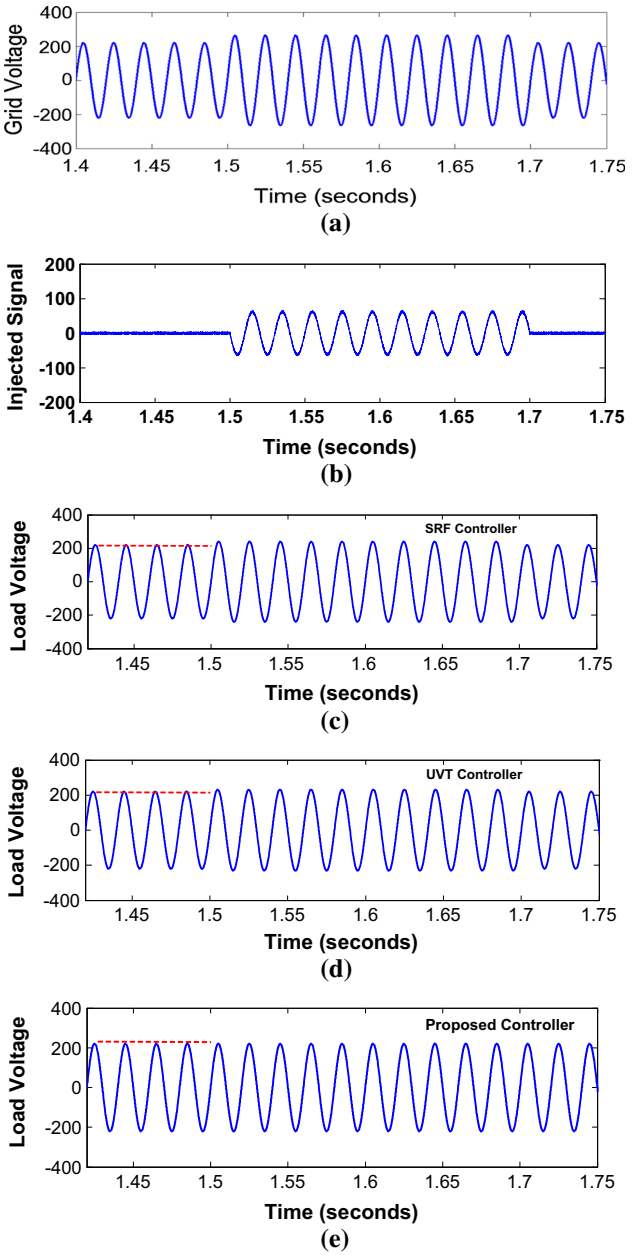


Fig. 9 Voltage swell compensation by PV-1UPQC: **a** grid voltage with swell, **b** injected series inverter voltage, **c** compensated load voltage by SRF controller, **d** load voltage with UVT controller, **e** load voltage with proposed method

systematic procedure of Routh's stability for the controller of PV-1UPQC is as follows:

The closed loop system transfer function as presented in Eq. (38) for series inverter of PV-1UPQC can be presented in the form of standard closed loop transfer function. The standard closed loop transfer function can be given as

$$\frac{C(s)}{R(s)} = \frac{b_0 s^m + b_1 s^{m-1} + \cdots + b_{m-1} s + b_m}{a_0 s^n + a_1 s^{n-1} + \cdots + a_{n-1} s + a_n}, \tag{42}$$

The following steps are required for Routh's stability criterion.

Step 1 Considering all the parameters of the close loop transfer function of the system as presented in Sect. 5.2.1, the transfer function of Eq. (38) can be given as

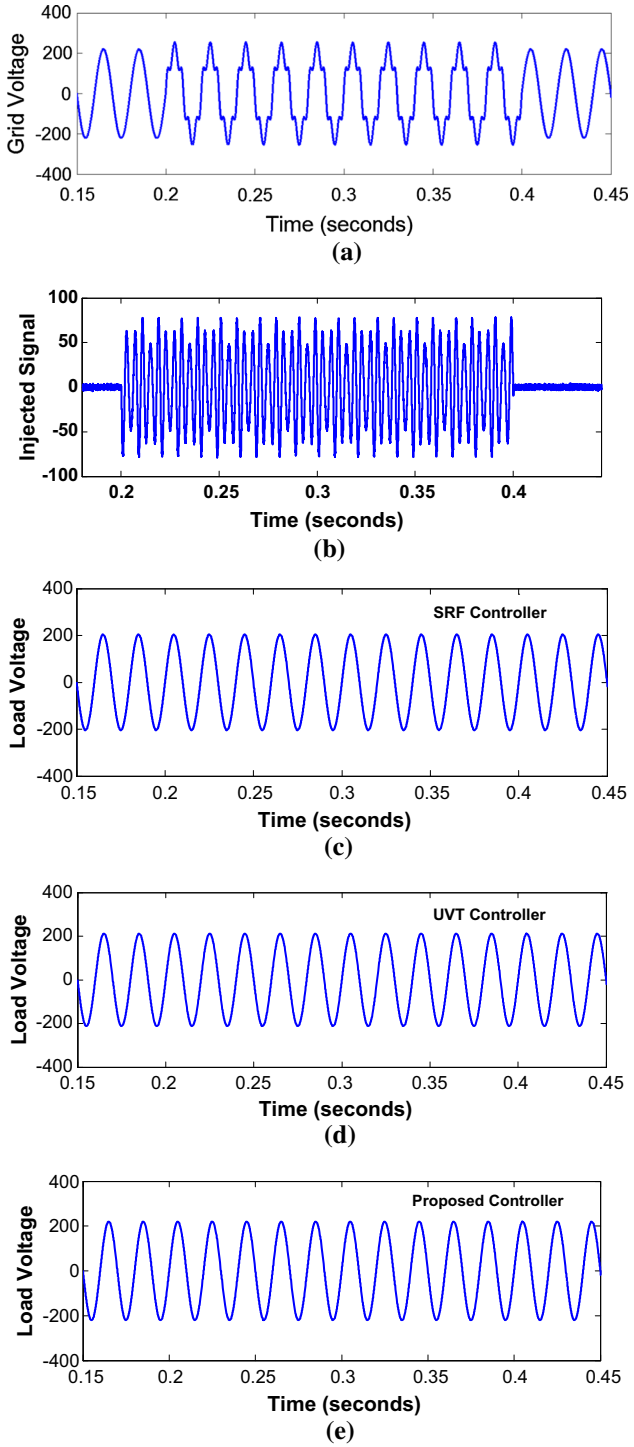


Fig. 10 Voltage harmonics compensation by PV-1UPQC: **a** grid voltage with harmonics, **b** injected series inverter voltage, **c** compensated load voltage by SRF controller, **d** load voltage with UVT controller, **e** load voltage with proposed method

$$\frac{C(s)}{R(s)} = \frac{33.75 \times 10^8 s + 13.5 \times 10^8}{6s^3 + 2000s^2 + 113.8 \times 10^8 s + 0.12 \times 10^8} \quad (43)$$

the $R(s)$ for Eq. (43) is presented as

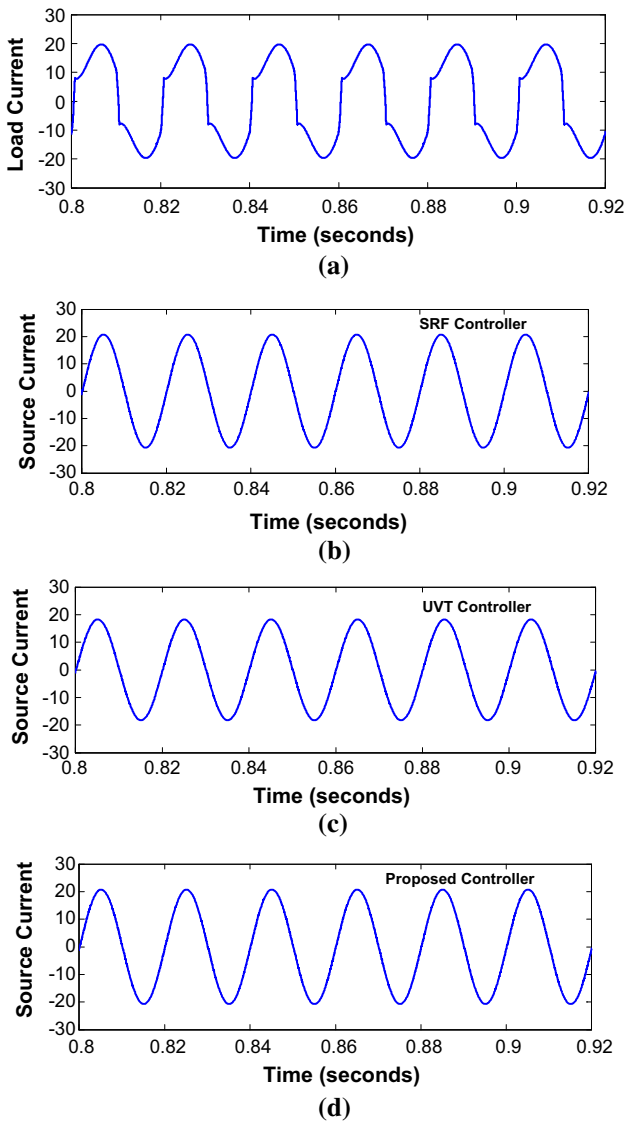


Fig. 11 Current harmonics compensation by PV-1UPQC: **a** load current with harmonics, **b** source current with SRF controller after compensation, **c** source current with UVT controller, **d** source current with proposed method

$$R(s) = 6s^3 + 2000s^2 + 113.8 \times 10^8 s + 0.12 \times 10^8 \quad (44)$$

It is assumed that any zero root is eliminated and $a_n \neq 0$.

Step 2 If any of the coefficients are negative or any sign change, there is chance of a root that is imaginary. In such case, the system is not stable. In this system, transfer function $R(s)$, all the coefficients are positive.

Step 3 As all the coefficients are positive, the coefficients are arranged according to the pattern of Routh table. The array of the coefficients is presented as follows

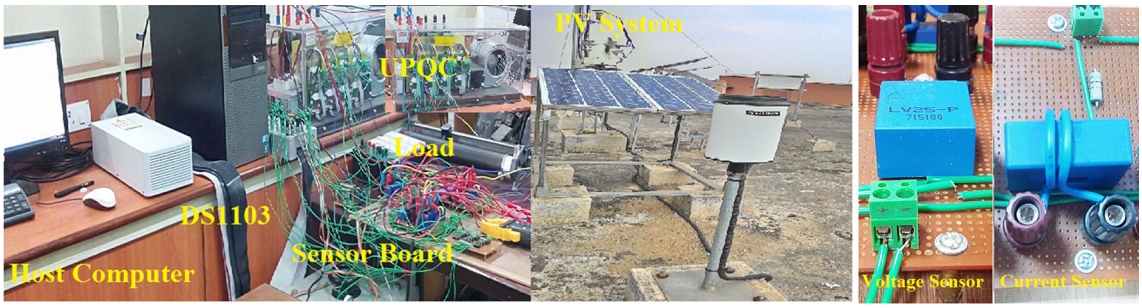


Fig. 12 Experimental setup of PV-1UPQC: laboratory prototype, PV system, current and voltage sensors

Table 2 Experimental prototype details

Parameters	Value
Grid voltage	50 V
Fundamental frequency	50 Hz
Source inductance	0.4 mH
DC-bus capacitor	1150 μF
Series inverter coupling inductance	2.5 mH
Ripple filter	3μF, 5 Ω
Shunt inverter coupling inductance	2.1 mH
Nonlinear load	20Ω/30 mH
Series transformer ratio	1:2
Switching frequency	8 kHz
Sampling time	50 μs

$$\begin{array}{llll} s^3 & a_0 & a_2 \\ s^2 & a_1 & a_3 \\ s^1 & b_1 & b_2 \\ s^0 & c_1 & c_2 \end{array} \Rightarrow \begin{array}{lll} s^3 & 6 & 113.8 \times 10^8 \\ s^2 & 2000 & 0.12 \times 10^8 \\ s^1 & 113.8 \times 10^8 & 0 \\ s^0 & 0.12 \times 10^8 & 0 \end{array}$$

From the above Routh table, it can be concluded that there is no sign change in the first column of Routh table; therefore, all the poles lie in the left-half of the s-plane. Hence, from the above condition we can conclude that the above closed loop system is stable.

In a similar way, the closed loop system transfer function as presented in Eq. (41) for the shunt inverter control can be presented in the form of (42), is presented in (45). The steps for determining the stability by Routh's stability criterion are as follows:

Step 1 Considering all the parameters of the controller as presented in Sect. 5.2.1, the transfer function can be given as

$$\frac{C(s)}{R(s)} = \frac{112.5}{2.02 \times 10^3 s + 114}, \tag{45}$$

$$\text{where } R(s) = 2.02 \times 10^3 s + 114 \tag{46}$$

It is assumed that any zero root is eliminated and $a_n \neq 0$.

Step 2 If any of the coefficients are negative or any sign change, there is chance of a root that is imaginary. In such case, the system is not stable. In this system transfer function $R(s)$, all the coefficients are positive.

Step 3 As all the coefficients are positive, the coefficients are arranged according to the pattern of Routh table. The array of the coefficients is presented as follows

$$\begin{array}{lll} s^1 & 2.02 \times 10^3 & 0 \\ s^0 & 114 & 0 \end{array}$$

From the above Routh table, it is clearly found that there is no sign change in the first column; therefore, the number of poles on the right hand side of s-plane is zero. Hence, we can conclude that the above closed loop system is stable. As both the transfer function of the system is stable, the system is completely stable.

6 Simulation Results and Discussion

To show the effectiveness of proposed controller for elimination of voltage sags, approximately 20% sags are considered for evaluation purpose. It is clearly noticed from Fig. 8a that at the point of 0.5s, voltage sag has been introduced in grid voltage, up to 0.7s. For the compensation of this sag in grid voltage, series inverter of PV-tied UPQC system inject compensation signal shown in Fig. 8b. As the load voltage is desired to be constant to perform normal operation, sag present in the grid voltage is compensated by PV-tied UPQC. It is shown in Fig. 8c, d that elimination of voltage sag is not precise by the SRF controller and UVT controller. However, the proposed controller completely removes the sag and maintains load voltage as presented in Fig. 8e.

At the instance voltage swell occurs in the grid, consumer loads are fed with more than its capacity which leads to abnormal operation. Therefore, it is eliminated by the proposed system. Voltage swell present in the grid is shown in Fig. 9a which is compensated by compensating signal injected by series inverter as shown in Fig. 9b. After complete compensation, the load voltage is maintained at normal level.

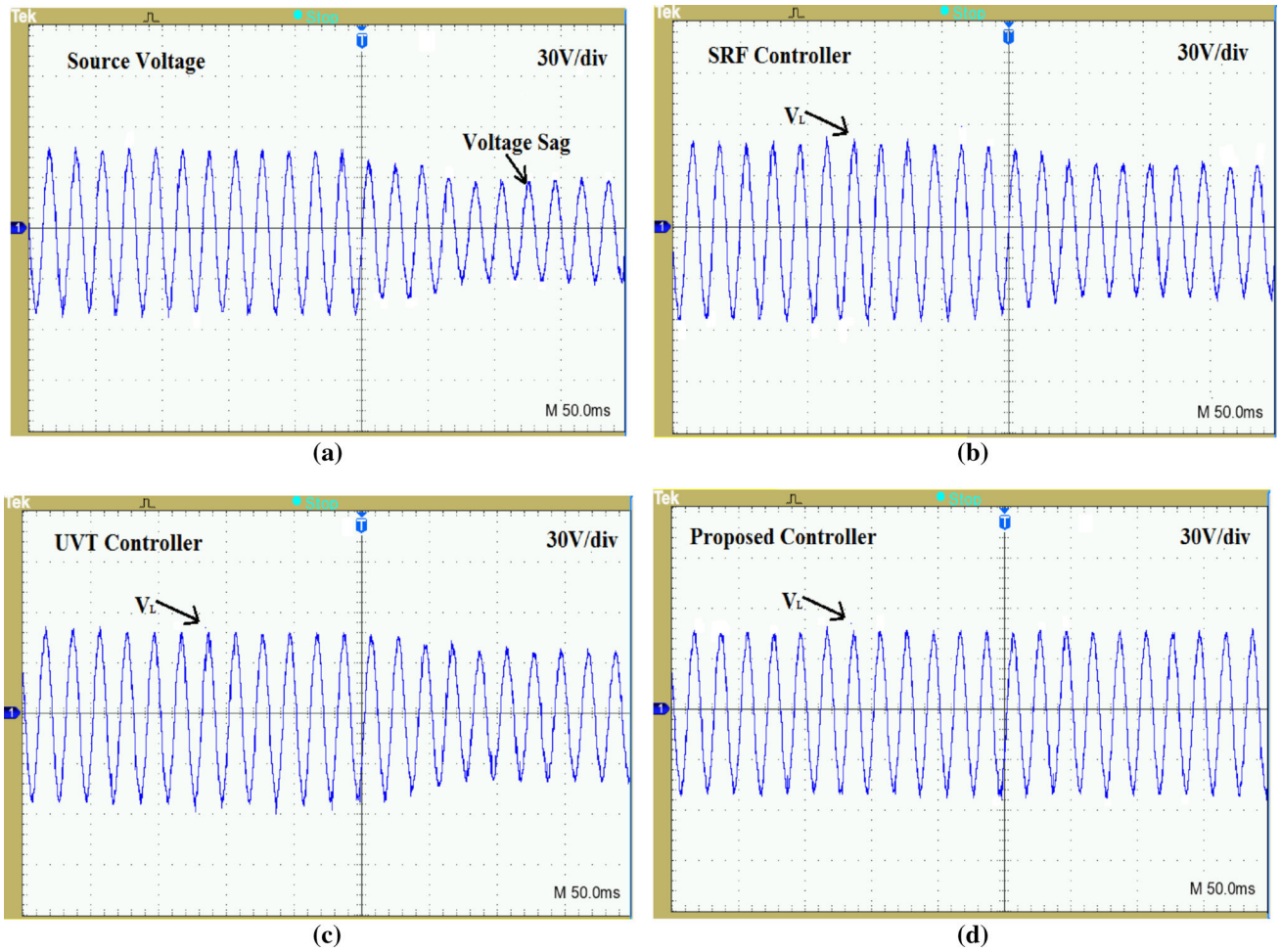


Fig. 13 Voltage sag compensation: **a** source voltage sag, compensation by PV-tied UPQC with **b** SRF controller, **c** UVT controller, **d** proposed controller

The results obtained by implementation of conventional controllers such as SRF and UVT controller for compensation of voltage swell are presented in Fig. 9c, d. It is revealed from the simulation results that proposed notch filter PLL-based controller has effectiveness toward complete voltage swell compensation which is presented in Fig. 9e.

Voltage harmonics are the another class of disturbances considered for voltage quality issues. The presence of voltage harmonics in the grid voltage is shown in Fig. 10a, and the compensation signal generated by series inverter of PV-1UPQC is presented in Fig. 10b. Proposed PV-1UPQC eliminates the harmonic content, and load voltage is maintained at desired level. Conventional controllers such as SRF and UVT controller eliminate voltage harmonics but cannot maintain the load voltage at perfect sinusoidal and desired level as presented in Fig. 10c, d. Therefore, proposed controller is utilized for effective voltage harmonics elimination as shown in Fig. 10e.

Nonlinear loads connected to the source grid are the major cause for harmonics in load current. Harmonic contamination prevents the current being sinusoidal as shown in Fig. 11a. However, proposed topology of PV-1UPQC shows its performance by eliminating the current harmonics to maintain sinusoidal source current as desired, which is presented in Fig. 11d. The SRF and UVT controllers also eliminate current harmonics but failed to perform as of proposed controller. The simulation results of source current obtained by SRF controller are shown in Fig. 11b and by UVT controller are given in Fig. 11c.

7 Experimental Setup Development and Discussion on Results

The performance evaluation and validation of proposed grid-connected system with proposed controller through experimentation is very much essential. Therefore, a hardware prototype is developed in the laboratory with PV system installed in the roof. The detailed structure of the prototype

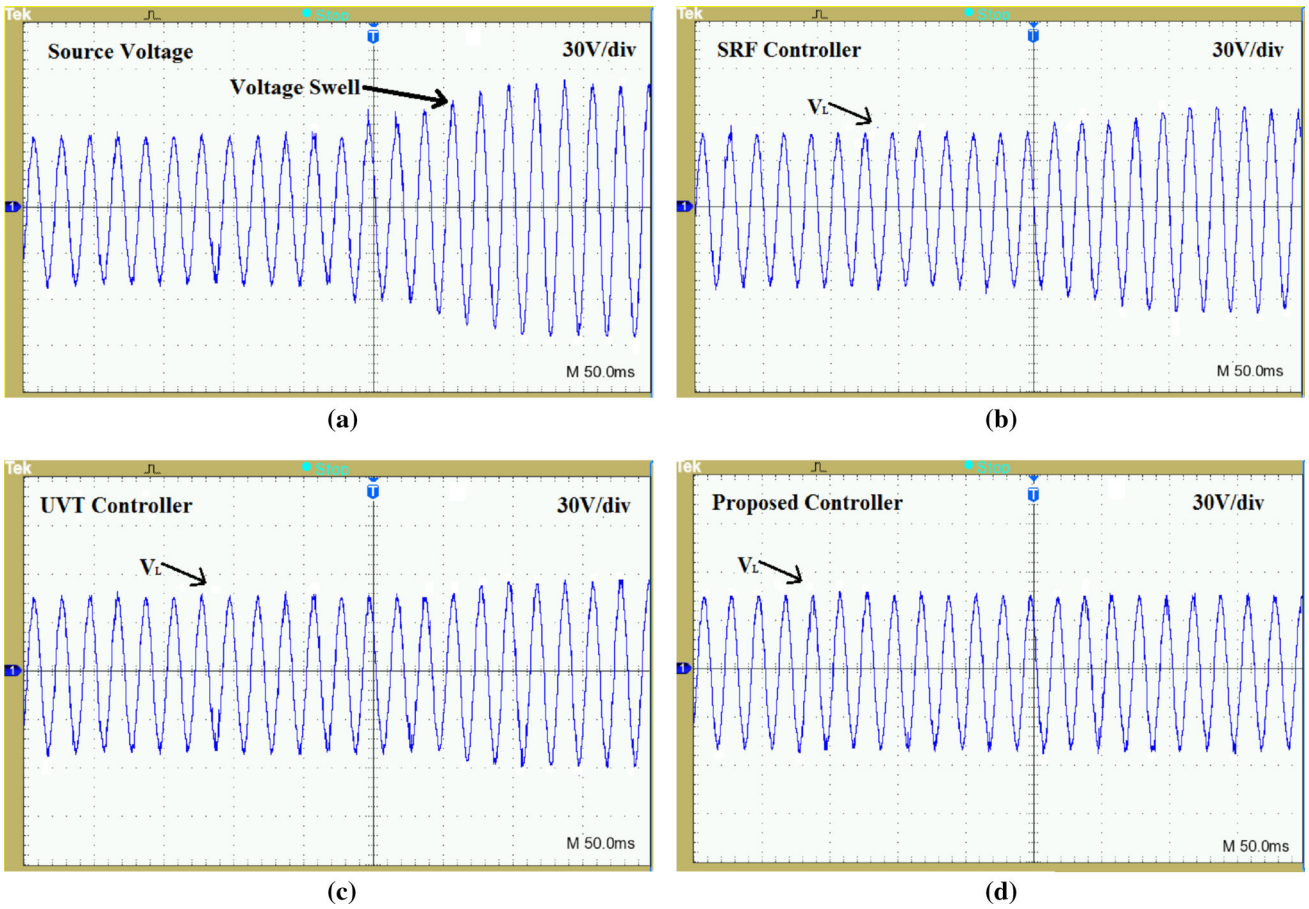


Fig. 14 Voltage swell compensation (30V/div): **a** grid voltage during swell, load voltage after compensation by PV-tied UPQC with **b** SRF controller, **c** UVT controller, **d** proposed controller

is given in Fig. 12. The system parts that are utilized for prototype development are :

(1) Programmable AC supply
(2) Installed PV array
(3) Series transformer
(4) Back to back inverter
(5) DS1103 with real-time interface
(6) Inductors and resistors for load
(7) filter inductors
(8) voltage sensors LV-25-P
(9) current sensors LA-55-P
(10) DC-bus capacitor
(11) Host computer
(12) Digital storage oscilloscope
(13) IGBT driver circuit
(14) Isolation circuit

The host computer, DS1103 digital controller and outside real hardware prototype work in a loop. All these components are interfaced with each other. The utilization of ADC and DAC channels of the DS1103 switching signals is generated and given to back to back-connected SEMIKRON inverter. The generated PWM pulses have the magnitude of 5 volts, but SEMIKRON inverters require 15-volt signal to operate. Therefore, dSPACE 5-volt signals are passed through CD4504 (voltage-level shifter) driver. This CD4504 amplifies PWM voltage magnitude level to 15 volt, which is acceptable by SEMIKRON inverter. The functional diagram of CD4504 is given in [24]. Voltage and current signals fed to DSPACE controller are sensed by Hall effect sensors (LV-25-P, LA-55-P). Protection circuit is installed to avoid any abnormal situation and malfunction of the prototype due to voltage spikes, over-currents. The prototype developed model is tested with reduced voltage level of 50 V. Switching frequency of 8 kHz is considered for the system operation. The system parameters that have been adopted for experimental purpose are given in Table 2.

The grid voltage with sag presented in Fig. 13a and load voltage after compensation by series inverter with proposed controller is shown in Fig. 13d. It is clearly observed from the figure that voltage sag is compensated by the proposed

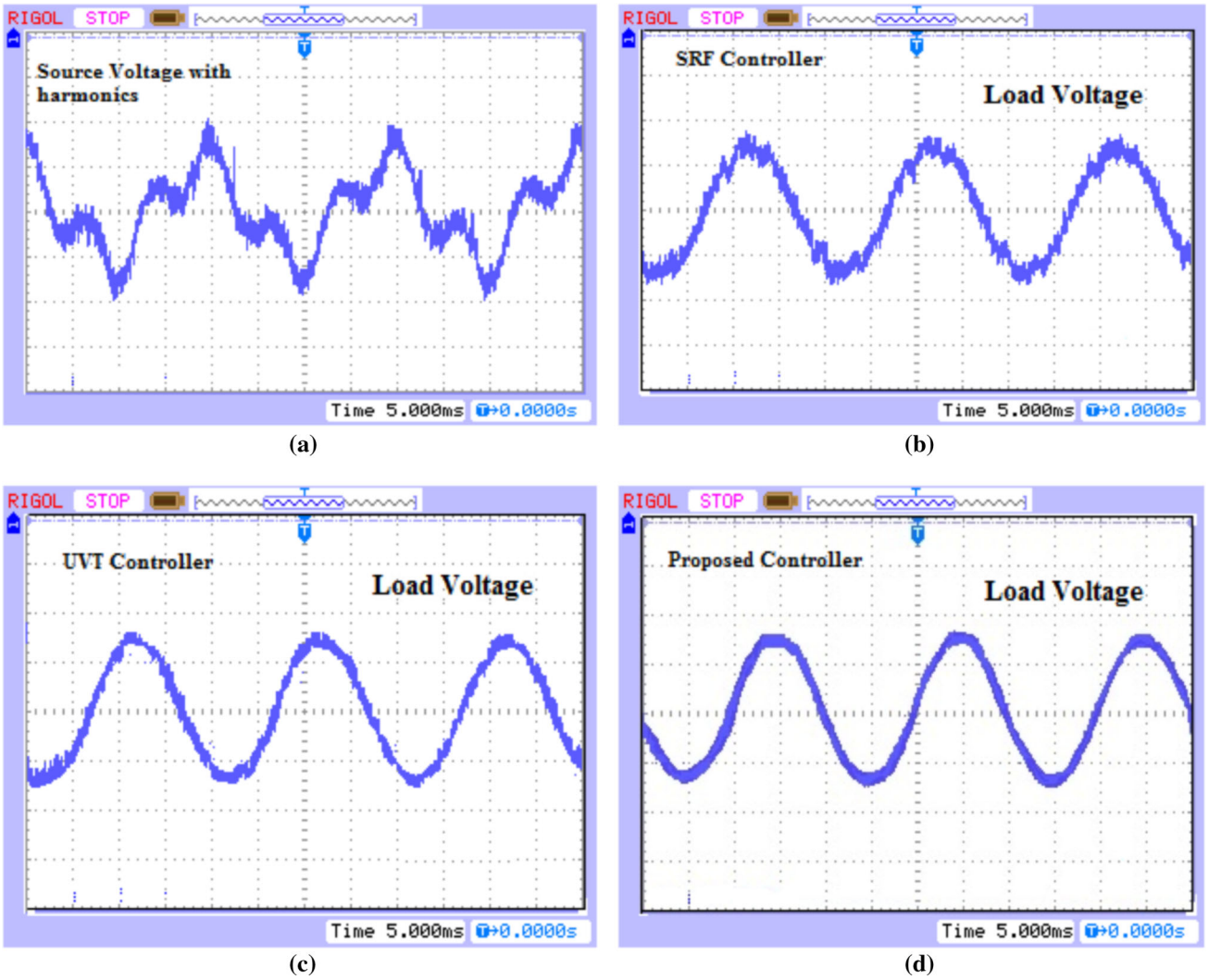


Fig. 15 Voltage harmonics compensation (30V/div): **a** grid voltage with harmonics, load voltage after compensation by PV-tied UPQC with **b** SRF controller, **c** UVT controller, **d** proposed controller

methodology, and load voltage is maintained at constant level. Voltage sag compensation by conventional SRF controller and UVT controller is given in Fig. 13b, c, respectively. Voltage swell that appears in grid voltage is shown in Fig. 14a. The presence of voltage swell creates abnormal operation at the load end, which is completely undesirable. Therefore, elimination of voltage swell is necessary. Series inverter of PV-tied UPQC generates the compensation signal to cancel voltage swell. The load voltage after voltage swell compensation by conventional controllers and proposed controller is presented in Fig. 14b, c, d, respectively. Grid voltage rich in harmonics is another major voltage disturbances that is clearly mentioned in voltage quality issues. The presence of harmonics in grid voltage is shown in Fig. 15a. This voltage harmonics are eliminated by PV-tied UPQC with the proposed controller, and perfect sinusoidal voltage is maintained at load end which is shown in Fig. 15d. Voltage harmonics compensation by SRF controller and UVT controller has been performed, and results are presented in Fig. 15b, c, respectively, for performance evaluation. Similarly current harmonics are also major issues related to grid current. As the grid is feeding the nonlinear load, harmonics are injected to the power system. The harmonics-rich load current is shown in Fig. 16a. Shunt inverter of PV-tied UPQC is responsible for current harmonics elimination. Source current after harmonics compensation is shown in Fig. 16d by proposed controller. Total harmonic distortion before and after current harmonics compensation is shown in Fig. 17 for conventional controller and proposed controller.

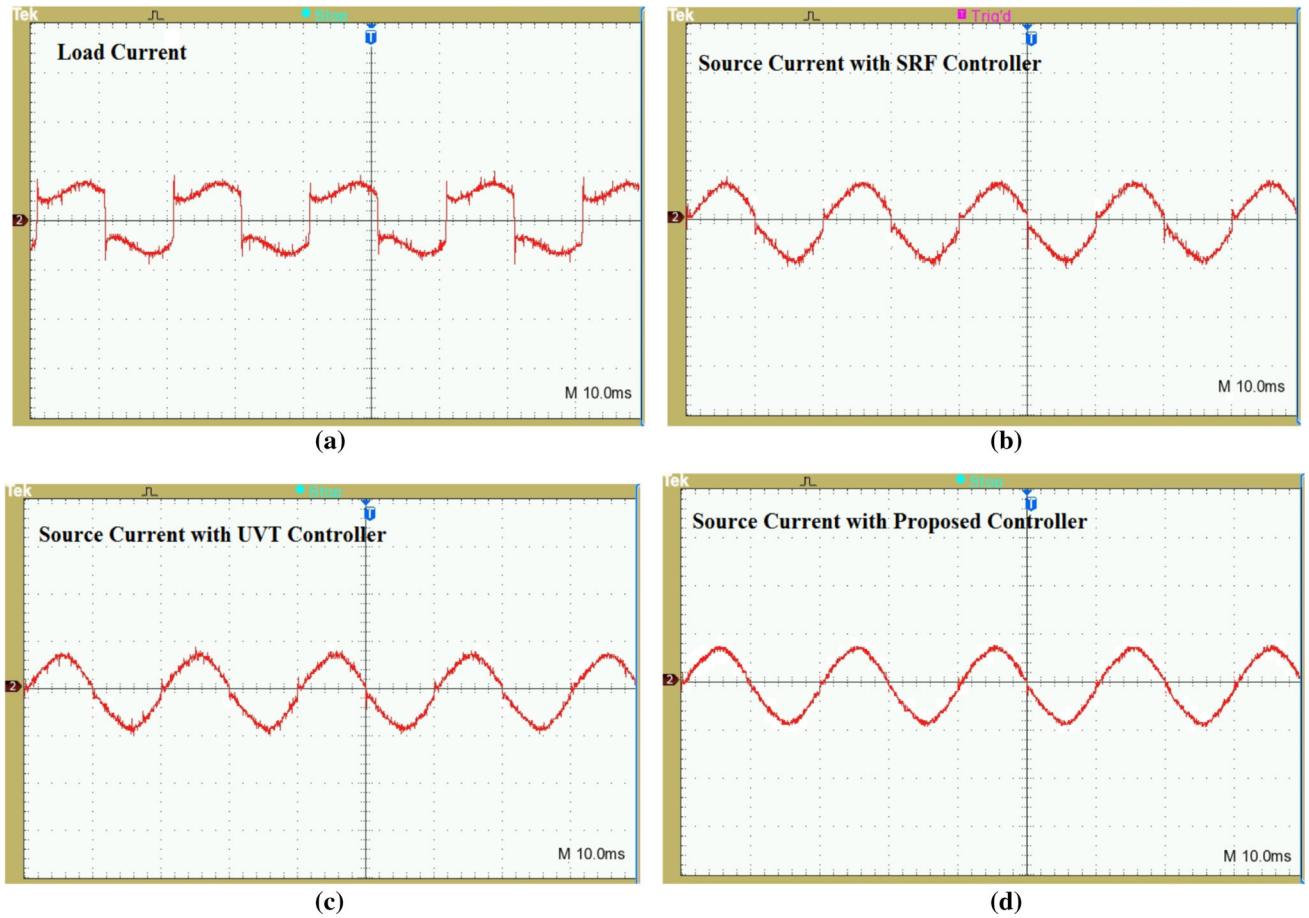


Fig. 16 Current harmonics compensation by PV-tied UPQC: **a** harmonic-rich load current, source current after compensation by (3A/div) **b** SRF controller (3A/div), **c** UVT controller (3A/div), **d** proposed controller (3A/div)

8 Conclusion

This paper presents a novel controller based on notch filter PLL, which eliminates multiple zero crossing, voltage and current quality issues under highly distorted grid and load condition. The presence of highly distorted grid voltages and currents, grid synchronization and proper compensation of power quality issues become more difficult with conventional PLL-based controller. Therefore, proposed novel controller based on notch filter PLL is implemented for the PV-1UPQC system to enhance the efficiency and performance. This paper has shown steps for evaluation of various design parameters of PV-1UPQC. Moreover, detailed design and stability analysis of notch filter-based PLL is discussed elaborately. The notch filter PLL-based controller is applied to PV-1UPQC system for compensation of power quality issues such as voltage sag, voltage swell, voltage harmonics and current harmonics. The effectiveness and efficiency of the proposed controller are validated by simulation as well as experimental studies with laboratory developed prototype. It is evident from the simulation and experimental model that PV-1UPQC system with proposed controller based on notch filter PLL efficiently compensate voltage sags, voltage swells, voltage harmonics and current harmonics under highly distorted grid and load conditions. Furthermore, results have been compared with conventional PLL-based SRF and UVT controllers and it is clearly revealed that proposed control methodology is more efficient for aforementioned grid conditions.

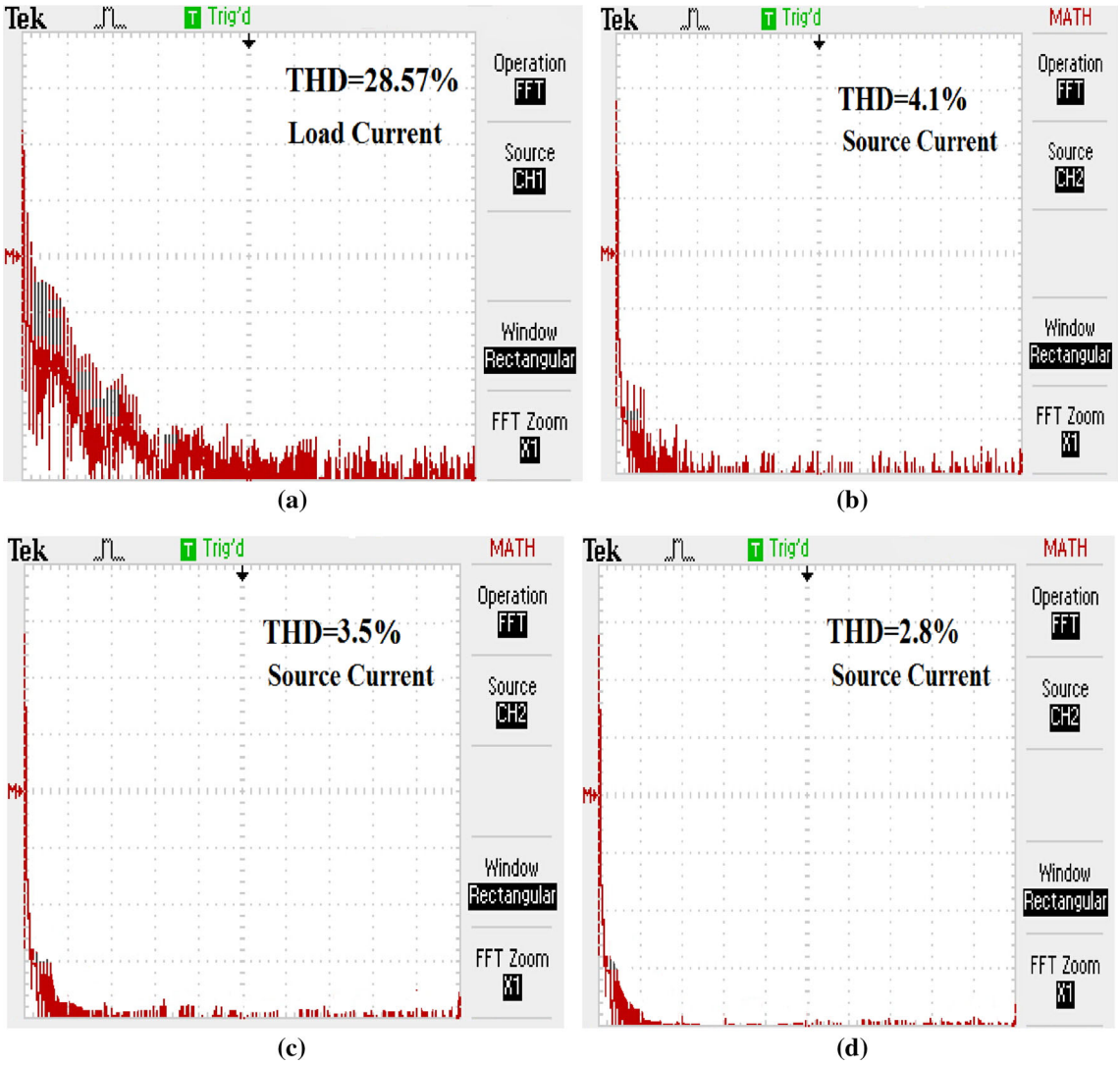


Fig. 17 FFT analysis: **a** harmonic-rich load current THD, **b** THD of source current after compensation by SRF controller, **c** THD of source current after compensation by UVT controller, **d** THD of source current after compensation by proposed controller

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