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ORIGINAL ARTICLE

State of the art design of adder modules: performance validation of GDI methodology for energy harvesting applications

Puli Raju[1] · Vallabhuni Vijay[1] · P. Ashok Babu[1] · P. Sridhar[2]

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Abstract Based on Gate Diffusion Input and Conventional Complementary Metal-Oxide Semiconductor logic, this study offers a full-swing high-speed hybrid Full Adder cell. The design was evaluated and compared to standard ten full adder designs for their key significance in real-time applications. The implementation uses the Cadence tool in the 18 nm FinFET module. The small size of MOSFETs (less than 28 nm nanometers) has caused specific operational issues in recent years, such as enhanced gate-oxide leakage, amplified junction leakage, strong sub-threshold conduction, and lowered output resistance. To solve the issues described above, FinFET offers the benefits of an increased operating speed, lower power consumption, and decreased static leakage current, which is utilized to realize most applications by replacing MOSFET. Considering the attractive characteristics of FinFETs, ten standard full adder cells have been designed and tested using FinFETs. The proposed design shows a significant improvement regarding speed and power delay products. The limitations of the proposed models are validated by increasing the adder cells to the maximum number of 64 bits.

Keywords CMOS logic styles · EDP · FinFET · Gate diffusion input (GDI) · Layout · PDP

1 Introduction

Due to the recent significant increase in portable digital devices, which require high-efficiency processing in confined silicon areas, the design of integrated circuits (ICs) with optimum performance characteristics has become critical (Yousefi et al. 2022; Gulafshan et al. 2022). Low operating frequency and low supply voltage are two methods for lowering IC power consumption. However, regularly lowering the supply voltage causes the driver current to drop and the circuit delay to rise (Hasan et al. 2021a). Therefore, using efficient circuit design techniques is crucial for improving the performance of digital circuits. In order to improve the performance of modern digital circuits, researchers have recently demonstrated much interest in energy-efficient design techniques with optimal speeds (Chu 2290).

Most processors and complex gate arrays use the adder as a fundamental element. Furthermore, the addition operation will occupy all the fundamental arithmetic operations. The analytical modeling of all the digital blocks relies on adder modules. Complex addition operations are developed with the help of the fundamental 1-bit adder module. The overall block performance depends on the individually developed core 1-bit adder module, which, intern results in the overall application's physical significance.

This article mainly focuses on the combination of conventional CMOS and GDI techniques. The full adder key

✉ Puli Raju
raju.p@iare.ac.in

Vallabhuni Vijay
vijaykalam@ieee.org

P. Ashok Babu
p.ashokbabu@iare.ac.in

P. Sridhar
sridhar@iare.ac.in

[1] Department of Electronics and Communication Engineering, Institute of Aeronautical Engineering, Dundigal, Hyderabad 500043, India

[2] Department of Electrical and Electronics Engineering, Institute of Aeronautical Engineering, Dudigal, Hyderabad 500043, India

Table 1 The truth table of the full adder operation

Inputs			Final outcomes and their realizations			
$Carry_{in}$	IN_1	IN_2	$Carry_{out}$	Realization	Sum	Realization
0	0	0	0	AND	0	XOR
	0	1	0		1	
	1	0	0		1	
	1	1	1		0	
1	0	0	0	OR	1	XNOR
	0	1	1		0	
	1	0	1		0	
	1	1	1		1	

The Sum is an XOR operation, and C_{out} is a AND operation when $C_{in}=0$.The Sum is an XNOR operation, C_{out} is an OR operation when $C_{in}=1$

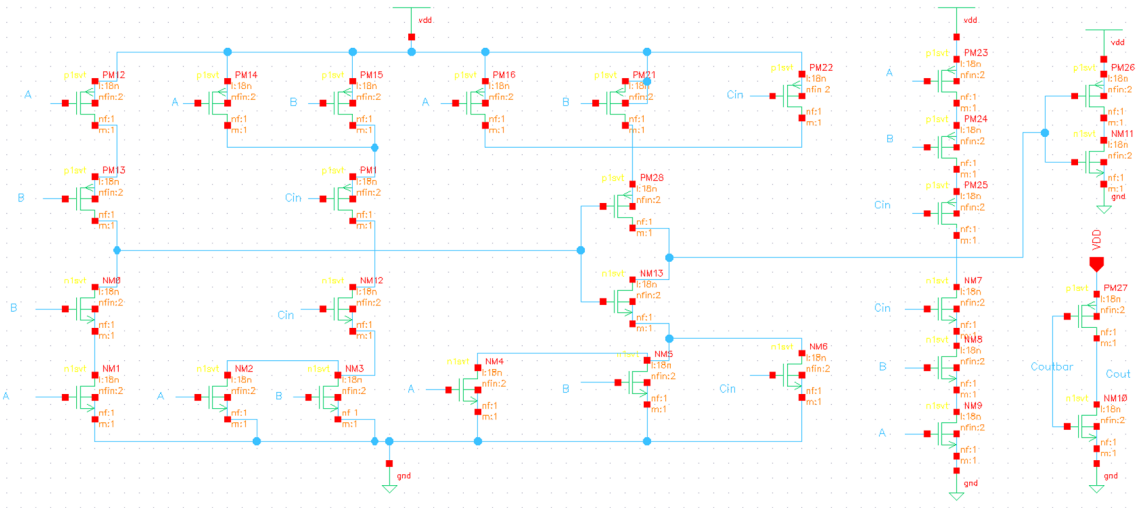


Fig. 1 Full adder given in (Mak 2022)

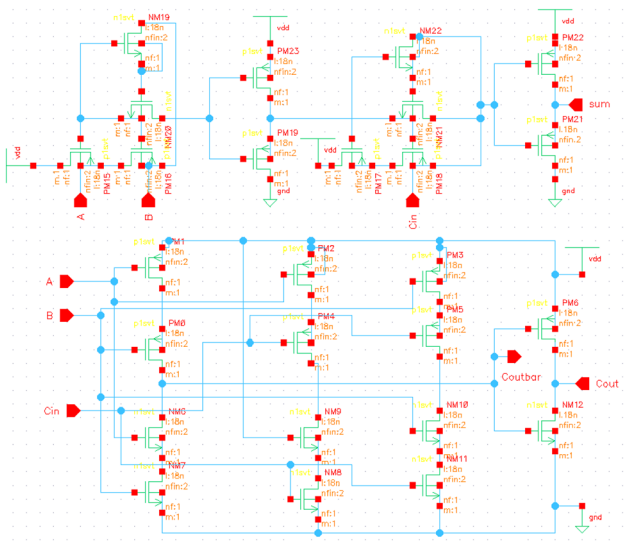
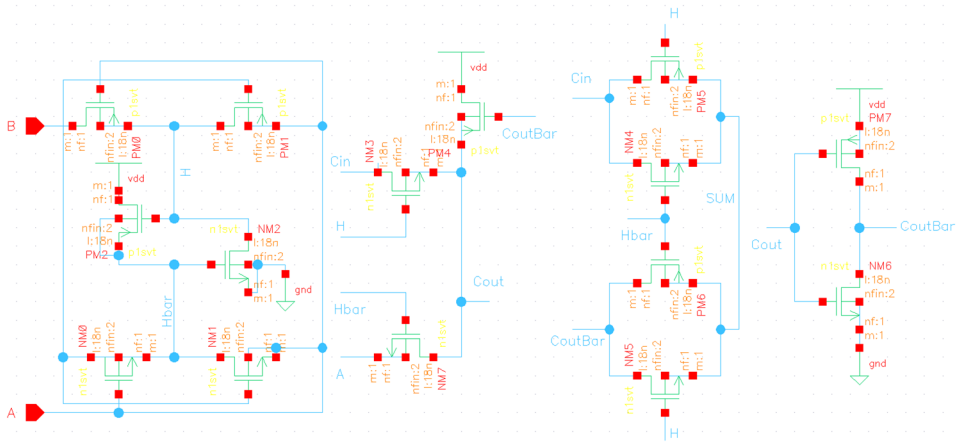


Fig. 2 Full adder given in (Velammal et al. 2021)

metrics contrasted with ten (10) other cutting-edge FAs to support it. The proposed full adders are optimized to a maximum of 32 bits incorporating a non-CLS approach for performance measurement in more extensive systems. Compared to FA cells currently in use, the proposed FA cell performed superbly (Bhattacharjee et al. 2021; Véstias et al. 2022; Kumar et al. 2021; Maleki et al. 2021).

2 Full adders design using FinFET nodes

The compact applications of the digital blocks are merely realized with the help of individual full adder modules. FA is divided into single logic and hybrid logic depending on the logic design method. The Complementary Path Transistor Logic (CPL) FA is said to be the earliest FA design (Roy et al. 2022).



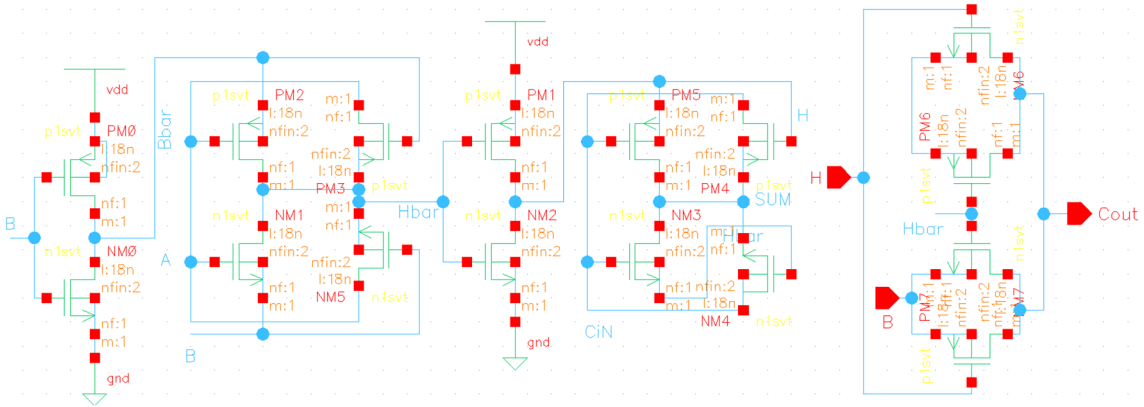


Fig. 3 Full adder given in (Rafiee et al. 2021)

Fig. 4 Full adder given in (Seyedi and Jafari Navimipour 2022)

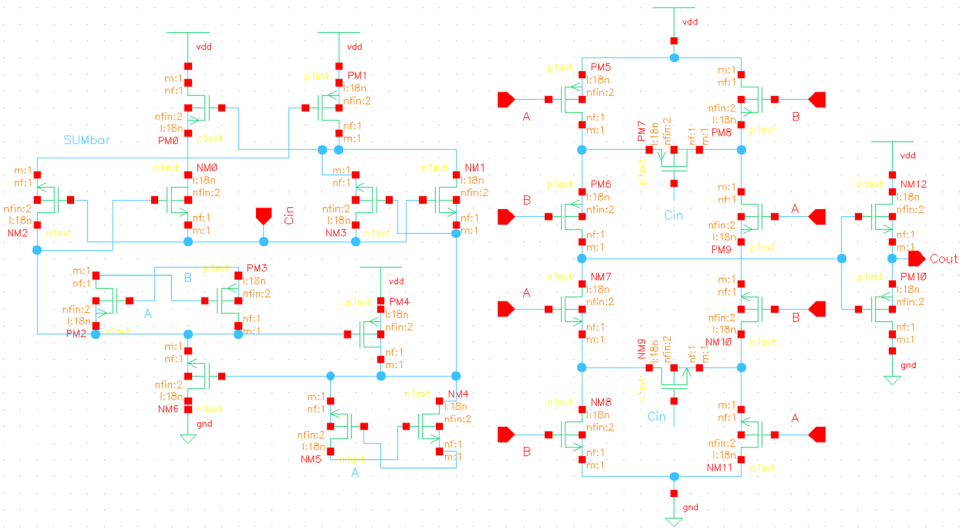


Fig. 5 Full adder given in (Fatemieh et al. 2021)

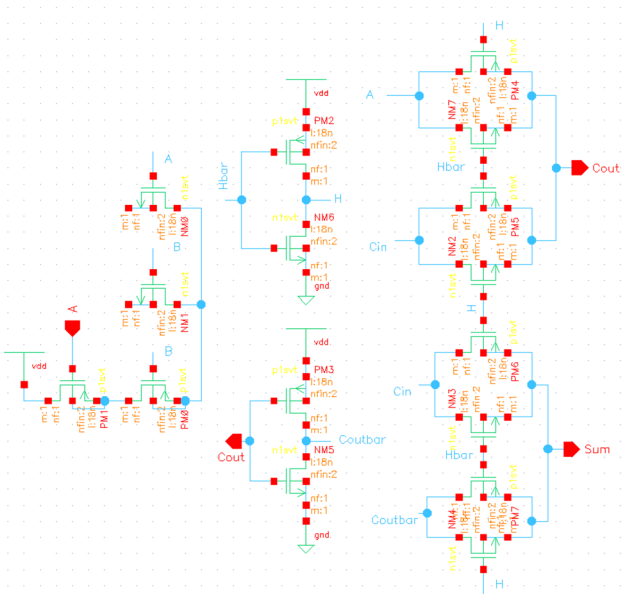


Fig. 6 Full adder given in (Krishnaveni et al. 2021)

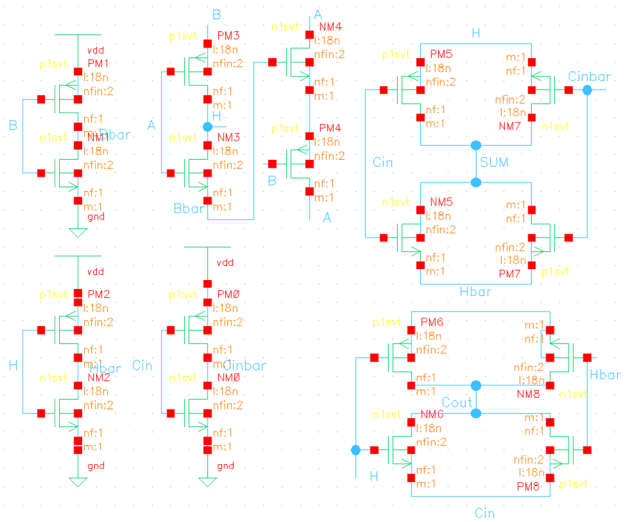


Fig. 7 Full adder given in (Soe et al. 2021)

The problem of voltage degradation severely hinders the use of CPLs in modern electrical circuits. Because of the primary advantages of the conventional CCMOS, most of the applications are being developed with the help of this technique. High power consumption, many transistors, and excessive input impedance are still issues. The CPL and CCMOS methodologies use one full adder style and topology for realization (Mak 2022; Sardroudi et al. 2021; Velammal et al. 2021; Rafiee et al. 2021; Seyedi and Jafari Navimipour 2022; Fatemieh et al. 2021; Krishnaveni, et al. 2021; Soe et al. 2021).

Recently, hybrid FA designs have attracted attention. Hybrid FA improves performance using many logic strategies within the same circuit (Sardroudi et al. 2021). FAs mentioned in Ultra-Low Power FA (ULPFA) (Velammal et al. 2021), Low-Power High Speed (LPHS) FA (Rafiee et al. 2021), and (Seyedi and Jafari Navimipour 2022; Fatemieh et al. 2021; Krishnaveni et al. 2021; Soe et al. 2021) are included in the hybrid domain. ULPFA uses Branch Based Logic (BBL) and Path Transistor Logic (PTL) to implement FA (Velammal et al. 2021). Stable and robust drive capability of the carry generation circuit. However, the summing circuit has no driving power. The same is true for Mirzaee et al. (Fatemieh et al. 2021). The LPHSFA of Rafiee et al. (2021) has a very low TC, making it suitable for applications requiring a small footprint and low power consumption (15 transistors). The LPHSFA of Rafiee et al. (2021) has a very low TC (15 transistors) and is suitable for systems that require a small area and low power consumption. The pass-transistor and transmission gate logic has been adopted in Soe et al. (2021). The issue of voltage degradation in CPL is minimized with the proposed design, whereas the driving capability enhancement is still a primary requirement. The design (Velammal et al. 2021) used three various levels of signal enhancements (Dhariwal et al. 2022; Raj et al. 2022; Naghizade and Saghaei 2021; Zareei et al. 2021; Hasan et al. 2021b; Arunkumar et al. 2022; Ravula et al. 2022; Mahmoud et al. 2021).

The full adder properties of the designs given in the literature of Chu (2290); Bhattacharjee et al. 2021; Véstias et al. 2022; Kumar et al. 2021) are much more similar. Using GDI technology, Shoba et al. (Soe et al. 2021) presented three different FA designs. These FAs have modified his GDI gates that allow the full-scale operation to address the voltage sag problem. By using fewer transistors, GDI technology also enables the creation of energy-efficient logic gates. The GDI method has a severe stress degradation flaw preventing widespread adoption. The design (Kumar et al. 2021) can be made with a minimum of 14 transistor counts, but this design has the limitation of a threshold level of voltage is a significant issue.

3 Proposed full adder design

Besides the limitations of the GDI technique, the methodology offers high demand for power efficiency and increased speed of designs. This article presented a hybrid and advanced to that conventional technique, which is achieved with the CCMOS and GDI. To reduce TC, this work uses logic gates with GDI-based inputs. The required power rails are fed from VDD and the *Gnd*, respectively,

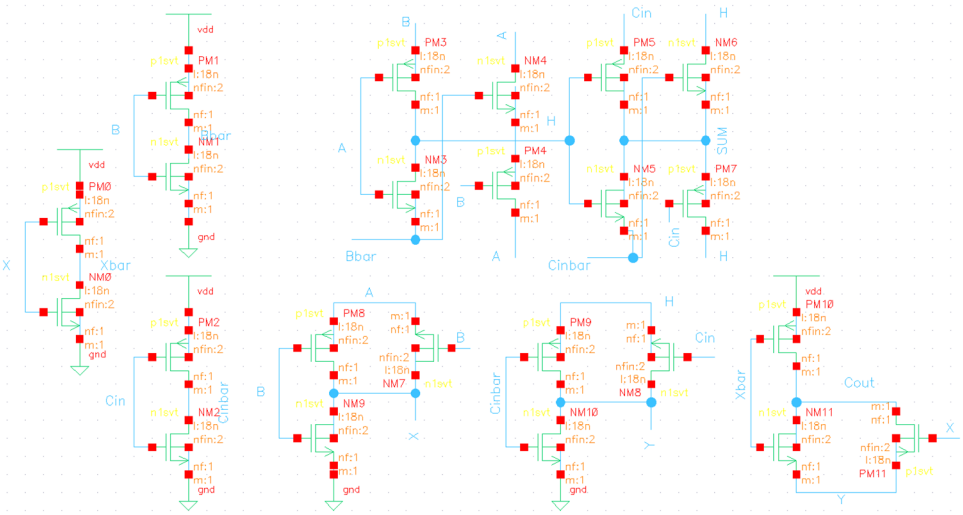


Fig. 8 Full adder given in (Soe et al. 2021)

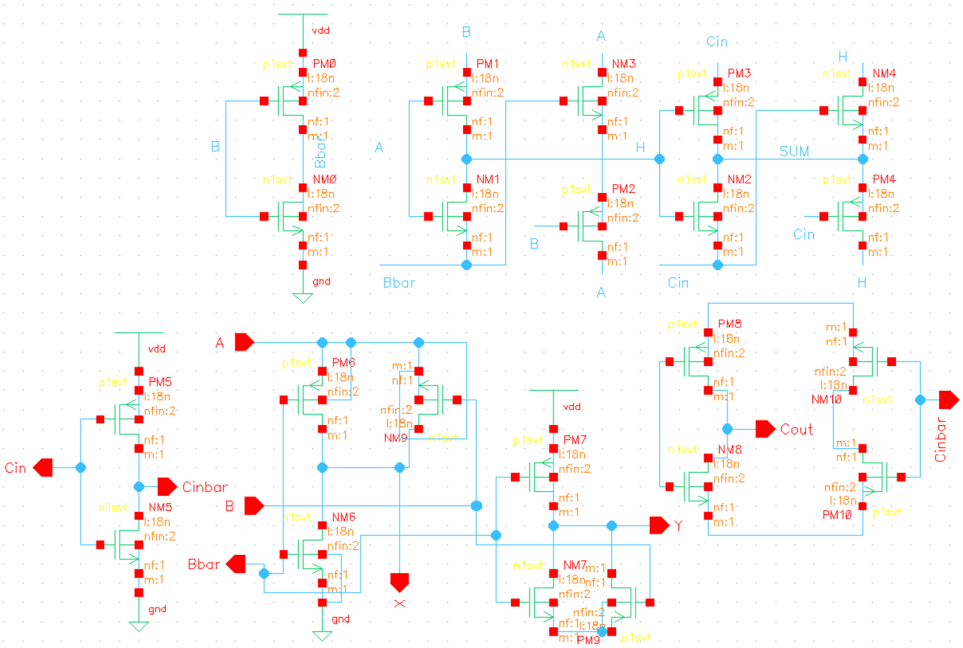


Fig. 9 Full adder given in (Soe et al. 2021)

from the CCMOS logic, which removes the limitation of the GDI methodology. The proposed FA modeling and critical specifications are presented in the following subsection.

3.1 Proposed adder cell logical modeling

The logical nature of the adder modules should be modeled first before its realization. Table 1 shows the FA truth table, which shows the FA adheres to the following requirements:

From this, it can be confirmed that the Sum is being generated from XOR–XNOR where, whereas C_{out} is developed with AND–OR logic.

3.2 Testbench setup

The testbench setup for the proposed models is given below in Figs. 1, 2. Using XNOR–XOR and NAND–NOR, the required adder blocks are realized in contrast to that of XOR–XNOR and AND–OR gates. GDI-based 2:1 multiplexers (MUX), NAND–NOR, and XNOR–XOR are cascaded to

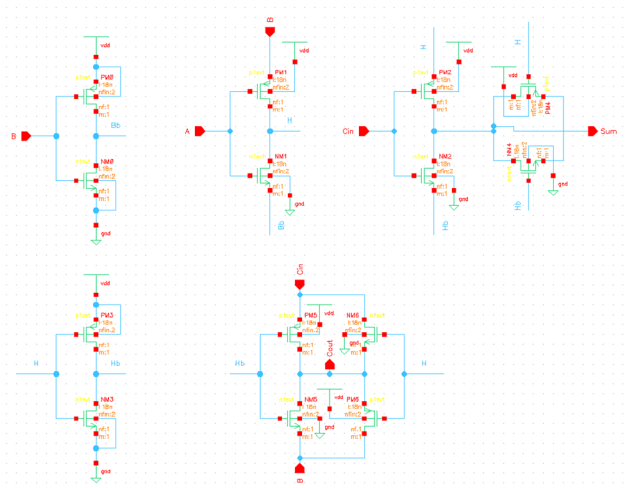


Fig. 10 Full adder given in (Dhariwal et al. 2022)

Table 2 Mathematical modeling of the GDI-based adder cells

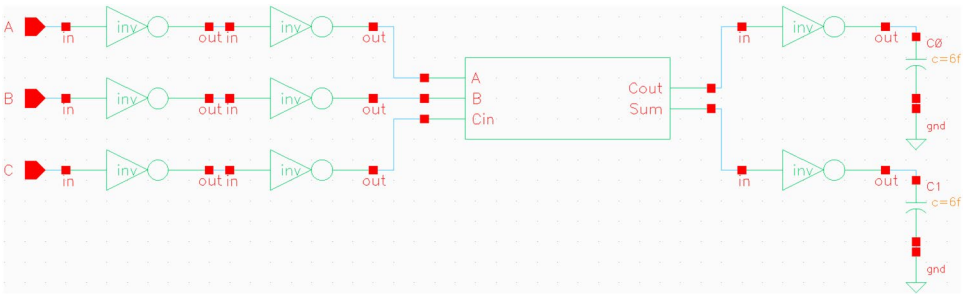
GDI module inputs			GDI module Output	Realization
G	P	Q		
$Carry_{in}$	IN_1	IN_2	$(IN_1IN_2)'$	2:1 Mux
IN_1	IN_2	IN_2'	$(IN_1+IN_2)'$	XOR
IN_1	IN_2'	IN_2	$IN_1IN_2+(IN_1IN_2)'$	XNOR
IN_1	IN_2'	GND	$IN_1IN_2'+IN_1'IN_2$	NOR
IN_1	V_{DD}	IN_2'	$Carry_{in}'IN_1+Carry_{in}IN_2$	NAND

route the desired signal to the output port, depending on Cin. Cout and Sum are the outputs of the GDI-based network (the complement of C_{out} and Sum). In the final phase, the signal sent by the GDI network is used by the CCMOS inverter to generate C_{out} and Sum.

3.3 XNOR–XOR and NAND–NOR gate design using GDI

From the literature, the GDI method has been taken to implement the standard multiplexers with the help of conventional AND–OR logic. Figures 3, 4, 5, 6, 7, 8, 9, 10 shows the layout of a simple GDI cell. The P-channel CMOS (P-MOS) and N-channel CMOS source and drain terminals of the primary GDI cell are the same as the source and drain terminals of a CCMOS-based NOT gate, but the signal sent to these terminals works differently (NMOS). The connections of the power supply rails of V_{DD} and *Gnd* are made across the inverter source and drain. The GDI cell input is the common point of the drain-source nodes. The required adder implementation using GDI methodology uses the available standard modules of XNOR, XOR, NAND, and NOR blocks (Table 2).

Fig. 11 Simulation test bench structure



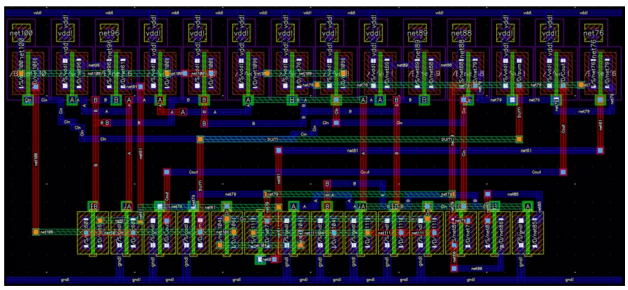


Fig. 12 Layout of the full adder shown in Fig. 1

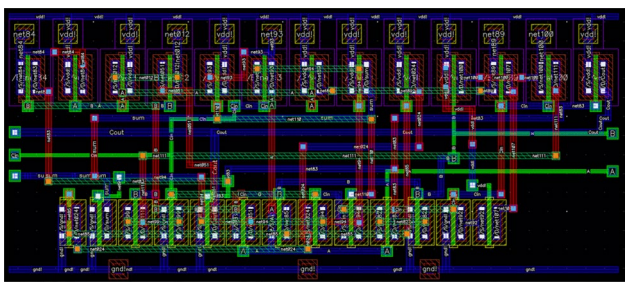


Fig. 13 Layout of the full adder shown in Fig. 2

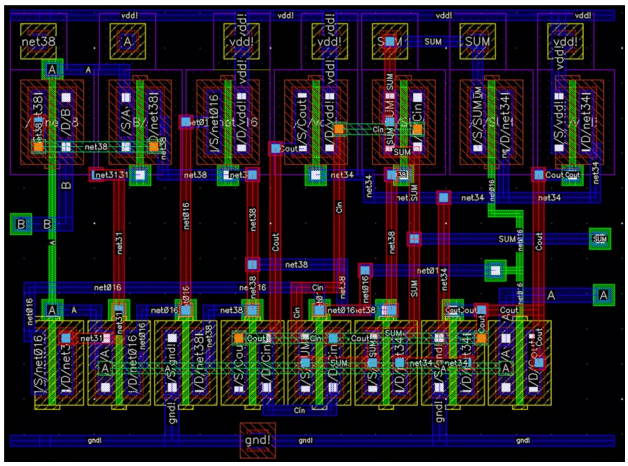


Fig. 14 Layout of the full adder shown in Fig. 3

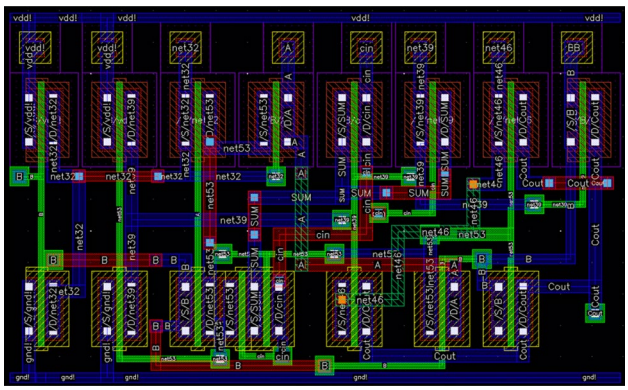


Fig. 15 Layout of the full adder shown in Fig. 4

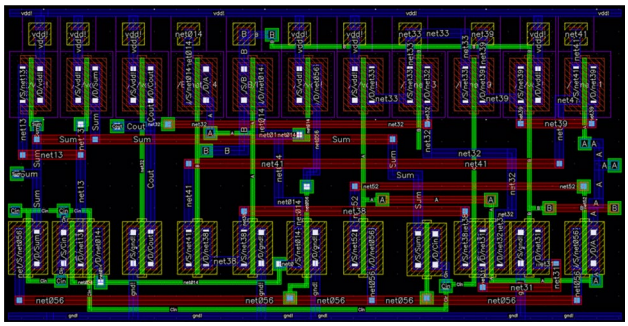


Fig. 16 Layout of the full adder shown in Fig. 5

4 Validation of the proposed adder cells using pre-layout and post-layout simulations

The proposed circuits are developed using the Cadence tool with 18 nm FinFET spectre models. Firstly, all the circuits are designed using Cadence Virtuoso using FinFET

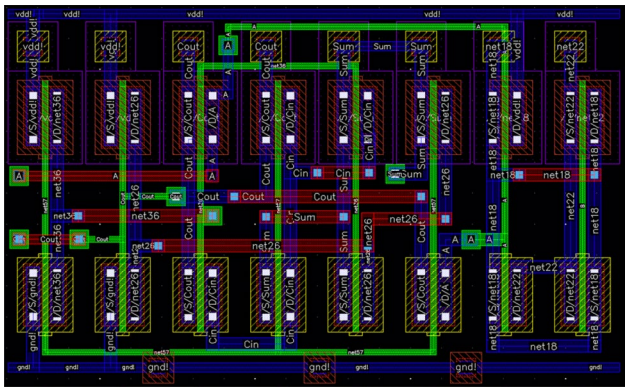


Fig. 17 Layout of the full adder shown in Fig. 6

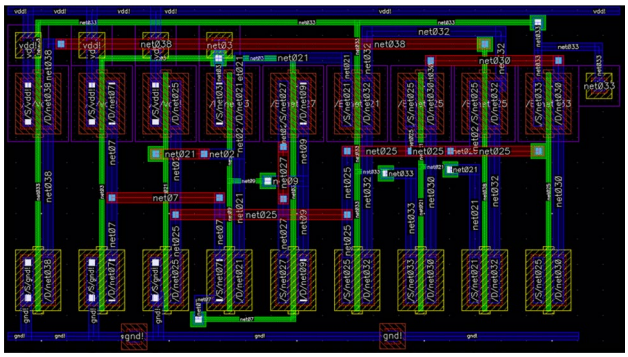


Fig. 18 Layout of the full adder shown in Fig. 7

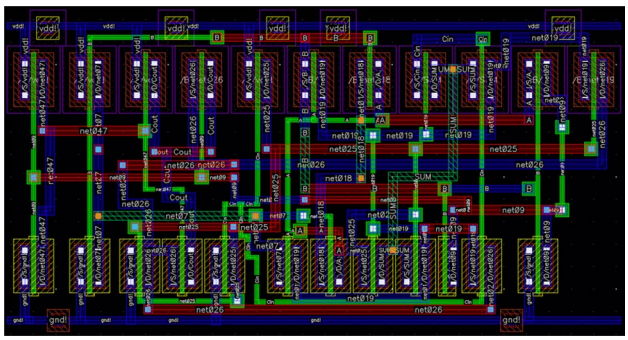


Fig. 19 Layout of the full adder shown in Fig. 8

nodes to meet the desired functionality. The desired outputs of the circuits at their corresponding nodes are being validated using transient responses. Later, the circuits are verified for the required frequency of working using AC analysis. Secondly, by conducting Montecarlo analysis, pre-layout simulations, and performance metrics are taken for all the circuits with the testbench setup shown in Fig. 11.

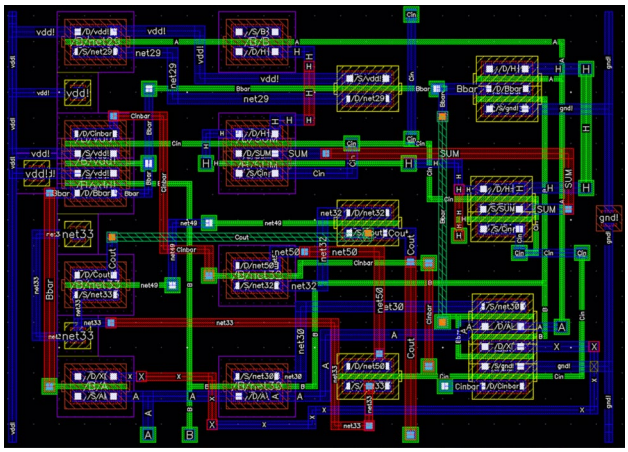


Fig. 20 Layout of the full adder shown in Fig. 9

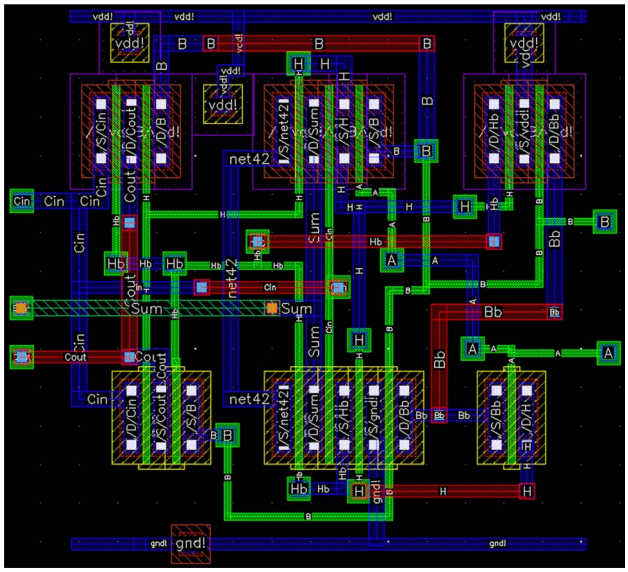


Fig. 21 Layout of the full adder shown in Fig. 10

Buffer cells are added to the input ports in the actual test bench setup given in Fig. 11 for performing functionality checking. The parasitic resistance and capacitances are induced in the input terminals provided by the real-time usage of integrated circuits' interconnects and externally joined peripherals. Because of this phenomenon, the circuit exhibits distortions in the signal as well as they do cause a delay in the signals. In turn, the test bench for performing the simulation should have the input buffers to depict the real-time circuit performance. The amount of distortion that should be added to the circuit undergoing validation is at a

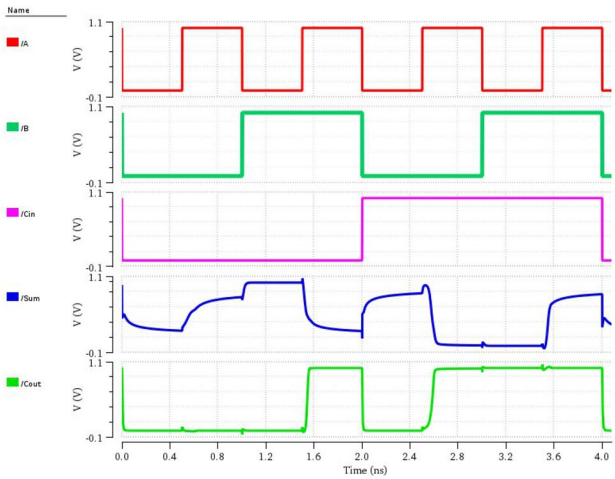


Fig. 22 Transient Response of the Designed full adders for the supply voltage $V_{DD} = 1$ V

minimum level almost equal to that practical occurrence in the deployment stages. In the same fashion, the testbench is connected with output inverters and followed by the capacitors with the utmost minimum level of 6 fF, leading to the form of the actual loads to the design.

The designs are simulated to measure their salient features with power dissipation, speed, power delay product (PDP), and energy-delay product (EDP). Moreover, these metrics were tabulated to evaluate one's meritorious advantages and limitations. The supply voltage varies from the minimum to maximum operating voltage of FinFET nodes. At every potential and by considering each test case of the cells, the designs have given different delay and power dissipation values from which the circuit's total power dissipation has been measured. These power dissipation values at each V_{DD} value are taken, and with the mathematical expression of average power given in Table 3, the designed circuit's total power dissipation has been calculated. The prominent issue of leakage power of conventional MOS transistors at lower technology levels is being avoided, and the optimum performance levels are observed with the FinFET nodes of the designs by mitigating leakage power issues. The dynamic power occupies a significant portion of the overall power dissipation value. Specifically, the leakage power is developed at circuit nodes because of non-application of input test cases leads to an idle state of the circuit, and at this level, circuit power usage is treated as leakage power and, in other terms, named static power. The leakage power is measured by observing the designed Full adder cells' power at the stand-still level. Among all the measured values of delay

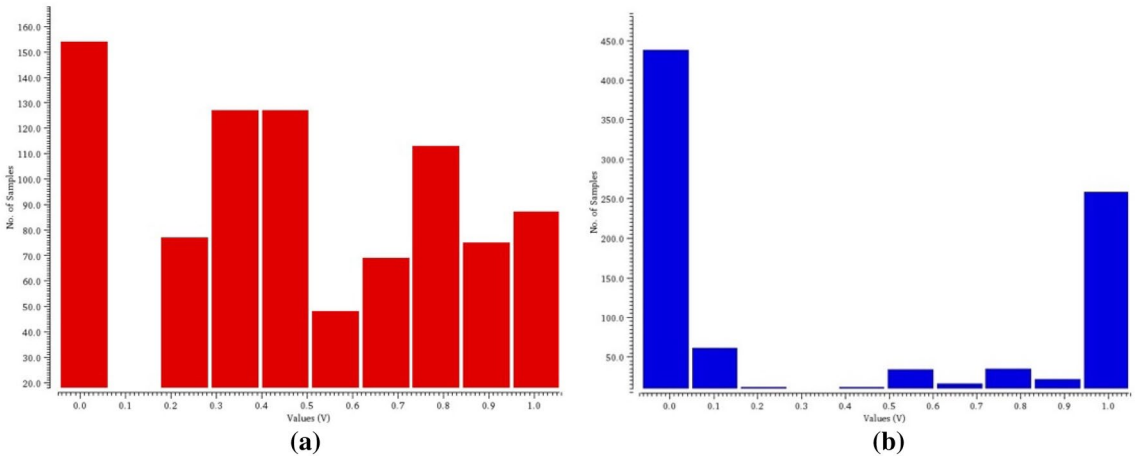


Fig. 23 Montecarlo analysis of the designed full adders sum and carry outputs

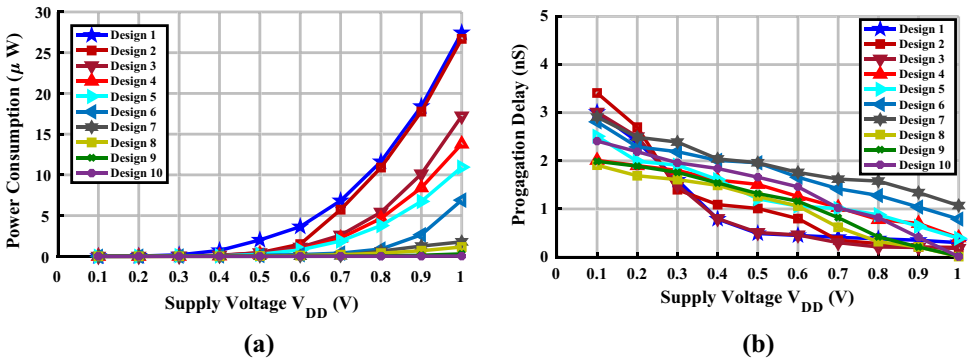


Fig. 24 Vdd vs. Power consumption and propagation delay

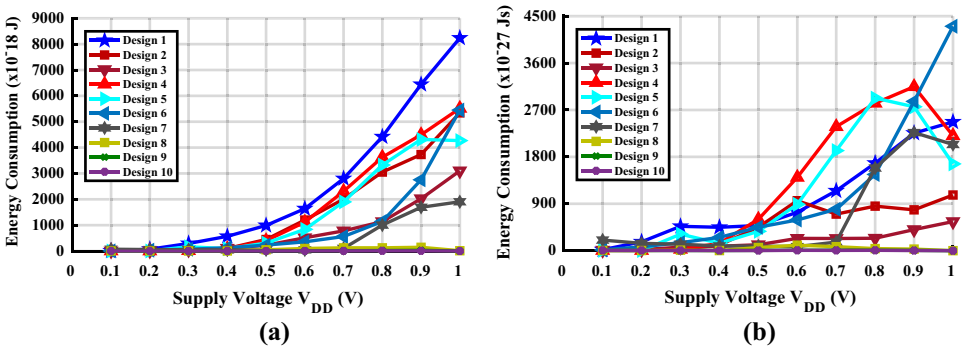


Fig. 25 V_{DD} vs. PDP and EDP

metrics, the delay with the highest value is taken as the final delay of the critical path of the design. In this manuscript, the delay metric is calculated at half of the overall applied V_{DD} values of input and output responses.

The optimized layouts of the proposed circuits constructed in Cadence has given in Figs. 12, 13, 14, 15, 16, 17, 18, 19, 20, 21. The layouts are carried out using FinFET 15 nm technology. The proposed FA cells layouts LVS has matched and the RC extraction files are being added to the test bench to take post-layout results.

RC extracted file is being added to the test bench given in Fig. 11. The post-layout results are measured by varying the supply voltage from 0.1 to 1 V of V_{DD}.

The sample response of the transient analysis of the proposed FinFET-based FA cell at $V_{DD} = 1$ V for all the input test cases is given in Fig. 22.

Table 3 Validation of the proposed full adder designs at $V_{DD} = 1$ V

References	Transistor Count	Average Power (uW)	Leakage power (nW)	% of Leakage power with respect to avg. power	Propagation Delay (ps)	PDP (aJ)	Area (um^2)
Roy et al. 2022)	26	1.32	41.32	3.123	60.5	76.23	11.14
Mak 2022)	24	1.54	45.34	3.134	78.4	112.15	11.15
Sardroudi et al. 2021)	16	0.87	27.34	3.453	85.2	78.2	7.67
Sardroudi et al. 2021)	16	0.64	16.45	2.123	99.2	60.23	7.78
Velammal et al. 2021)	22	1.17	17.89	3.093	64.2	72.4	8.98
Velammal et al. 2021)	14	0.79	36.23	3.763	52.4	33.12	7.62
Rafiee et al. 2021)	16	1.03	20.23	3.243	45.4	36.37	7.92
Seyedi and Jafari Navimipour 2022)	20	0.99	21.34	3.673	52.5	48.62	7.92
Fatemieh et al. 2021)	20	0.92	25.34	3.893	53.7	55.34	8.02
Krishnaveni et al. 2021)	16	0.73	24.43	3.593	59.2	42.58	7.01

To raise the actual voltage levels at the corresponding output levels for both Sum and Carry, the outputs of the designs are validated using Montecarlo analysis. The same Response is presented in Fig. 23.

The variation of delay, power consumption, PDP, and EDP values are given in Figs. 24 and 25 for all ten cells.

4.1 The standard cell representation of the full adder module

Table 3 gives the experimental findings of the proposed circuits at a supply voltage of 1 V. Further simulations were run with the supply voltage varied between 0.6 and 1 V for a more thorough performance examination. The findings are displayed in Figs. 22, 23, 24, 25. All the proposed circuits are tested with the help of a test bench setup. The salient features of propagation delay, power consumption, power delay products, and energy-delay product have been calculated for all the proposed designs in addition to the variation of these three critical parameters at different supply voltages.

Dynamic power is the amount consumed during the transition of signals from one to the other switching state. Besides, the leakage power is always focused on the involvement of a total number of transistors, but for the adopted designs, the leakage power is related to the other second-order effects too. From the given simulation results, it can be visualized that different adders with varied transistors have their unique performance metrics, and the power and delay constraints are too separate. Based on the number of internal nodes and active paths of signal routing, decide the required adder cell with the optimized performance factor.

5 Conclusion

This study describes a hybrid FA cell with good performance properties based on GDI and CCMOS circuitry. Ten different designs were compared to the recommended adder's design in an 18 nm spectre model of FinFET. The test bench adjustment for validation of the designed full adders is considered to meet the required specifications. The proposed designs are all tested individually and combined concerning the testbench results in improved performance of the designed circuits. Concerns about voltage degradation and the constrained driving capabilities of the GDI gates were also allayed by the addition of CCMOS logic-based inverters. Based on the elevated features of the designs, moreover scalability for application in a broader range of adders, the recommended FA design is a perfect replacement for the object of calculating units in existing ultra-large-scale computing systems.

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Declarations

Conflict of interest All authors certify that they have no affiliations with or involvement in any organization or entity with any financial interest or non-financial interest in the subject matter or materials discussed in this manuscript.

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References

Arunkumar K et al 2022. Design of high speed, low power 16x16 vedic multiplier with adiabatic logic. In: 2022 8th International conference on smart structures and systems (ICSSS), p 1–9. IEEE

Bhattacharjee S et al (2021). Design and simulation of a small power two-bit mc circuit via full adder logic. In: Journal of physics: conference series, vol 1962, no 1, p 012029. IOP Publishing

Chu S (2022) Comparative analysis of optimization schemes of carry look-ahead adder. In: Journal of physics: conference series, vol 2290, no 1, p 012008. IOP Publishing

Dhariwal S et al (2022) Hybrid GDI ptl full adder: a proposed design for low power applications. Int J Perform Eng 18(1):1–22

Fatemieh SE et al (2021) LAHAF: Low-power, area-efficient, and high-performance approximate full adder based on static CMOS. Sustain Comput: Informa Syst 30:100529

Gulafshan G et al (2022) Fast and area efficient hybrid MTJ-CMOS spintronic approximate adder. TechRxiv. https://doi.org/10.36227/techrxiv.19316669.v1

Hasan M et al (2021a) Comprehensive study of 1-Bit full adder cells: review, performance comparison and scalability analysis. SN Appl Sci 3(6):1–15

Hasan M et al (2021b) A scalable high-speed hybrid 1-bit full adder design using XOR–XNOR module. Int J Cir the App 49(11):3597–3606

Krishnaveni D et al (2021) Reversible fade gate as decoder, encoder and full adder. Advances in automation, signal processing, instrumentation, and control. Springer, Singapore, pp 1323–1331

Kumar MS et al (2021) A novel ultra-low power 7T full adder design using mixed logic. In: Journal of physics: conference series vol 1804, no 1, p 012186. IOP Publishing

Mahmoud A, Vanderveken F, Ciubotaru F, Adelmann C, Cotofana S, Hamdioui S (2021) Spin wave based full adder. In: 2021 IEEE international symposium on circuits and systems (ISCAS), p 1–5. IEEE

Mak KY et al (2022) Single-bit full adder and logic gate based on synthetic antiferromagnetic bilayer skyrmions. Rare Met. https://doi.org/10.1007/s12598-022-01981-8

Maleki MJ et al (2021) Design and analysis of a new compact all-optical full-adder based on photonic crystals. Optik 227:166107

Naghizade S, Saghaei H (2021) A novel design of all-optical full-adder using nonlinear X-shaped photonic crystal resonators. Opt Quant Electron 53(3):1–13

Rafiee M et al (2021) An efficient multiplier by pass transistor logic partial product and a modified hybrid full adder for image processing applications. Microelectron J 118:105287

Raj S et al (2022) Hybrid approximate adders using pass transistor logic and transmission gate. Advanced computational paradigms and hybrid intelligent computing. Springer, Singapore, pp 273–284

Ravula MR et al 2022 Designing carry look ahead adder to enrich performance using one bit hybrid full adder. In: 2022 International conference on electronics and renewable systems (ICEARS), p 86–89. IEEE

Roy R et al (2022) Design of an efficient multilayer hybrid reversible spintronic ripple carry adder using quantum cellular automata technique. IETE J Research. https://doi.org/10.1080/03772063.2022.2027277

Sardroudi FM et al (2021) A low-power dynamic ternary full adder using carbon nanotube field-effect transistors. AEU-Int J Ele Comm 131:153600

Seyedi S, Jafari Navimipour N (2022) Designing a multi-layer full-adder using a new three-input majority gate based on quantum computing. Concurr Comput: Pract Exp 34(4):e6653

Soe WH et al (2021) A single-molecule digital full adder. J Phys Chem Lett 12(35):8528–8532

Velammal MN et al (2021). Design of high-speed nanoscale adder logic circuit for low power consumption. In: 2021 IEEE pune section international conference (PuneCon), p 1–6. IEEE

Véstias M et al (2022) Efficient design of low bitwidth convolutional neural networks on FPGA with optimized dot product units. ACM Tran Reco Tech Sys (TRETS) 16(1):1–36

Yousefi M et al (2022) Design and simulation of pseudo ternary adder based on CNTFET. AUT J Ele Eng 54(2):4–4

Zareei Z et al (2021) Design of efficient approximate 1-bit Full Adder cells using CNFET technology applicable in motion detector systems. Mic J 108:104962