



# Distribution system power quality compensation using a HSeAPF based on SRF and SMC features

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**Abstract** The purpose of this paper is to describe the design of a Hybrid Series Active Power Filter (HSeAPF) system to improve the quality of power on three-phase power distribution grids. The system controls are comprised of Pulse Width Modulation (PWM) based on the Synchronous Reference Frame (SRF) theory, and supported by Phase Locked Loop (PLL) for generating the switching pulses to control a Voltage Source Converter (VSC). The DC link voltage is controlled by Non-Linear Sliding Mode Control (SMC) for faster response and to ensure that it is maintained at a constant value. When this voltage is compared with Proportional Integral (PI), then the improvements made can be shown. The function of HSeAPF control is to eliminate voltage fluctuations, voltage swell/sag, and prevent voltage/current harmonics are produced by both non-linear loads and small inverters connected to the distribution network. A digital Phase Locked Loop that generates frequencies and an oscillating phase-locked output signal controls the voltage. The results from the simulation indicate that the HSeAPF can effectively suppress the dynamic and harmonic reactive power compensation system. Also, the distribution network has a low Total Harmonic Distortion (< 5%), demonstrating that

the designed system is efficient, which is an essential requirement when it comes to the IEEE-519 and IEC 61,000–3-6 standards.

**Keywords** Active Power Filter (APF) · Phase Locked Loop (PLL) · Synchronous Reference Frame (SRF) · Sliding Mode Control (SMC) · Voltage Harmonics

## 1 Introduction

As more power technology is implemented globally, there is an increasing number of power system quality issues. Current and voltage harmonics have a negative impact on power production efficiency, transmission, and utilization. An Active Power Filter (APF) is a power electronic device that produces and injects a compensation current and/or voltage into the power grid to help mitigate power quality issues. Improving the quality of power will help reduce the cost of distributing power to the supplier, and therefore, the consumer, it will help reduce the cost of operations. Improving power quality can be achieved by either an active or passive power filter (Altawil et al. 2012). Active Power Filters (APFs) inject controlled amounts of currents or voltages using power electronic converters to counter the effects of electric network harmonics (Narayan and Lakshminarayana 2018; Altawil et al. 2012; Golestan et al. 2020).

With the advancement in the development of APFs, the application of these devices in compensation applications has increased. APFs can also be utilized in compensating harmonic dumping or supply voltages between different networks of power distribution. APF provides advanced custom solutions for issues related to power quality, particularly voltage and current disturbances. In previous studies (Altawil et al. 2012; Al-Masri et al. 2019; Narayan

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and Lakshminarayana 2018), this power condition has been used for compensation of either current harmonics with Shunt APF (ShAPF)/ DSTATCOM, voltage swell/sag with Dynamic Voltage Restorer (DVR) or improve power quality (both current and voltage) by use of a Unified Power Quality Conditioner (UPQC). Other studies (Altawil et al. 2012; Smadi et al. 2019; Emin et al. 2013) have also reported the use of ShAPF to alleviate current quality problems. ShAPF is limited to only solving the issue of quality with the current, whereas and the latter controller can solve all problems related to power quality, it has several drawbacks due to its size and complexity of control. In the current work, a solution has been proposed to overcome power quality issues related to both current and voltage, where a series active power filter has been used to mitigate harmonics and voltage swell/sag. In contrast, harmonic currents are improved by using a passive filter.

### 1.1 Literature review

Previous research works there are some the researchers in this field are summarized as follows:

The problem is an intuitive fractional-order fuzzy controller for a three-phase (APF) is constructed that utilizes a backstepping and variable structure controller to correct active power and normalize the DC voltage. To address the solution of a variable fuzzy controller is proposed to better estimate the unidentified period in the controller, and in order to compensate for a proportional sliding mode surface. You can make changes to the parameters of this problem while live. Also, a variable fuzzy controller is proposed, and the system that utilizes a fractional-order sliding mode surface for addressing the problem of THD is also contrasted. The methodology will be applied in the study for it will direct the investigation in contrast to conventional integer-order sliding surface control strategies, a dynamic sliding-mode fuzzy logic controller, along with a backstepping control strategy, which utilizes conventional integer-order sliding surface control strategies that have been extended for use in the APF design. And the last one is: This system identifies and configures the parameters using an intuitive control strategy and a fuzzy controller while concurrently tracking the unidentified nonlinear period. The study used the proposed algorithm use the In SimPower Toolbox / MATLAB, a virtual controller fractional backstepping sliding mode control (FBSMC) is used to achieve the results. The final results for the THD values are 24.71%, 1.5%, 1.39%, and 1.83% between the proposed fractional back stepping sliding mode adaptive fuzzy controller, and 24.71%, 2.33%, 2.30%, and 2.37% for the said controller with integer-order (Fei et al. 2019).

The problem is UPQC dc link voltage controlled with non-linear sliding (NLS) for sag/swell, current harmonics,

and voltage unbalance compensation. To address the solution of the variable damping ratio is more desirable for eliminating the nonlinear term's problem on the closed-loop system, as the output moves closer to the desired reference position. Improved dc link voltage control from a faster response and lower overshoot thanks to UPQC. The study used the proposed algorithm use the Real-time performance analysis was conducted at Opal-RT Lab's laboratory using Opal-RT Lab's systems. To gain more insight into the methodology, the study will implement a non-linear sliding surface, which is reliant on varying the DC link power flow. The final results at the end of the day, the results showed that the NLS controller's results were closer to reality than those of the controllers proposed by other groups. THD and PI of the NLS Controller is 4.28% and 3.37%. The NLS-Controller is rated at 9.89 kW, and the PI-Controller is rated at 9.25 kW. Reactive power is utilized in the NLS-Controller 16VAR, and PI-Controller 44VAR (Patjoshi and Mahapatra 2014).

The problem is assessing the using a power conditioner combined with non-linear power quality control helped overcome the problem of linear (UPQC). This controller is built with a sliding mode control, with both active and reactive power theories, and interactive use in mind. A UPQC a APF in shunt and one in series together as part of a common dc link capacitor that was connected to all the systems in the facility. To address the solution of the (1) deliver a fast response time, (2) plus full compensation for voltage sags and swells, (3) outstanding performance in a power system that is prone to voltage fluctuations (4) Optimal performance in the face of inconsistent networks. The study used the proposed algorithm use the UPQC simulation was performed in MATLAB software, and the sliding mode controller was used SMC. The methodology will be applied in the study for to connect Combination of instantaneous active and reactive power and SMC theories. A non-linear controller's capability was proven through simulation in the MATLAB toolbox, and the results from the conventional PI controller were used to compare the controller's performance. The final results compensated PI controllers make the system 25.96 percent compensated; SMC controllers, however, only add up to 2.44 percent. A comparative study looks at the voltage and current THD of the network and the uncompensated (UN) network, where the PI controller is applied, and the uncompensated UN network, where the sliding controller is used. A THD of 11.38% is associated with uncompensated voltage and current, while a THD of 29.12% is attributed to compensated voltage and current. 3.73% with the sliding controller, as opposed to 3.73% with the fixed controller, has a combined deviation of 3.68%, whereas 3.53% overall deviation. The product has been developed to withstand unbalance operating systems. About 11% of the

uncompensated network's unbalances are out of balance, while 9% of the compensated network's unbalances are out of balance (Mojtaba et al. 2018).

The problem is assessing the lack of a balanced current and the power system causes a high-performance optimization technique to be needed for a Multifunctional grid-tied inverter (MFGTI). To address the solution of the harmonic, reactive, and negative sequence current element in the Positive Fundamental Components Estimator (PFCE) estimator can be used to estimate those three components. This is an open-loop algorithm with little computational power required PFCE. Thus, appropriate robustness is obtained while keeping computational overhead at a minimum. The study used the proposed algorithm use the MFGTI control system is designed using the instantaneous power theory concept. Redesigned bus controller built on variable mode concept as a methodology PFCE the SMC is useful because of its good dynamic productivity and tolerance to fluctuation in input variables. The PFCE's implementation of the system is capable of delivering active power, canceling harmonics, generating reactive power, and ensuring the overall system is balanced under non-ideal main voltage conditions. The final results will illustrate that (1)—the (MFGTI) results in correction for current and spectra in the normal operating conditions THD. Prior to adjustment, they were 19.7% for the primary current and spectrum, as well as 18.4% for the THD. Before compensating the THD, the results were: 19.7% for the primary current and spectrum, as well as 18.4% for the spectrum and primary current THD. Before compensation, experimental results show a primary current and spectrum value of 18.2% THD, which are consistent with measurements using a passive filter, an SMC, and a THD of 8.4%. PFCE, PI, and a THD of 3.6% were additionally measured using the same techniques. The preliminary results obtained under an unstable main voltage: unstable primary current: It is found that the primary current and spectrum both use the LSCN, LPF, and SMC when under unstable main voltage is applied. Under unstable main voltage (the condition found in experiments conducted under that condition) the experimental results demonstrate that the primary current and spectrum both use LSCN, LPF, and SMC. (Safa et al. 2018).

The problem is assessing the document introduces an innovative method based on diffusion slip pulse width modulation (FSMPWM) and (SEHAPF) to generate control signals for THD reduction. To address the solution of the reactive power is adjusted by using hybrid filters on the transmission line to curtail harmonic distortion and reduce their variance when the load or power source fluctuates. To accomplish this, the methodology study has developed a power factor and a power factor neutral system. FSMPWM is implemented using a Mamdani fuzzy rule that triggers

fixed pulses, the proposed method reduces the noise vibration response by controlling the narrow insulating coat between the sliding surface. The research employed the proposed algorithm for FSMPWM Control of SEHAPF. The final results the conclusion states that the THD % assessment of the primary current used in SEHAPF compared to HCC or FSMPWM produced better results. We have three sections to measure the THD for load voltages: between FSMPWM and HCC. This implementation of SEHAPF the THD without SEHAPF the THD has a THD of 35.06 percent, HCC the THD has a THD of 4.60 percent, and FSMPWM the THD has a THD of 2.36 percent. Without SEHAPF, the THD is 35.08%, HCC is 4.83%, and FSMPWM is 2.46%. Third, the THD without SEHAPF is 35.11%, HCC is 4.56%, and FSMPWM is 2.39% (Das et al. 2018).

The problem is assessing the output lag pulse frequency fluctuation in a hybridized an inductor-capacitor (LC) - coupling (HAPF). The LC Oscillator's increase in resistance, which represents the series current ratio, affects the current non-linearity of the inverter, and produces unpredictable short duration pulse to switchable power semiconductor drivers. To address the solution of the leads to reduced system efficiency. The first step will be to conduct an analysis of the output lag control of the HAPF to see it is contrast to a linearized one. The study used the proposed algorithm use the HAPF into three regions of operation: linearized, quasi-linear and non-linearized. These operations were performed using PSCAD/EMTDC. The methodology will be applied in the study for to make sure the HAPF's inverter current slope can be linearized using output lag control, the methodology will focus on defining the corresponding requirements for process lag bandwidth and sampling time. If unexpected trigger signals are generated, triggering devices and HAPF compensating performances could be adversely affected. Finally, In the experiment and in the simulation, the results are compared of a three-phase and single-phase power supply systems with the output lag controller results for HAPF to find out how the data compares. The final results the findings conclude that, there were three things to test for: linearized voltage under load quasi-linear and non-linearized to assess THD of the voltage under load and THD of the system current:

(1) For non-linearized: current THD was 5.6% and voltage under load THD was 27.3%.

(2) For quasi-linear: current THD was 4.3% and voltage under load THD) was 16.4%.

(3) For linearized operation: current THD was 3% and voltage under load THD was 9.8%.(Lam et al. 2012).

The HSeAPF employs a control strategy where a pre-set value of reactive voltage is delivered to the power network to balance the voltage, eliminate harmonics, and keep the

DC link voltage at the pre-set value. In summary, the current work contributes the following:

- i. Increasing the HSeAPF system performance in terms of speed convergence and accuracy.
- ii. Ensure that the level of compensation of voltage swell/sag is appropriate for all conditions of operation.
- iii. Achieve the limits of the Total Harmonic Distortion (THD) on the power distribution network at the Point of Common Coupling (PCC) for different scenarios. This requirement by the IEEE-519 standard (Recommended Practice and Requirements for Harmonic Control in Electric Power Systems,“ in IEEE Std 519–2014 (Revision of IEEE, 2014), and therefore, needs to be satisfied in a power distribution system.

This paper is organized in subsequent sections as follows:

Section II: This section highlights system configuration, including the calculation of important parameters.

Section III: The system’s schematic diagrams and control strategies have been presented and discussed in this section.

Section IV: In this section, the results from MATLAB / SIMULINK are presented and analysed.

Section V: Research conclusions.

## 2 Configuration of the System

In this section, the HSeAPF system modelling has been presented and analysed. Figure 1 comprises an AC Thevenin equivalent of a three-phase source, shunt passive filter, series active filter, and non-linear load. The series active filter (SeAPF) and the Passive Filter (PF) together form the HSeAPF, which is in turn connected to the Point of Common Coupling (PCC) via an interface transformer in each of the phases. The quality of voltage is improved by the SeAPF, while the current harmonics are eliminated by the PF. The reference voltage for the PWM simulated gate triggering pulses is generated by the SRF operated on PLL. An ideal source can replace the battery to feed the capacitor of the DC link, whose voltage can be controlled using the SMC to maintain it at an appropriate level.

### 2.1 Parameter’s selection of system

In order to compensate for voltage swell/sags and fluctuations, and harmonics from either the load or supply side, the HSeAPF normally functions as a voltage regulator. The problems mentioned above are eliminated by injecting an appropriate amount of voltage or harmonic components

into the PCC through the coupling transformer. The passive filter will reduce the effect of 5th, 7th and 11th current harmonics. Thus, the current passing through the series Voltage Current Control (VSC) is the as the current in the grid (Safa et al. 2018).

The importance of the DC link is that it helps to stabilize the ripples which are produced by the high frequency switching circuits. Furthermore, it helps in balancing the fluctuating instantaneous power that is injected into the power network. The ripple current is simply the total root-mean-square value of the amount of current that can pass through a capacitor without causing it to fail. The DC link capacitor stabilizes and smoothens the injected currents or voltages. The DC link voltage ( $V_{dc}$ ) is influenced by the modulation depth ( $m$ ) – which is taken as 1, and the peak phase voltage ( $V_{ph-peak}$ ). The magnitude of the DC link voltage should be  $\geq 2 * V_{ph-peak}$  (Singh et al. 2015), and is calculated using the equation:

$$V_{dc} = \frac{2V_{ph-peak}}{m} \quad (1)$$

Based on the above equation, an RMS voltage of 230 V gives a peak phase voltage of 325.27 V, considering that the minimum required value of DC link voltage = 650.5 V. Here, the selected value of DC link voltage could about 700 V. The sizing of the DC link capacitor is dependent on the power requirements and the magnitude of DC link voltage. The following energy balance equation is applicable for the DC link capacitor:

$$C_{dc} = \frac{3kV_{ph-rms}I_{se}t}{0.5(V_{dc}^2 - V_{dc-min}^2)} \quad (2)$$

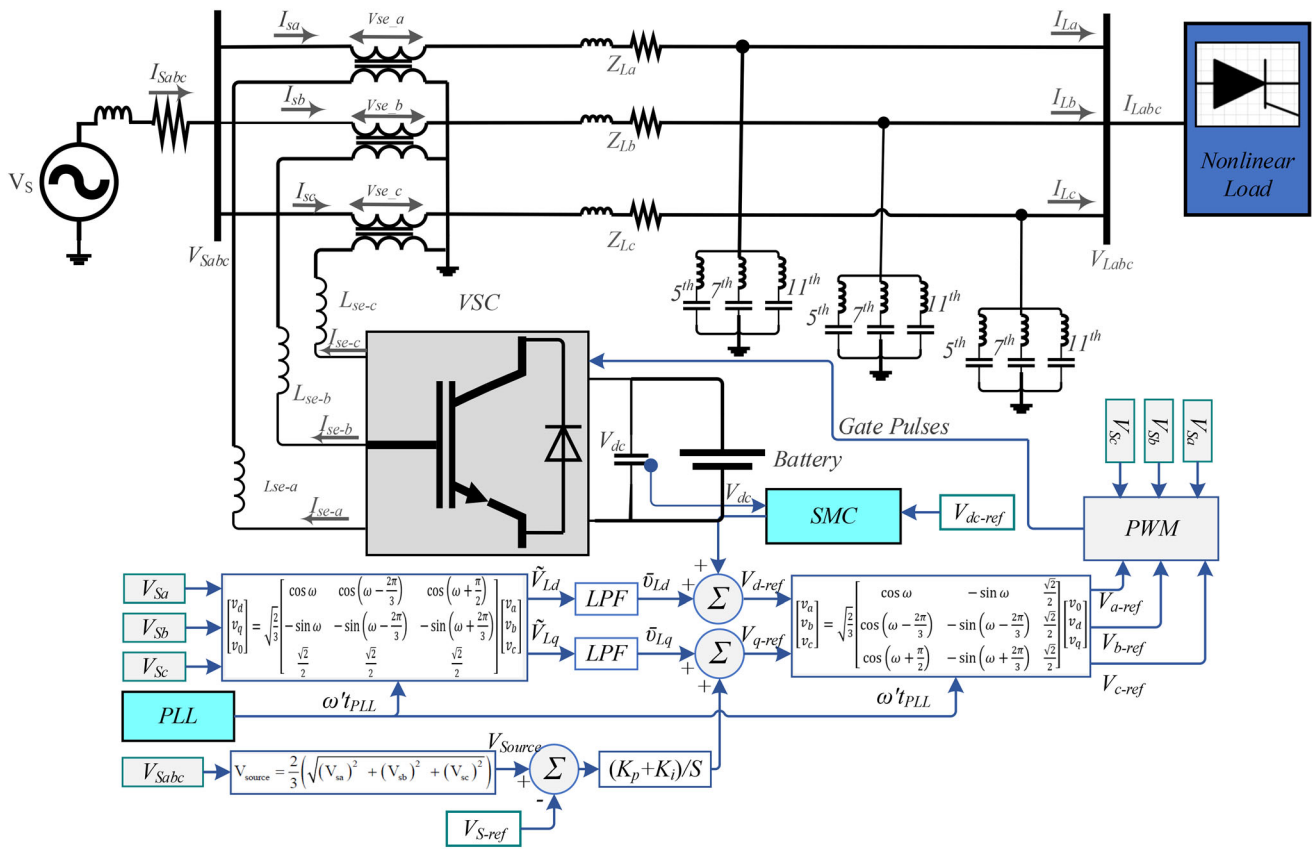
In Eq. 2 above  $V_{dc-min}$  represents the minimum DC bus voltage required,  $k$  represents the energy variation factor throughout dynamics,  $I_{se}$  represents the series phase current of the compensator,  $t$  is the minimum time that can be taken to achieve steady value after disturbance.

In an example design, the above values are given as follows:  $V_{dc-min} = 650.5$  V,  $V_{dc} = 700$ ,  $k = 0.1$ ,  $V_{ph-rms} = 230$  V,  $I_{se} = 35$ ,  $a = 1.5$  and  $t = 4ms$ . Calculating, the value of  $C_{dc} = 0.04335$   $\mu$ F (Devassy and Singh 2017).

It is considered that the SeAPF handles 0.5 of the system’s kVA rating, and twice the KVA handling capability for  $n$  cycles under transient conditions. The following equation gives the instantaneous reactive power:

$$Q_i = V_{se} \cdot I_{se} \quad (3)$$

For  $i = a, b, c$ . Where,  $k$  represents the phase rotations, and  $V_{se}$  represents the compensation voltage. Given that the filter does not generate active power, the sum of reactive power gives zero, i.e.



**Fig. 1** Schematic Diagram of the HSeAPF based on SMC and PLL-SRF

$$V_{se}i_{sa} + V_{s}i_{dc} = 0 \tag{4}$$

The compensation for a swell/sag according to the design of the SeAPF is 0.25 pu, that is,  $V_{se} = 81.3$  V. Therefore, the minimum voltage to be injected at a DC link voltage of 700 V leads to a low modulation index for the series compensator. Operating the SeAPF with minimum harmonics requires the use of a series transformer, whose turn ratio is given by:

$$N_{Se} = \frac{V_{ph}}{V_{Se}} \tag{5}$$

The transformer rating is given by:

$$S_{Se} = 3V_{Se}I_{se|swell} \tag{6}$$

The ratio of the transformer turns obtained from Eq. 5 is  $N_{Se} = 4.001 \approx 4$ , and the transformer rating from Eq. 6 is  $S_{Se} = 8.5$  kVA when the grid is under swell/sag. The interfacing conductor of the series compensator is rated depending on the ripple current are either swell, sag or fluctuation, DC link voltage and switching frequency. The rating value is given by:

$$L_{se} = \frac{\sqrt{3}mV_{dc}N_{Se}}{12af_{sw}I_{ripple}} \tag{7}$$

In the above equation,  $f_{sw}$  represents the switching frequency – 12 kHz (Devassy and Singh 2017), while  $I_{ripple}$  represents the inductor current ripple, taken as 20% of the grid current. Hence, the value of  $L_{se} = 2.405$  mH.

The shunt passive filter is a second-order damped filter comprising L-C components in a parallel arrangement. The PF accommodates the flow of low impedance sink for harmonic frequencies towards the grid. For all harmonic frequencies, the PF offers low impedance, but at fundamental frequency, it offers large impedance. The impedance of the passive filter can be obtained using the equation:

$$Z_{pf} = \frac{jL_{pf}\omega}{1 - L_{pf}C_{pf}\omega^2} \tag{8}$$

At frequencies lower than the fundamental frequency, one of the impedances of the filter is inductive capacitive for all higher harmonics. Therefore,

$$\text{If } \omega < \frac{1}{\sqrt{L_{pf}C_{pf}}}, \text{ Then } Z_{pf} = \frac{1}{\omega C_{pf}}, \text{ Else } Z_{pf} = L_{pf}\omega \tag{9}$$

$L_{pf}$  and  $C_{pf}$  are selected such that at the fundamental frequency, they give a maximum  $Z_{pf}$ . The resonant frequency desired is 60 Hz, and is given by:



$$f_r = \frac{1}{2\pi} \sqrt{1/L_{pf} C_{pf}} \quad (10)$$

### 3 Control OF HSeAPF

The control of the HSeAPF is connected to the utility system in series is through a matching transformer to prevent harmonic currents from reaching the supply system or to recompense for load voltage distortion. It is programmed to provide zero impedance to the fundamental frequency at the PCC and high impedance to harmonic frequencies to prevent harmonic currents from entering the system. It injects the necessary voltage for compensation of voltage harmonics, voltage sags /swells in dynamic voltage restoration, voltage flicker, and other voltage disturbances at the PCC. With line impedance and shunt passive filters, it can also be utilized to dampen harmonic propagation induced by resonance. For recompensing voltage-source nonlinear loads, the series active filter works well. The series active filter's role is to isolate current harmonics between the load and the source, not to directly compensation for the load's current harmonics. The disability of the series active compensator to directly compensation for current harmonics, balance the load current, suppress neutral currents, and recompense for reactive power is a disadvantage. It also carries full load current and must be able to tolerate high power ratings. If the filter's transformer fails, the load will be cut off from the power supply. Series active filters are either voltage or current sources that can be controlled. In addition, the PF compensates for harmonics created by the load current.

The quality and performance of the APF depends partially on the modulation and control method used to implement the recompense schema. Several control strategies can be used to regulate the current produced by the filter: variable switching frequency, such as hysteresis and SMC allow direct control of the current but make the design of the output filter quite difficult as well as the reduction of the noise level. PWM control removes these problems, but the dynamic reply of the current feedback loop reduces the ability of the filter to recompense for fast current transitions. Several algorithms in time and frequency domains are proposed to extract or estimation recompensing harmonic references for controlling the APFs. The most prevalent are the time-domain methods such as the notch filter, the instantaneous reactive power theory (IRPT), (SRF) theory, high-pass filter method, low-pass filter method, unity PF method, SMC, passivity-based control, (PI) controller, flux-based controller, and sine multiplication method. The chief advantage of these time-domain control methods compared to the frequency-

domain methods based on the fast Fourier transformation (FFT) is the fast response obtained. On the other side, frequency domain methods provide accurate individual and multiple harmonic load-current detection (Altawil et al. 2012; Al-Masri et al. 2019; Narayan and Lakshminarayana 2018; Altawil et al. 2012; Golestan et al. 2020). The most important of the available methods is the SRF-based PLL for the inverter and the SMC used for the DC link. The latter has been used in this current.

#### 3.1 PLL Algorithm

A PLL is employed to help in phase-detecting grid voltages and extracting the fundamental voltage signals from the system based on their phase difference.

The design of the PLL technique is such that it functions properly in varying conditions of voltage distortion. There are three-phase grid voltages in Fig. 2 that have been detected, measured and applied as input signals to PLL. The angle of transformation is evaluated as output of the PLL. Upon evaluation, a product of the line voltages and auxiliary feedback currents alongside three-phase auxiliary instantaneous active power signals and unity amplitude is obtained. The frequency of the loop is controlled by the error between the signals (M. Allehyani, H. Samkari and B. K. Johnson 2016). When the two signals have a phase difference, the signals will have a varying frequency. A phase detector compares the frequencies of the oscillator output and the input signal (Dash and Ray 2018). This enables it to generate an error signal corresponding to the phase difference created by the two signals. Based on how precise the PI gains are tuned,

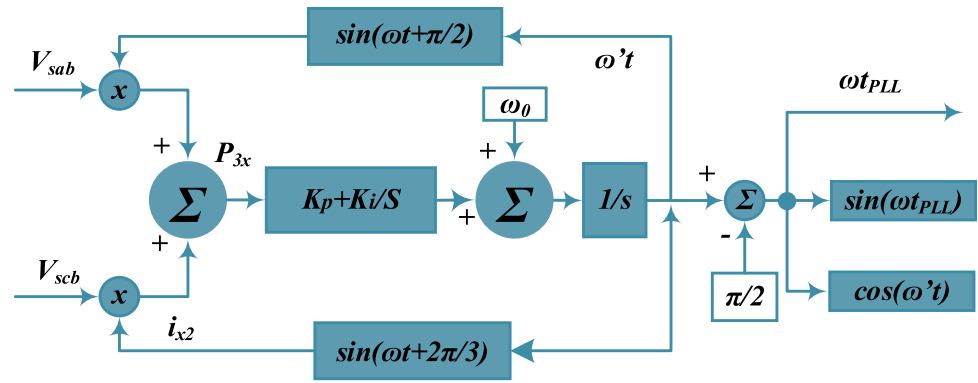
The PLL technique can operate effectively under distorted grid voltages. In this research work, the PLL circuit and SRF control scheme have been used in system design.

#### 3.2 Synchronous reference frame

The reference compensating voltages which the series transformers need to inject are calculated using the SRF control algorithm. The signal generation algorithm for reference voltage depends on the PLL scheme and SRF algorithm (see Fig. 1).

The three-phase voltage supplied is detected by the interface transformer in the reference frame  $abc$ , before conversion to a d-q-0 component to evaluate the reference load voltages according to Eq. 11 below:

**Fig. 2** PLL Circuit Block Diagram



$$\begin{bmatrix} v_d \\ v_q \\ v_0 \end{bmatrix} = \frac{1}{\sqrt{3}} \begin{bmatrix} \cos(\omega) & \cos(\omega - \frac{2\pi}{3}) & \cos(\omega + \frac{\pi}{2}) \\ -\sin(\omega) & -\sin(\omega - \frac{2\pi}{3}) & -\sin(\omega + \frac{2\pi}{3}) \\ \frac{\sqrt{2}}{2} & \frac{\sqrt{2}}{2} & \frac{\sqrt{2}}{2} \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \tag{11}$$

$$\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = \frac{1}{\sqrt{3}} \begin{bmatrix} \cos(\omega) & -\sin(\omega) & \frac{\sqrt{2}}{2} \\ \cos(\omega - \frac{2\pi}{3}) & -\sin(\omega - \frac{2\pi}{3}) & \frac{\sqrt{2}}{2} \\ \cos(\omega + \frac{\pi}{2}) & -\sin(\omega + \frac{2\pi}{3}) & \frac{\sqrt{2}}{2} \end{bmatrix} \begin{bmatrix} v_0 \\ v_d \\ v_q \end{bmatrix} \tag{12}$$

The d-axis  $v_d$  and q-axis  $v_q$  components that are obtained comprise average component and oscillating component:

$$v_d = \bar{v}_d + \tilde{v}_d \tag{13}$$

$$v_q = \bar{v}_q + \tilde{v}_q \tag{14}$$

The components shown in Eqs. (13) and (14) above are as a result of the unbalanced grid voltage with harmonics. Oscillating components show that there exists harmonics as well as negative sequence components of the grid voltages, which are caused by conditions created by distorted load. Conversely, the average components show that the voltages have positive sequence components. The presence of zero sequence components  $v_0$  show that there are unbalanced grid voltages. Both zero and negative components are fixed to zero in order to cancel the unbalanced voltage, harmonics, and distortions in voltage signals. On the other hand, the positive sequence component passes through the LPF to achieve the average value.

To obtain the voltage amplitude for compensating source voltages ( $V_{sa}$ ,  $V_{sb}$ ,  $V_{sc}$ ), the value of AC voltage at the source ( $V_{Source}$ ) is calculated using the equation below:

$$V_{Source} = \frac{2}{3} \sqrt{V_{sa}^2 + V_{sb}^2 + V_{sc}^2}$$

The reference voltages ( $v_a^*$ ,  $v_b^*$ ,  $v_c^*$ ) is the output of the inverse transformation in Eq. (12), which is compared with the actual load voltages ( $v_{La}$ ,  $v_{Lb}$ ,  $v_{Lc}$ ) in sinusoidal PWM controller, producing the switching signals for the Insulated Gate Bipolar Transistor (IGBTs) in SeAPF.

### 3.3 The DC bus controller

The operation of a HSeAPF is greatly influenced by DC bus dynamic performances. The distribution system is very dynamic, which makes the regulator to be insensitive to load condition, main voltage and system parameters. Thus, a fast response is required to match the rapid changes in grid fluctuations, making it an alternative of the PI controller used in Altawil et al. (2012) which is difficult to tune under these circumstances. Conversely, Sliding Mode Control (SMC) is very robust, with a quick response time (M. Allehyani, H. Samkari and B. K. Johnson, 2016). The SMC block diagram (see Fig. 3) is designed to control level of voltage at the DC link capacitor  $V_{DC}$ . The error resulting between the DC bus voltage and the reference voltage is defined by the state variable  $x_1$  Dash and Ray 2018; Al-Soeidat et al. 2018):

$$x_1 = V_{dc}^* - V_{dc} \tag{16}$$

The derivative of  $x_1$  is the second state variable  $x_2$ :

$$x_2 = \dot{x}_1 \tag{17}$$

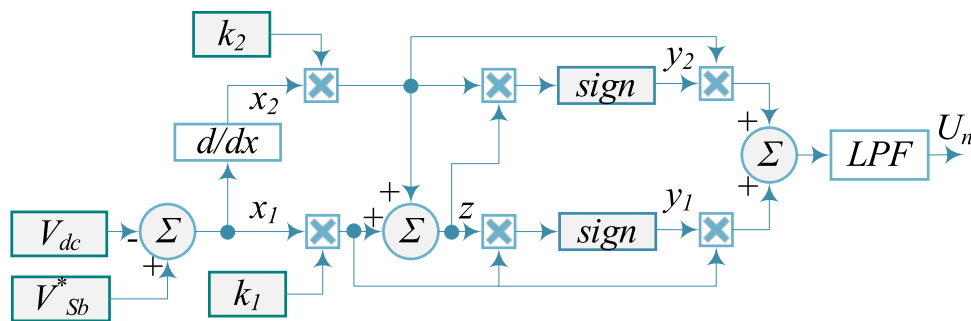
The control term in SMC,  $y = sgn(\sigma)$  is defined as follows:

$$sgn(\sigma) = \begin{cases} +1 & \text{if } \sigma \geq 1 \\ -1 & \text{if } \sigma < 1 \end{cases} \tag{18}$$

The switching functions  $y_1$  and  $y_2$  are defined as follows:

$$y_1 = \begin{cases} +1 & \text{if } x_1 > 0 \\ -1 & \text{if } x_1 < 0 \end{cases} \tag{19}$$

**Fig. 3** SMC Schematic Diagram



$$y_2 = \begin{cases} +1 & \text{if } z x_2 > 0 \\ -1 & \text{if } z x_2 < 0 \end{cases} \quad (20)$$

$$z = c_1 x_1 + c_2 x_2 \quad (21)$$

In Eq. (21) above,  $z$  is the switching function, while  $c_1$  and  $c_2$  are positive constants. The SMC output is calculated using the equation:

$$U_n = x_1 y + x_2 x_2 \quad (22)$$

A low-pass filter with a frequency of 30 Hz is added to minimize the oscillations in the SMC output.

### 4 Results and discussion

The efficiency of the proposed HSeAPF-based Phase Locked Loop-Synchronous Reference Frame (PLL-SRF) and SMC controllers control system was tested on MATLAB/SIMULINK using the parameters presented in Table 1. The SMC controller is used in a three-phase HSeAPF system to control the voltage across DC link capacitor and compared with a conventional PI controller. A diode-rectifier bridge (three-phase) that feeds RL load functions as load that produces harmonic current. Some scenarios have been considered in the simulation analysis. These include a step change in load for transient performance, adding a fifth and seventh harmonics to the source voltage to create up to 20% of nominal source voltage harmonics, and creation of 0.2 pu of swell/sag for several cycles. Two different cases were considered in this research for analysis of HSeAPF performance.

#### 4.1 Case study 1

Ability of HSeAPF to compensate load currents and source voltages under sag and harmonic conditions as follows:

The simulation results for the proposed HSeAPF approach, voltage swell, and harmonics conditions are given in Fig. 4. In this case, a Nonlinear load has been used in the load side with a Total Harmonic Distortion (THD) of 32.3%, 5th and 7th voltage harmonics with a 20% magnitude from the source side between the time (0–0.2) sec

and a voltage swell with a magnitude of 20% is between the time (0.2–0.35) sec. Figures 1(a), (b) show the source voltages, and it is harmonic spectrum with a THD % = 12.3. The load current and the correspondence are depicted in Figs. 4 (c), (d). We can see that the 5th 7th and 11th are the highest harmonics magnitudes.

As illustrated by enlarged results, Fig. 5(a), (b) and Fig. 6(a), (b) show the load voltage profile (using PI with a 320.6 V and 321.7 V using SMC controllers) is maintained at a desired level irrespective of voltage swell and/or voltage harmonics in the source voltage magnitudes, However, the SMC control shows better performance with (THD = 3.75%) over the PI controller with (THD = 5.0%). During the swell compensation, as viewed from Figs. 5(a) - (c), and Figs. 6(a) and (c).

On the other hand, Fig. 5(c), (d) and Fig. 6(c), (d), show the source currents profile after compensation using 3 sets of PFs and using PI and SMC controllers for controlling the DC-link respectively. It could be noticed that the load currents have been compensated successfully to have source current magnitudes with ( $I_s = 32.08$  A and THD = 4.88%) in case of using PI controller and ( $I_s = 32.98$  A and THD = 4.08%) while using SMC controllers for the DC-link.

Both controllers maintain self-supporting dc link voltage and kept the voltage at a pre-set level, However SMC shows faster response time and less oscillation than PI controller.

#### 4.2 Case study 2

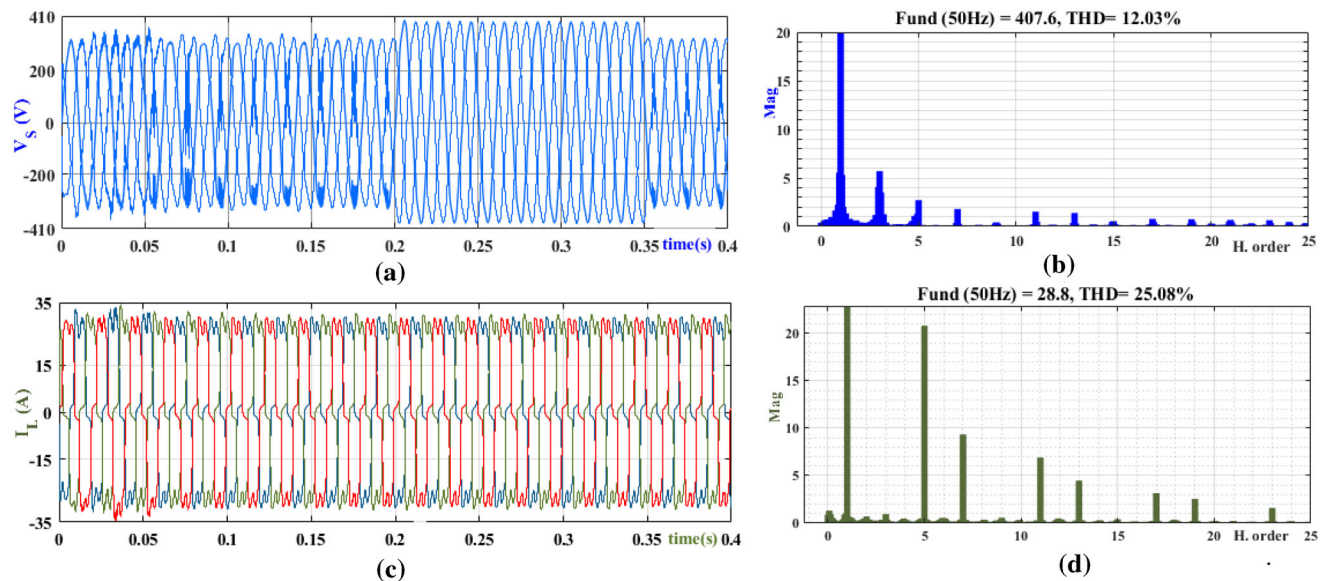
Ability of HSeAPF to compensate dynamic nonlinear load and voltage sag and harmonics:

In this case, the performance for controlling the DC link voltage of HSeAPF using SMC and PI controllers is considered. The comparison criteria is constructed based on the stabilization time of DC link voltage during transient load and disturbance on the supply voltage conditions. Fig. 7 The performance of the HSeAPF for controlling the DC link voltage with SMC and PI controllers for load transient, voltage harmonics and voltage sag conditions are analyzed in the following figures.



**Table 1** main parameters of the proposed module

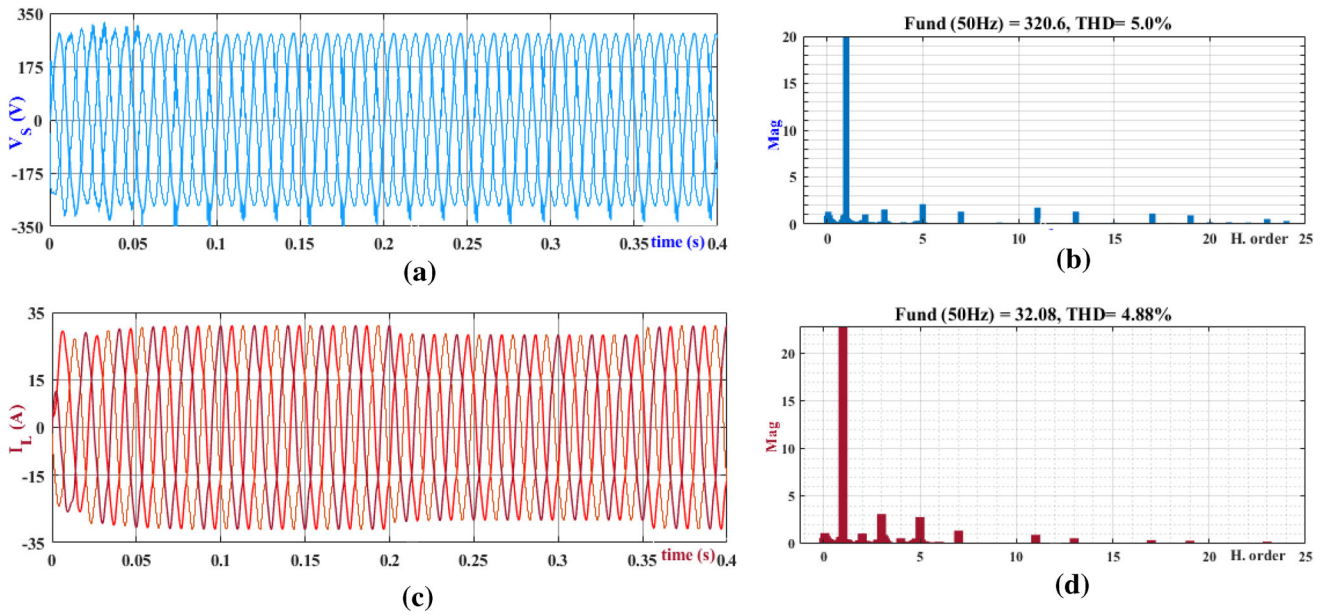
Description	System parameters	
	Parameters	Value
Source	Phase Voltage(rms), $V_s$	230 V
	Frequency $f$	50 Hz
	Source inductance, $L_s$	0.1 mH
Filter	SeAPF coupling inductance $L_{Se}$	2.405 mH
	SeAPF coupling transformer	$Y_g/Y$ and 4:1 turns ratio
Passive filter	5th harmonic	$L_f = 0.9$ mH $C_f = 450.3$ $\mu$ F
	7th harmonic	$L_f = 1.9$ mH $C_f = 213.3$ $\mu$ F
	11th harmonic	$L_f = 2.7$ mH, $C_f = 150.1$ $\mu$ F
Load	diode rectifier	6-diode
	Load resistance	8 $\Omega$
	Load inductance	1.5 mH
DC link	Reference voltage	700 V
	Capacitor	43.35 mF
Ki	Integral gain	1.2
Kp	Proportional Gain	0.02

**Fig. 4** **a, b** Source voltage, and it's harmonic spectrum. **c** And **d** load current, and it's harmonic spectrum respectively under voltage harmonics and voltage swell conditions

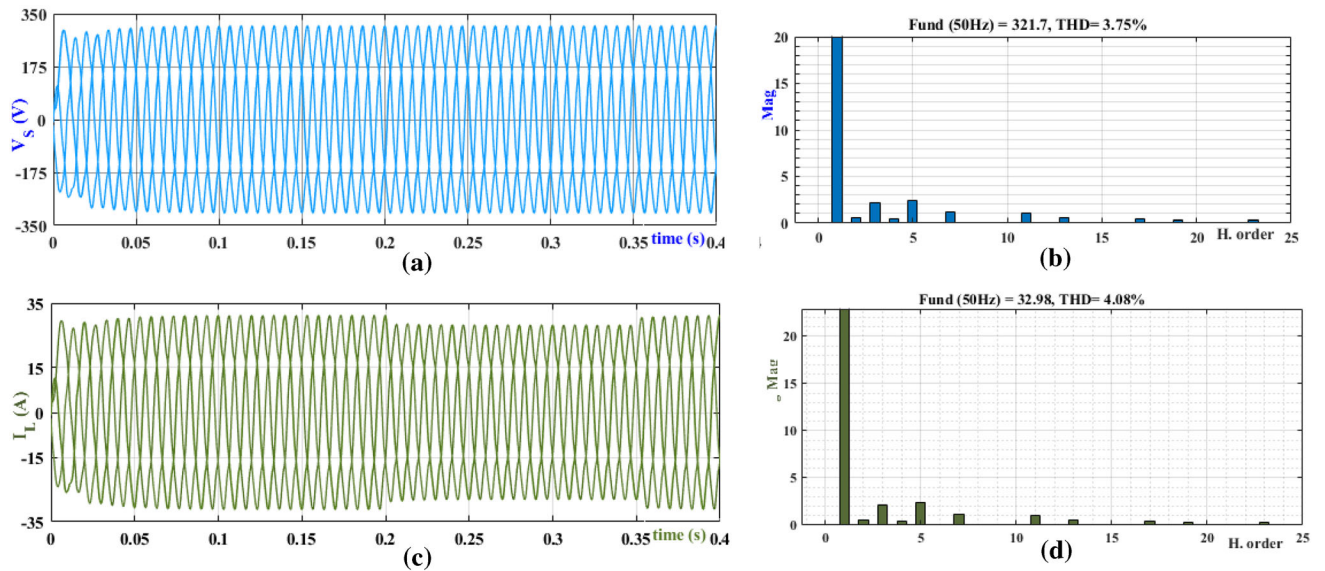
Figures 8(a) and (c) show the source voltages and the load currents, while Figs. 8(b) and (d) depict the correspondence harmonic spectrum for the waveforms, respectively. In Figs. 8(c), (d), the nonlinear load has been changed between the time (0.2–0.3) sec, the load current has increased by 30% with a THD% = 26.18. On the load side, Figs. 8(a), (b) show 5th and 7th voltage harmonics with a magnitude of 15% each and a 20% voltage sag from the source side between the time (0.05–0.15) sec and a THD% = 16.73.

The distinct features of the proposed HSeAPF approach are outlined as follows.

- (1) As illustrated by enlarged results, Fig. 9(a), (b) and Fig. 10(a), (b) show the load voltage profile in the case of using PI and SMC controllers in the DC-Link voltage control. This load voltage has maintained at the desired level irrespective of voltage sag and/or voltage harmonics in the source voltage magnitudes. However, the SMC control shows better performance (with a magnitude of 322.6 V And THD% = 3.85)



**Fig. 5** a, b Compensated load voltage, and its harmonic spectrum. c And d Compensated source current and its harmonic spectrum respectively using PI controller under voltage harmonics and swell conditions



**Fig. 6** a, b Compensated load voltage, and its harmonic spectrum c and d Compensated source current and its harmonic spectrum respectively using SMC controller under voltage harmonics and swell conditions

over the PI controller with (a magnitude of 320.32 V and THD% = 5.50).

On the other hand, Fig. 9(c), (d) and Fig. 10(c), (d), show the source currents profile after compensation using PI and SMC controllers in the DC-Link voltage control, respectively. It could be noticed that the load currents have been compensated successfully to have source currents

magnitude and harmonic spectra after compensation with ( $I_s = 32.38$  A and THD% = 4.78) using PI and ( $I_s = 33.08$  A and THD% = 3.02) using SMC controllers for the DC link voltage. Here we can notice that the THD has farther decreased using SMC, which is due to the better compensation of the voltage harmonics by the SMC which in turn reflects on the reduction of the current harmonics. Fig. 11.

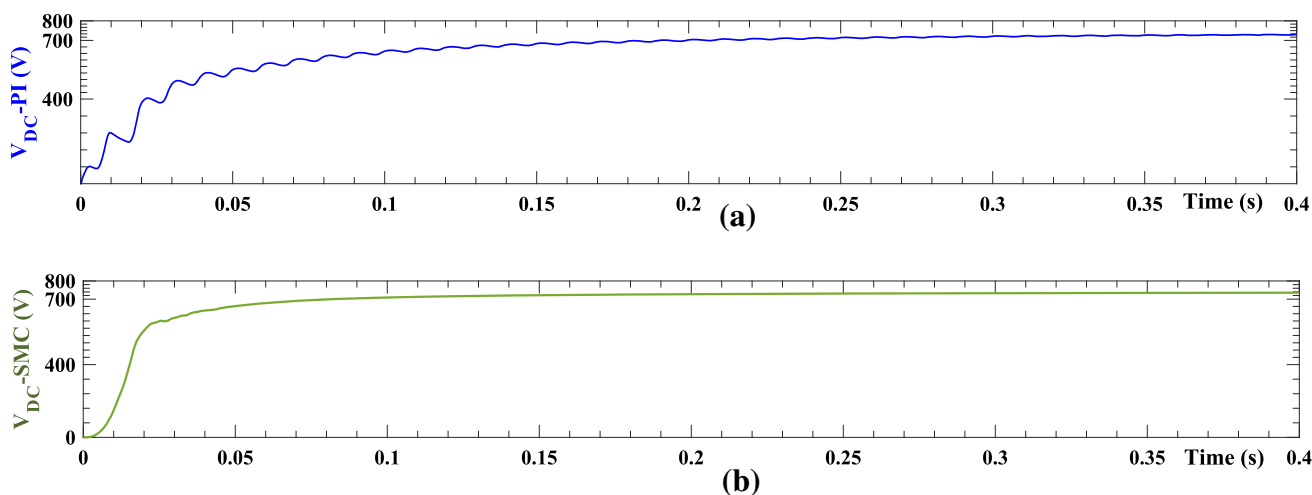


Fig. 7 DC Link voltage **a** using PI controller. **b** SMC controller under voltage harmonics and swell conditions

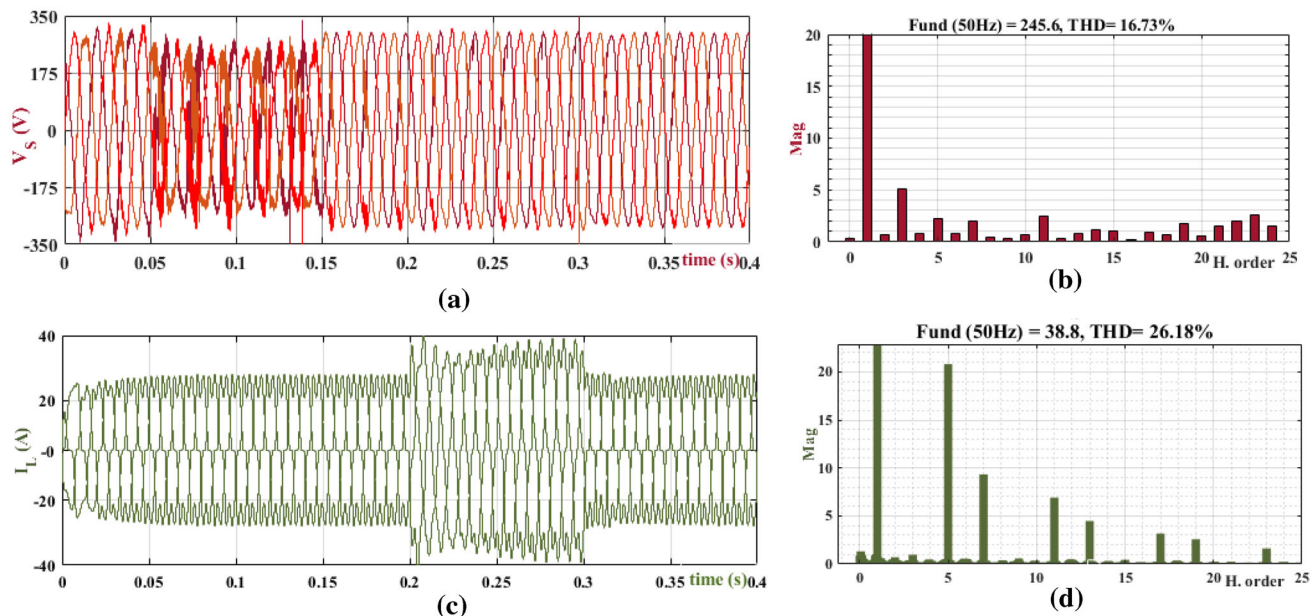


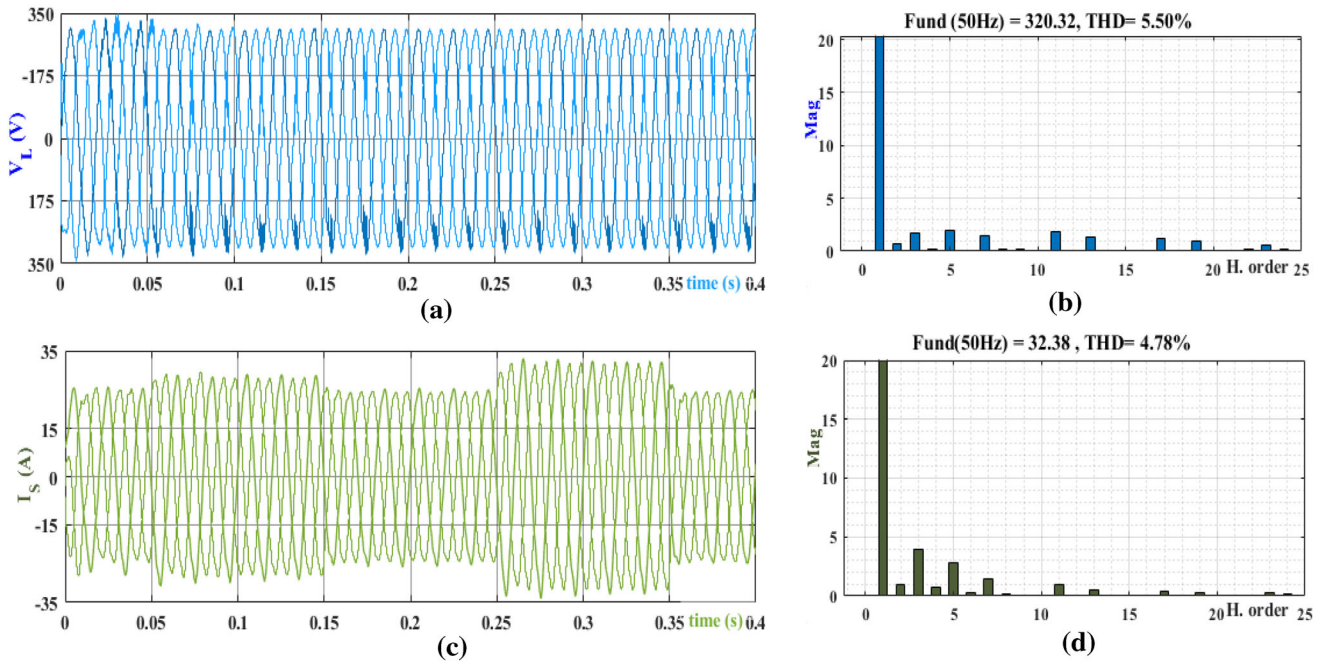
Fig. 8 **a, b** Source voltage, and its harmonic spectrum **c** and **d** load current, and its harmonic spectrum respectively under dynamic nonlinear load, voltage harmonics and sag conditions

### 5 Conclusion and future work

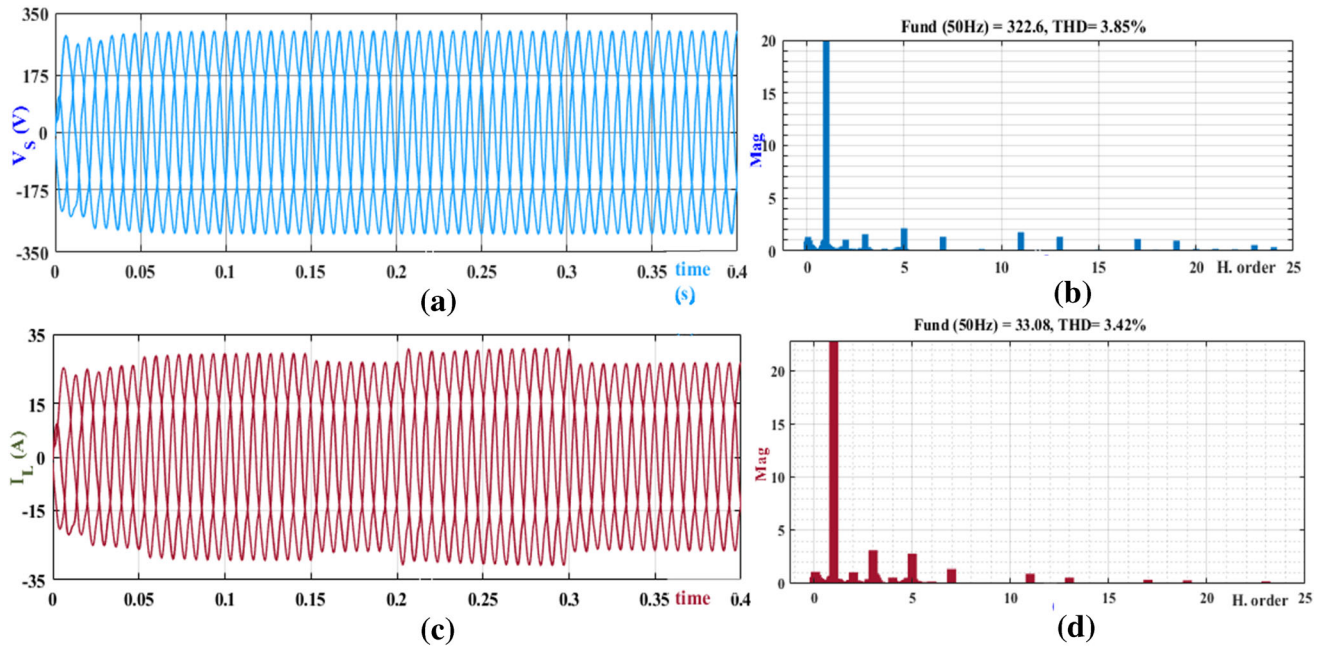
The primary objective of this paper was to examine and evaluate how HSeAPF can influence the distribution of disturbances and current harmonics such as voltage swell/sag and non-linear load in grid voltages. The simulation performed using MATLAB/ SIMULINK software show how effective the HSeAPF is under different scenarios. The performance of the proposed system was verified under two simulation study scenarios of current harmonics and voltage swell/sag. Based on the simulation results, the

proposed system can effectively compensate for swelling/sagging voltage at the grid side, voltage harmonics and current harmonics on the load side. The SMC and PI controllers all maintain self-supporting DC link voltage so that the system voltage is maintained at an appropriate level. Contrary to the PI controller, the SMC shows a quicker response time and less oscillation. In addition to a fast response, SMC is very robust in comparison to the conventional PI controller. In Future work, this study can be to build the hardware in some scale to prove your simulations are accurate, if we cannot build the whole

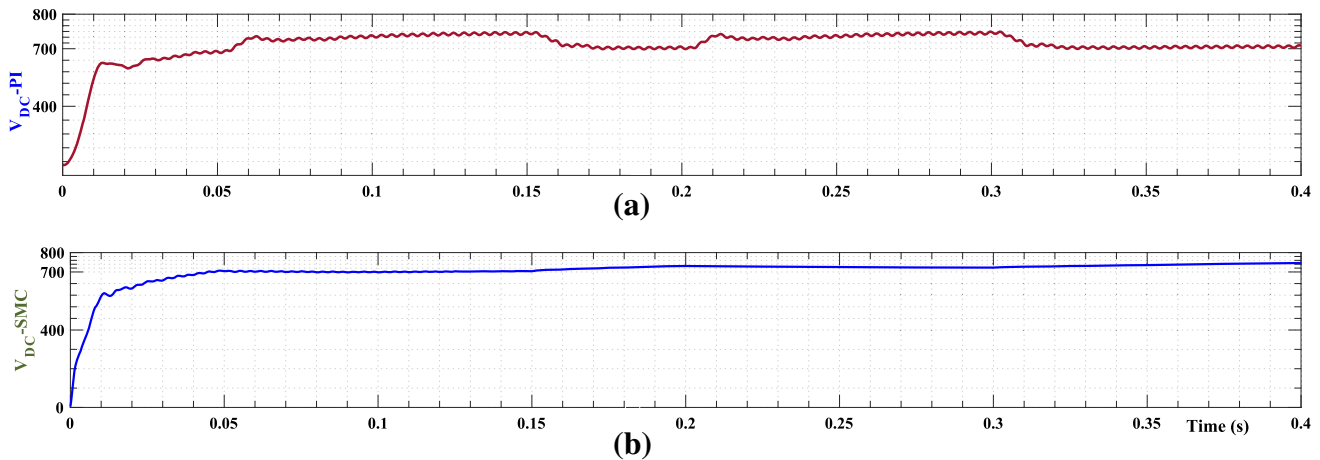




**Fig. 9** a, b Compensated load voltage, and its harmonic spectrum c and d Compensated source current and its harmonic spectrum respectively using PI controller under dynamic nonlinear load, voltage harmonics and sag conditions



**Fig. 10** a, b Compensated load voltage, and its harmonic spectrum c and d Compensated source current and its harmonic spectrum respectively using SMC controller. Under dynamic nonlinear load, voltage harmonics and sag conditions



**Fig. 11** DC Link voltage **a** using PI controller **b** SMC controller under dynamic nonlinear load, voltage harmonics and sag conditions

system may be a part of it that can be tested in the lab. The obtained harmonic spectra %THD for load voltages and source currents falls within the 5% limit, which is acceptable by *IEEE-519* and *IEC 61,000–3-6* standards.

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**Data Availability** No data were used to support this study.

#### Declarations

**Conflicts of Interest** The authors declare that they have no conflicts of interest.

**Ethical approval** All procedures performed in studies involving human participants were in accordance with the ethical standards of the institutional and/or national research committee and with the 1964 Helsinki declaration and its later amendments or comparable ethical standards. All applicable international, national, and/or institutional guidelines for the care and use of animals were followed.

**Informed consent** Informed consent was obtained from all individual participants included in the study.

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