



Design of Reconfigurable Inductorless RF VCO in 130 nm CMOS

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Abstract

The need for low-power and low-cost connected devices supporting several communication standards continues to increase with the rising demand in Internet of Things (IoT) applications. This paper presents a reconfigurable inductorless radiofrequency (RF) voltage-controlled oscillator (VCO) capable to work across various frequency bands with a low area. This VCO has an inductor-capacitor (LC) topology though using an active inductor based on a gyrator-C structure. It uses n-bits controlled CMOS inverters for coarse frequency tuning and diode varactor for fine frequency tuning. Implemented in 130-nm CMOS technology, the VCO can cover a frequency tuning of 1.22–2.6 GHz. It achieves a phase noise of -87 dBc/Hz at 1 MHz with a power consumption of 4 mW from 1.1-V supply. The active die area is only $54 \times 59 \mu\text{m}^2$.

Keywords LC-VCO · Active inductor · RF, CMOS · IoT · Multistandard, low-power

1 Introduction

The Internet of Things (IoT) has been hailed as the next frontier of innovation in which everyday objects in our environment (homes, offices, cars, factories, cities) connect to the Internet in ways that improve our lives. The IoT market is poised to exceed 75 billion devices by 2025, but several challenges remain in adding more connectivity to electronic devices, including cost, energy efficiency, security, and interoperability [1]. The main idea behind the IoT concept is the ability of data storage and exchange between different devices, connecting a large number of smart objects.

Many communication standards have been developed to deal with the demands of IoT applications. Some of which are Bluetooth Low Energy (BLE), ZigBee, LoRaWAN, and Wi-Fi HaLow (IEEE 802.11ah) [2, 3]. To provide multistandard operation, the most used solution was to combine several fixed narrowband radiofrequency (RF) receivers in radio systems with multiple chips [4]. But this strategy is expensive, not flexible and power hungry. As a solution, it is necessary to design reconfigurable multistandard with low-power and single-chip radio frontend.

Figure 1 presents the topology of a typical IoT node. It is composed of a microcontroller (MCU) that processes the sensed data and runs software stacks interfaced to a wireless device for RF connectivity. Since IoT devices must support several communication standards, each IoT node comprises multistandard radio module. Its design should be optimized to be energy efficient as it is battery-powered.

Therefore, the challenge is to design low-cost, low-power, and multistandard transceivers. This trend will continue in the future by the constant rise of connected device requirements. The voltage-controlled oscillator (VCO) is a key building block in all radio transceivers. It generates signals that can be used for frequency synthesis and clock generation, for example.

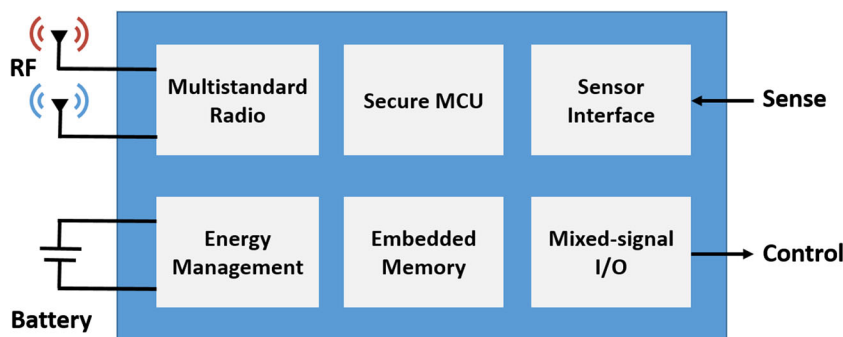
The development of the VCO building block that is still challenging must support wideband operation, be reconfigurable, and have suitable phase noise to address simultaneous multistandard communications. Besides, inductorless topologies are required since they lower the circuit area and then the chip cost.

Conventionally, ring-based VCO is characterized by a wide tuning range and low area occupation. Inductor-capacitor (LC)-VCO has better phase noise but occupies larger chip area and its frequency tuning range is compromised. Several techniques to extend frequency tuning range in LC-VCOs have been presented such as varying the capacitance or the inductor [5]. In the case of capacitors, the changing ratio of varactors is determined by the maximum to minimum capacitance ratio. For typical varactor capacitance ratios, the tuning range of an

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Fig. 1 Topology of a conventional IoT node



LC-VCO is limited to 30%. Hence, active inductors can be used to overcome this restricted tuning range. They also lead to reduce the silicon area and therefore the cost of the chip.

In this work, a novel topology of a multi-band inductorless LC-VCO is proposed. It uses two frequency tuning approaches: an active inductor based on digitally controlled CMOS inverters that concede coarse tuning and a diode varactor for fine tuning.

This paper is organized as follows. Section 2 presents the circuit design considerations. It describes the proposed inductorless VCO topology and investigates the used active inductor. Section 3 shows the circuit implementation and discusses the obtained results. Section 4 draws conclusions.

2 Active Inductor Design Considerations

Designing LC-VCOs requires a great attention when considering the LC-tank since it determines the whole VCO performance. In this work, varactor diode has been used since it presents a good compromise between quality factor, effective parallel equivalent conductance, and frequency tuning range. Moreover, its capacitance value varies linearly with control voltage (V_{ctrl}) comparing with MOS varactors. Concerning the inductor, it is the most vital component in LC-tanks, since its quality factor affects the phase noise and its resistive loss determines the power consumption.

Recent requirements of IoT applications boost the need to design low-power, low-cost, and multi-band oscillators. In order to optimize the circuit design and to respect the various constraints, it is necessary to develop generic and inductorless VCO with digitally tunable performance. In this work, a tunable active inductor will be used to design the inductorless VCO.

2.1 Active Inductor Topology

The proposed active inductor is based on a gyrator-C topology. A gyrator is a well-known circuit that presents at its input a scaled version of the inverse of the impedance connected to its output [6], as shown in Fig. 2(a). In the particular case of using

a capacitive load, an inductive behavior will be present at the input, as shown in Fig. 2(b).

Figure 3(a) depicts the proposed single-ended active inductor topology based on the gyrator-C principle given in Fig. 2(b). The transconductance g_{m1} is realized using a differential pair (M1, M2) while g_{m2} is variable and composed by n CMOS-controlled inverters (Inv1 to Invn). Each inverter is associated with switching transistors (PMOS and NMOS) in order to ensure the control of the inverter via the control voltage V_{ctrl} (cf. Fig. 3(b)). To obtain the transconductance of each inverter, both PMOS and NMOS switches should be closed. While setting n CMOS-controlled inverters in parallel, the value of the equivalent transconductance g_{m2} can be adjusted by modifying V_{ctrl} . There are $2^n - 1$ possible combinations ($V_{ctrl} = [0000]$ is not used). This structure has advantages of high linearity along with simple tuning and integration.

The equivalent impedance of the proposed tunable active inductor can be written as:

$$L_{AI} = \frac{C_A}{g_{m1} \cdot g_{m2}} \quad (1)$$

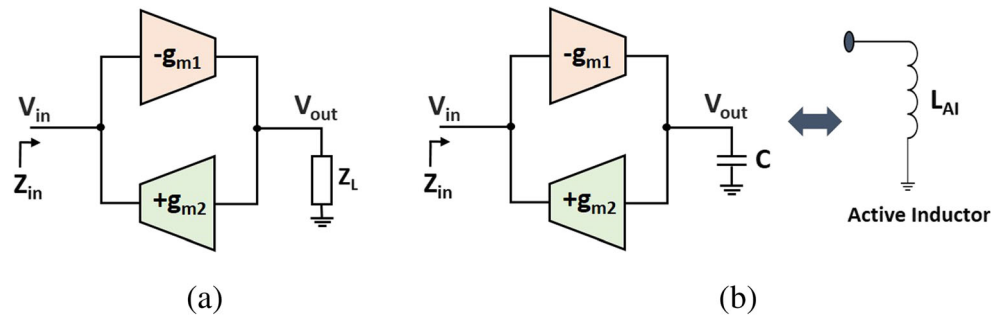
where C_A is given by the capacitance at node A and C_{var} .

Therefore, the inductance value can be modified electronically either by varying the transconductances or the capacitance values. In this work, we propose to adjust both g_{m2} and C_{var} for coarse and fine tuning respectively. In fact, g_{m2} is adjusted depending on the applied digital control word, while C_{var} is varied using a varactor depending on the voltage V_{Cvar} as shown in Fig. 3.

Design considerations have been taken into account in order to optimize the circuit performances. In fact, it is known that a good varactor is characterized by a high-quality factor and a maximal ratio C_{max}/C_{min} leading to large tuning range.

Besides, the series resistance of varactor has an imperious effect on the overall quality factor. In this regard, the diode varactor gives a better compromise between tuning range and Q than the MOS varactor. Afterwards, the focus goes to the active components. An optimal sizing of MOS transistors contributes to a noise reduction. In fact, the transistor noise is directly related to the gate resistance R_g , and then it should

Fig. 2 (a) Ideal gyrator and (b) gyrator-C basic concepts



be decreased. Since sizing the MOS with a maximal number of fingers causes a reduction of R_g , multi-finger transistors have been used in this work to decrease the noise.

A monitoring interface has been developed in order to generate the digital word of the different control voltages and to automate the choice of g_{m2} and therefore the desired inductance value. Besides, a comparative study to determine the optimal number of inverters has been investigated. It exhibits that a g_{m2} with four-stage inverters gives a good compromise between power consumption and frequency tuning range.

2.2 Active Inductor Characterization

An active inductor with four-stage inverters has been implemented in a 130-nm CMOS technology. In this case ($n = 4$), there are 15 possible V_{ctrl} combinations. Figure 4 shows the variation of the inductance versus frequency as V_{ctrl} is varied. It shows that the inductance can be tuned for the frequency of

interest until 2.6 GHz while changing the digital control word V_{ctrl} .

It is mandatory to maintain an inductive behavior of the active inductor and to keep the self-resonant frequency (SRF) higher than the operating frequency for each V_{ctrl} combination. The maximal values of SRF versus V_{ctrl} are given in Fig. 5(a). It shows that SRF increases from 1.64 to 3.16 GHz when changing V_{ctrl} .

Figure 5(b) presents the variation of g_{m2} , the equivalent transconductance of the inverters block, versus V_{ctrl} . It can be noticed that there is a dependence between SRF and g_{m2} and that increasing g_{m2} causes the rise of SRF . In this structure, the transconductance g_{m2} reaches high values and varies linearly between 3.24 and 22.7 mS at various V_{ctrl} that results in a linear variation of the inductance too.

Considering the example of an operating frequency of 1 GHz, the inductance variation versus V_{ctrl} is depicted in

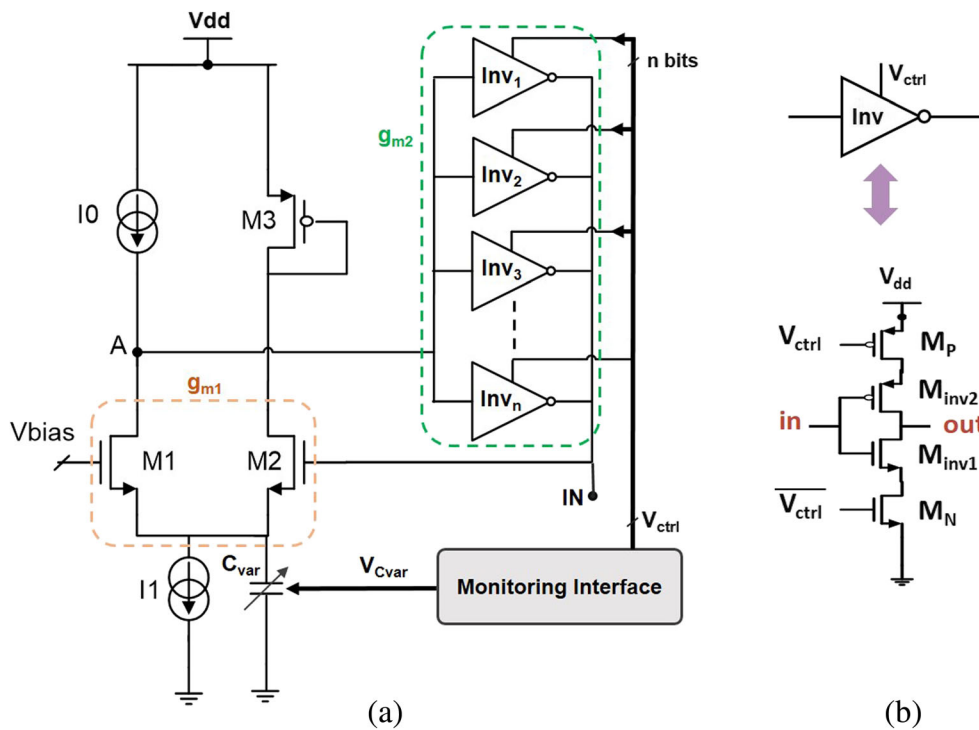


Fig. 3 (a) Proposed active inductor topology. (b) CMOS-controlled inverter structure

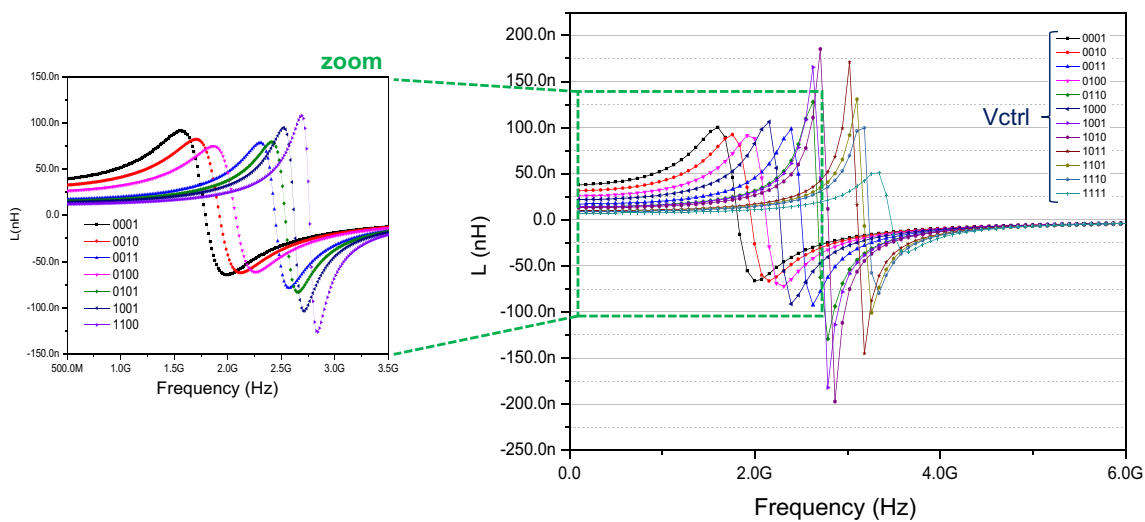


Fig. 4 Active inductor value variation versus frequency for different Vctrl combinations

Fig. 5 Variation of (a) SRF and (b) g_{m2} for the different Vctrl combinations

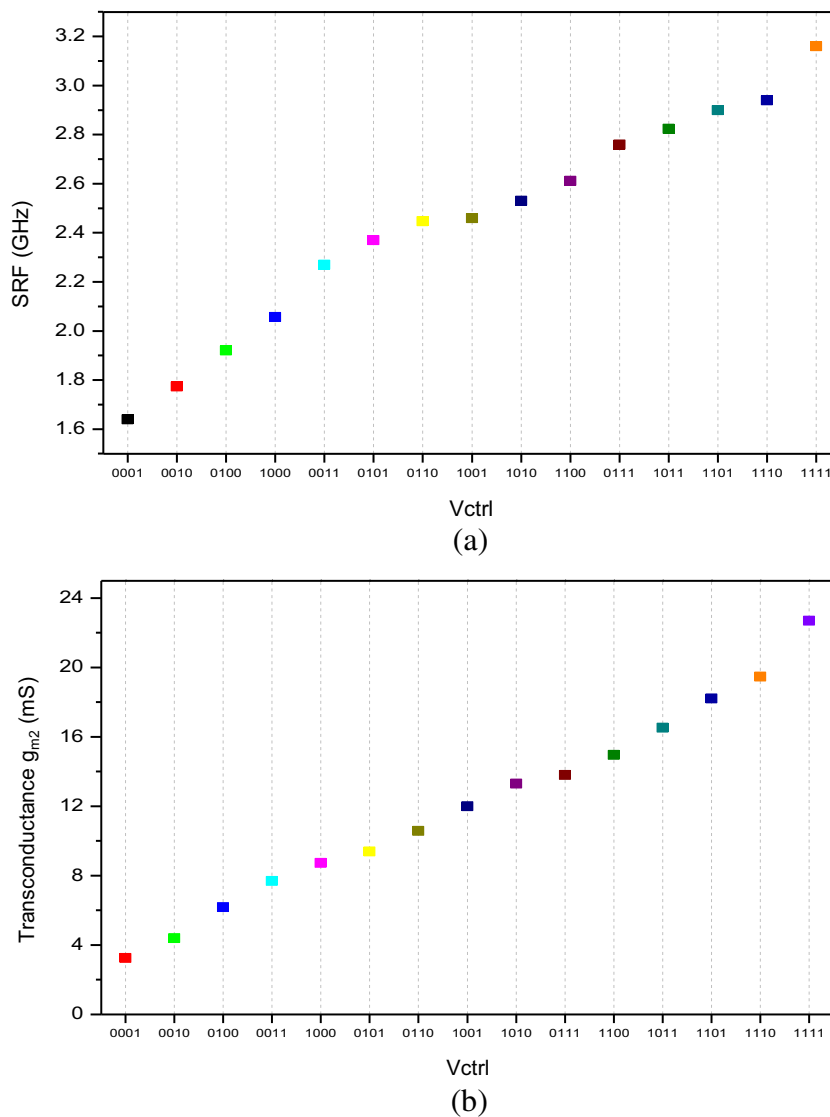


Fig. 6(a). It shows that L_{AI} decreases from 9 to 70 nH. That confirms that g_{m2} and L_{AI} are inversely proportional. The variation of the power consumption of the active inductor versus V_{ctrl} is also given in Fig. 6(b). It shows that the power varies linearly from 2.96 to 3.73 mW from 1.1-V supply.

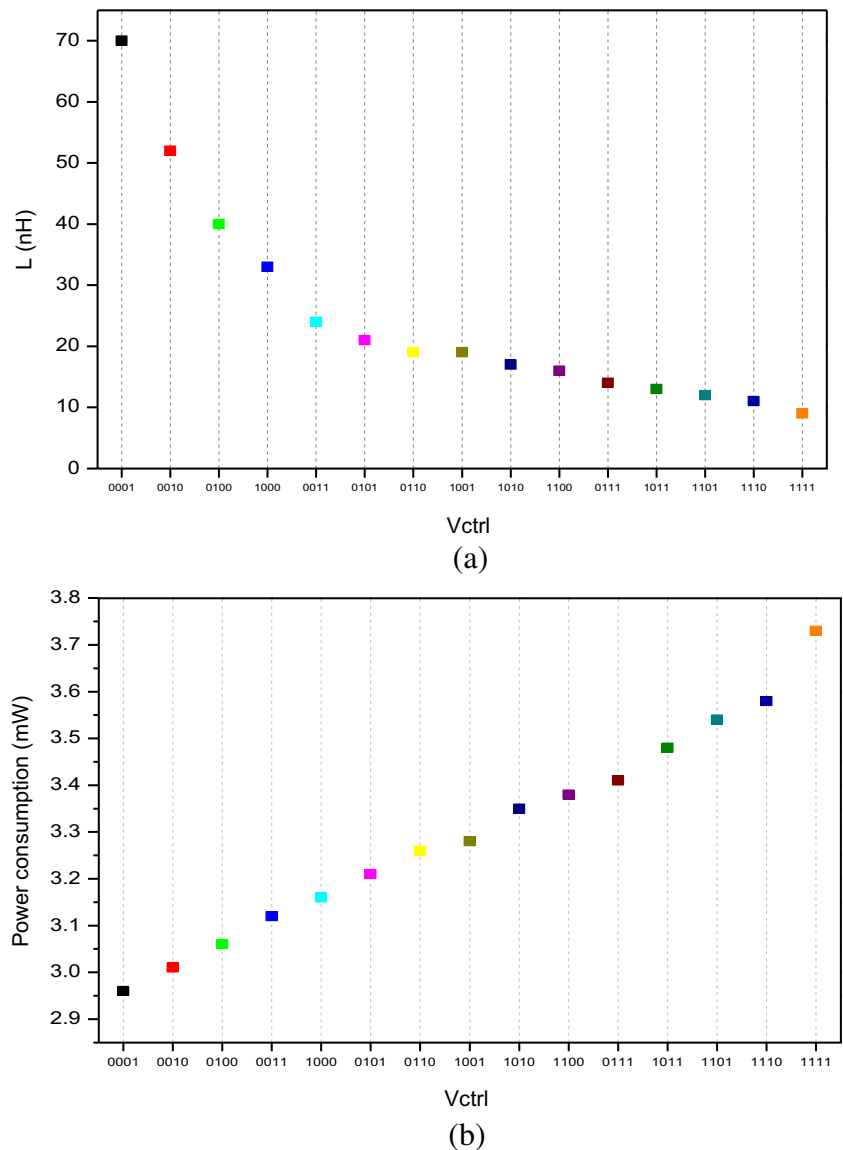
The quality factor (Q) could be defined as the ratio of the imaginary part to the real part of the input impedance. Decreasing the series resistance of the inductor can increase Q at the expense of the noise performance. Figure 7(a) shows the quality factor variation versus frequency for different control voltages. For example, at 2.4 GHz, Q factor equals 26 for $V_{ctrl} = [1110]$, while it is maximal and equal to 63 for $V_{ctrl} = [1011]$. In this case, the inductance value is 25 nH and is associated to a series resistance of 6 Ω . Figure 7(b) illustrates the Q factor and the equivalent inductance versus frequency for this latter case.

Furthermore, with regard to the varactor C_{var} tuning (cf. Fig. 3(a)), it allows not only the adjustment of the inductance value, but also a further tuning of the quality factor. Figure 8 depicts L_{AI} and Q variations versus frequency depending on the varactor value, for example, $V_{ctrl} = [1011]$. It demonstrates that adjusting the varactor has a direct impact on Q and L_{AI} variation. Hence, the controllability and flexibility aspects are well fulfilled with the proposed circuit.

3 Inductorless VCO Design

Figure 9 shows the proposed inductorless LC-VCO topology. It is based on the presented active inductor. Several inductorless LC-VCOs given in the literature use switched

Fig. 6 Variation of (a) the inductance and (b) power consumption for the different V_{ctrl} combinations



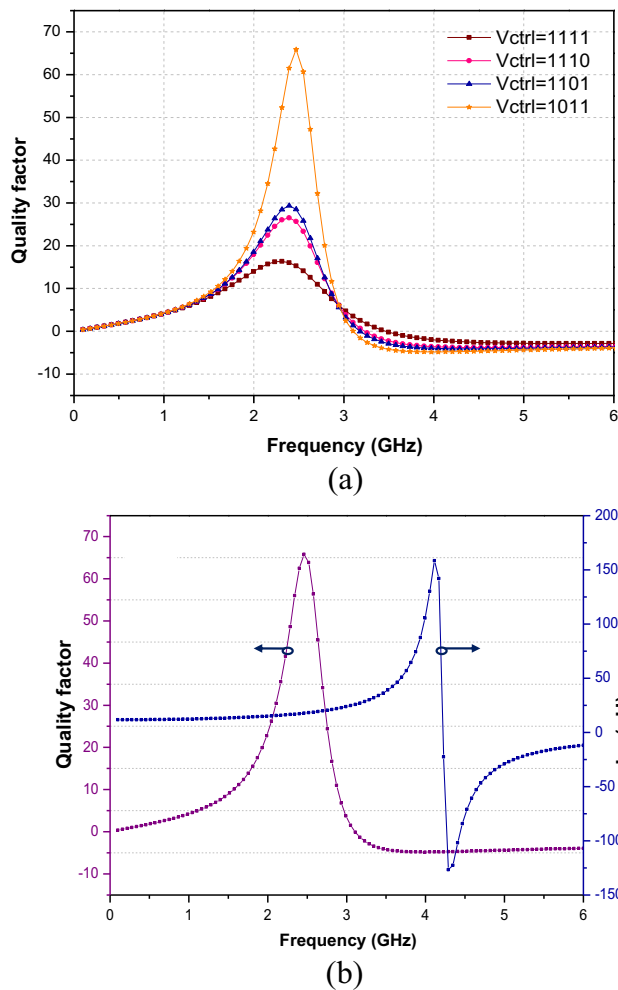


Fig. 7 (a) Quality factor variation for the different Vctrl combinations. (b) Equivalent L_{AI} and Q versus frequency for a fixed Vctrl [1011]

capacitor banks as a capacitor of the tank [7, 8]. However, in this work, the intrinsic parasitic capacitances of MOS transistors will be used to emulate the capacitance C_{tank} in lieu of using additional capacitors. That allows minimizing the circuit size.

This VCO structure uses seven CMOS inverters:

- Four controlled inverters (Inv_1 to Inv_4) that emulate the transconductance g_{m2} of the active inductor.
- An inverter Inv_C for inductor biasing.
- An inverter Inv_A that generates the negative resistance for LC-tank loss compensation.
- An inverter Inv_B that generates the positive resistance for oscillation maintain.

CMOS inverters have been used to keep the VCO simplicity while improving power consumption, area, and linearity performances.

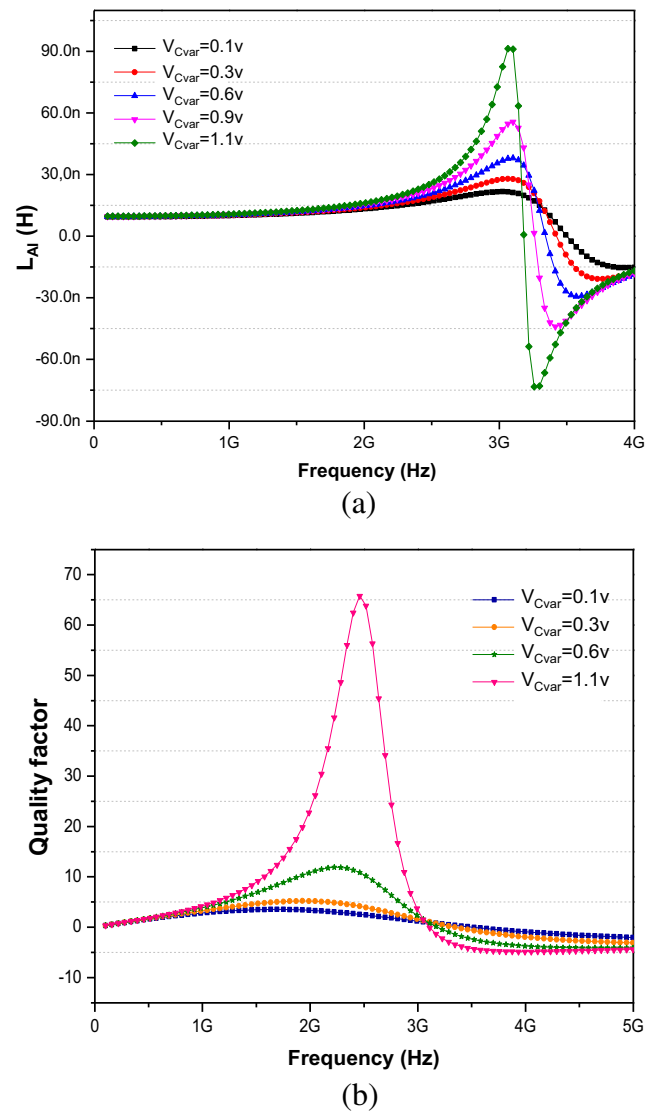


Fig. 8 (a) Equivalent inductance and (b) quality factor responses when tuning the varactor C_{var}

The positive and negative resistances can be expressed as:

$$R_P = 1/(g_{m_InvB}) \tag{2}$$

$$R_N = -g_{m3}/(g_{m_InvA} \times g_{m_diff}) \tag{3}$$

where g_{m_InvA} , g_{m_InvB} , and g_{m_diff} are the transconductances of inverters Inv_A , Inv_B , and of the differential pair respectively.

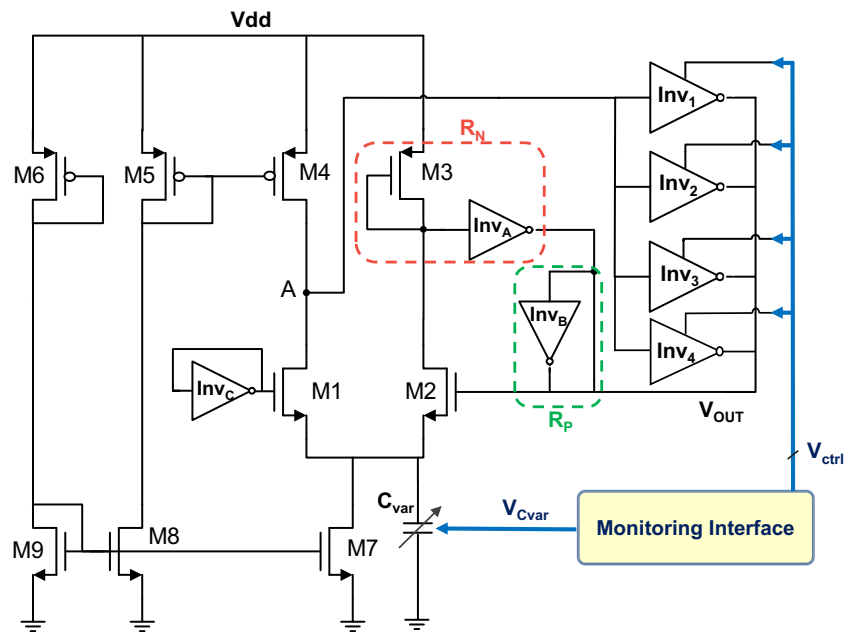
The quality factor of the oscillator at the resonant frequency can be expressed as:

$$Q = RC_{tank}\omega_0 = \frac{R}{L_{AI}\omega_0} = R\sqrt{\frac{C_{tank}}{L_{AI}}} \tag{4}$$

where $R = R_P // R_N$.

According to (5), it can be noted that rising the resistance R results on an increase of the quality factor.

Fig. 9 Proposed inductorless VCO implementation



To maintain oscillation, the quality factor should be higher than $\sqrt{2}/2$ and the positive resistance should be higher than the negative resistance ($R_p > |R_N|$). The VCO oscillation frequency is given by:

$$f_{\text{vco}} = \frac{1}{2\pi\sqrt{L_{AI} \cdot C_{\text{tank}}}} = \frac{\sqrt{g_{m1} \cdot g_{m2}}}{2\pi\sqrt{C_A \cdot C_{\text{tank}}}} \quad (5)$$

Therefore, the VCO frequency could be tuned by adjusting the active inductor value (varying g_{m2} due to the digital control word of the inverters and the control voltage of the varactor C_{var}).

In addition, it can be noted that in the proposed VCO structure, it is possible to ensure a wider frequency tuning range by simply increasing the inverters number n . The power performance will not be greatly degraded in this case if a good compromise between dimensions of CMOS inverters and the overall power consumption is ensured at the desired frequency range.

4 VCO Implementation and Results

The proposed 2.4-GHz inductorless VCO has been implemented in a 130-nm CMOS technology. Its layout and micrograph are shown in Fig. 10. It occupies an area of only $0.0031 \mu\text{m}^2$ excluding pads and $0.212 \mu\text{m}^2$ with pads. Post-layout simulations have been achieved using *Spectre-RF* simulator of *Cadence*® taking into account the non-idealities and the parasitic effects.

All transistors have been sized with the minimum channel length to reduce the power. Decoupling capacitors have been added before I/O pads used to apply DC voltages. A high-input impedance active probe has been adopted to measure the VCO output characteristic. This facilitates the experimental process and avoids using additional buffers for impedance matching with measuring devices.

Fig. 10 Chip photograph of the inductorless VCO

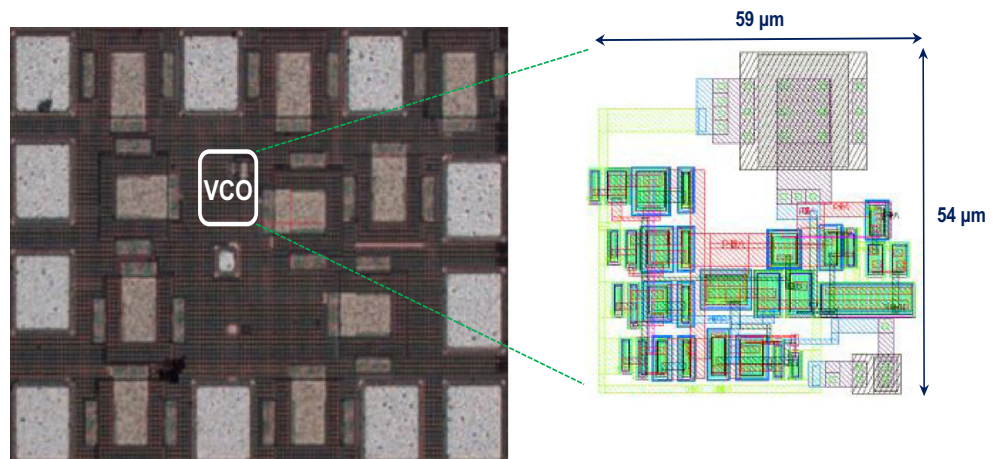


Table 1 VCO performances under PVT variations

Vctrl	PVT corners	Frequency (GHz)	Power (mW)	Phase noise at 1 MHz (dBc/Hz)
[0010]	TT; 27 °C	1.29	3.77	−86.73
	FF; −40 °C	1.64	3.9	−84.45
	SS, 120 °C	1.5	3.65	−80.71
[0111]	TT; 27 °C	2.05	4.09	−82.62
	FF; −40 °C	2.67	4.38	−79.21
	SS, 120 °C	1.75	3.86	−82.53
[1110]	TT; 27 °C	2.23	4.24	−81.7
	FF; −40 °C	2.9	4.6	−77.4
	SS, 120 °C	1.9	4	−80.72

It is essential to verify the VCO stability. Thus, it must be studied under various PVT (process, voltage, temperature) conditions. The obtained results, for different control voltages, are summarized in Table 1. It can be seen that the oscillation is maintained even in the worst case. For example, in the case of $V_{ctrl} = [0010]$, it can be seen that the variations of frequency, phase noise, and power consumption are almost 16%, 3%, and 6% respectively compared with the typical condition.

Since both process tolerances and component mismatch truncate Gaussian probability distribution functions, it is necessary to investigate statistical simulations. In our application, Monte Carlo simulations can be applied to verify the probability distribution of the oscillation frequency with certain process tolerances and a resultant component mismatch. Monte Carlo simulations have been performed with Spectre-RF simulator of Cadence. The variation analysis concerns process and mismatch

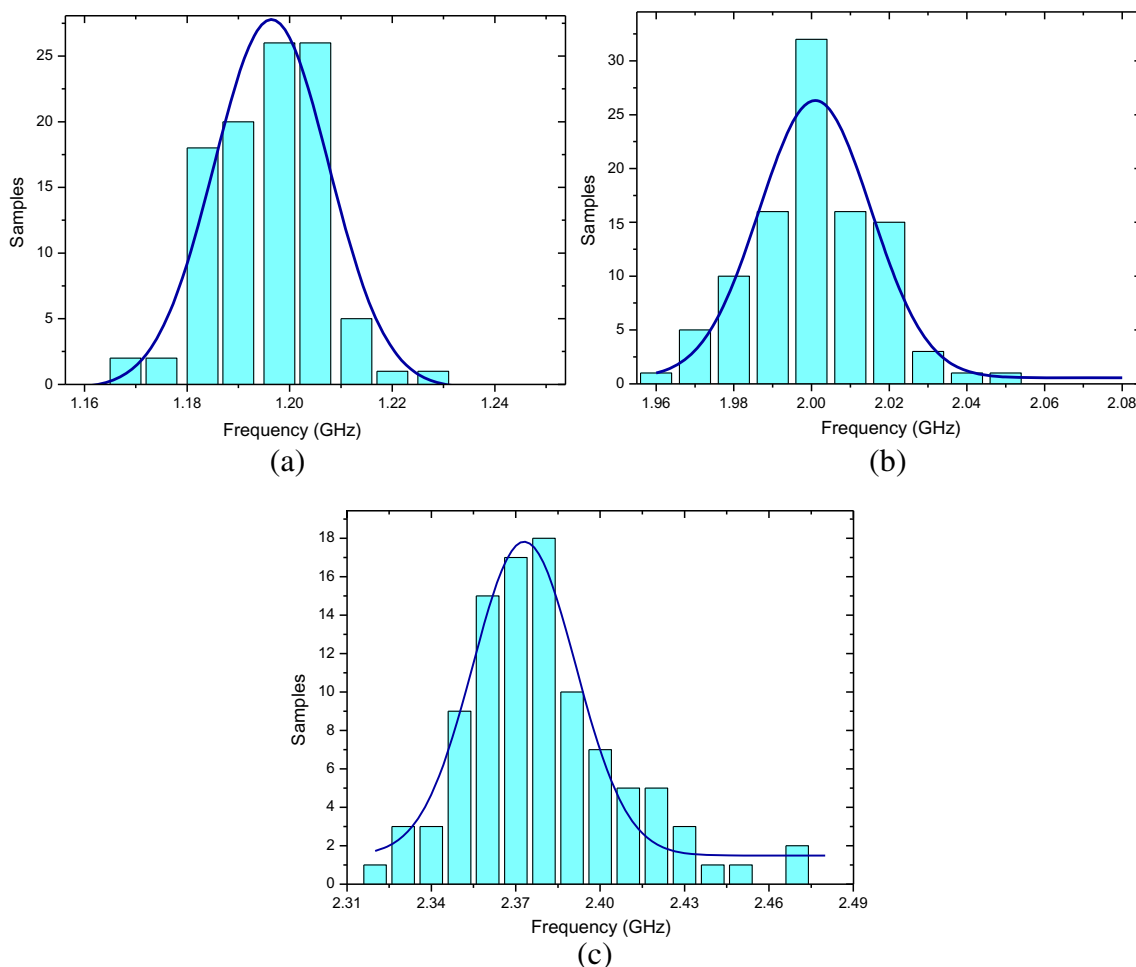
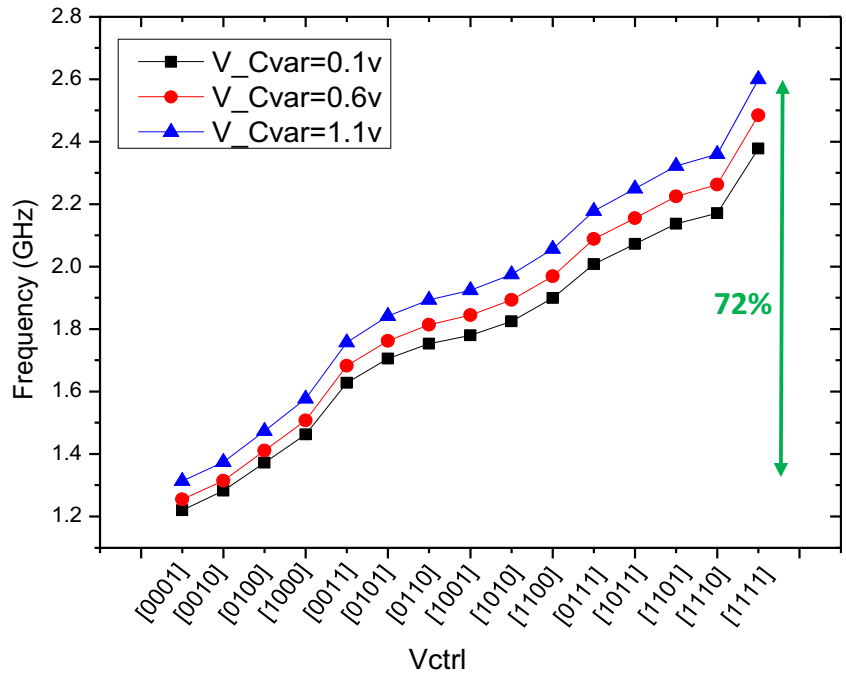


Fig. 11 Monte Carlo simulations: VCO frequency histogram for (a) $V_{ctrl} = [0010]$ ($f_{vco} = 1.2$ GHz), (b) $V_{ctrl} = [0111]$ ($f_{vco} = 2$ GHz), and (c) $V_{ctrl} = [1110]$ ($f_{vco} = 2.3$ GHz)

Fig. 12 VCO frequency versus V_{ctrl} and varactor variations



variations of the components corners, in 130-nm CMOS technology, on the oscillator frequency band.

Monte Carlo simulations of the proposed tunable VCO are given for 100 iterations. Results of three different V_{ctrl} values (the same values used in Table 1) are depicted in Fig. 11. They are expressed as frequency of occurrence histogram for different intervals of the oscillation frequency f_{vco} . Histograms are fitted with Gaussian function to extract probabilities statistics.

It can be seen, in the case of $V_{ctrl} = [0010]$, that 95% of the occurrences have the oscillation frequency in the required

range with a mean value equal to 2 GHz and a σ of 0.014 (cf. Fig. 11(b)).

In the case of $V_{ctrl} = [0010]$ and $[0111]$, there are 90% of samples in the desired band with a mean value equal to 1.119 GHz and 2.37 GHz, respectively. These simulations depict also a maximum degradation of f_{vco} by roughly 100 MHz for minimal and maximal frequencies in the VCO's tuning band.

The results demonstrate that the performance parameter sweep is stable within a suitable range.

Fig. 13 Phase noise and power consumption of the VCO versus frequency

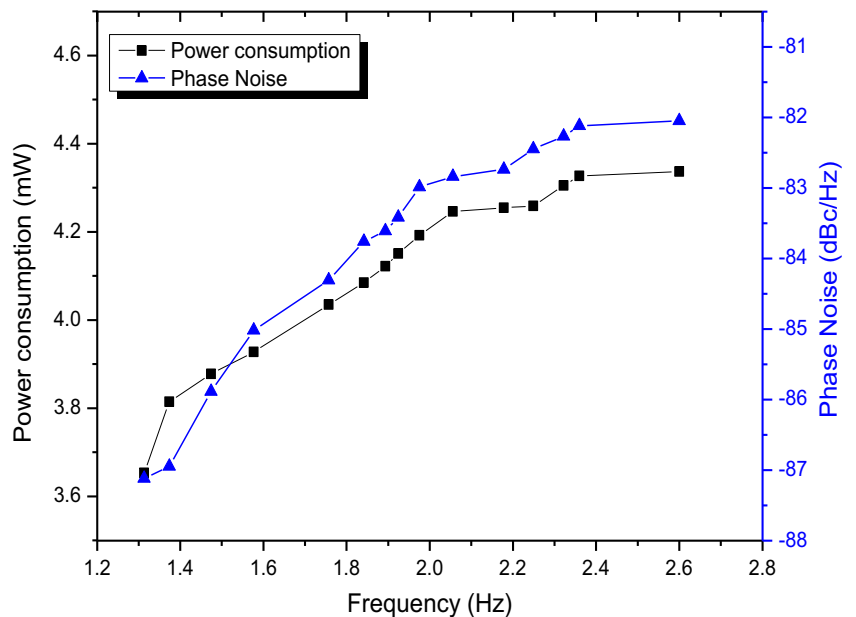


Table 2 Performance comparison of inductorless VCOs

Ref.	Process (nm)	Freq. range (GHz)	Power (mW)	Phase noise (dBc/Hz)	Area (mm ²)	FOM (dBc/Hz)
[8]	180	0.6~7.2	41~49	-86 to 110	0.51 ^a	-149
[10]	180	1.32~2.15	28	-86	-	-138
[11]	180	1.13~2.67	2.2~13	-82.8 to -92.2	0.029	-149
[12]	180	0.55~3.8	11.9	-78 to -89	-	-136
[13]	180	0.1~2.5	16.27	-80 to -93	0.0096	-135
This work	130	1.22~2.6	3.6~4.3	-82 to -87	0.0031	-151

^a With pads

Moreover, the implemented reconfigurable VCO achieves a wide frequency tuning range from 1.22 to 2.6 GHz when changing the control voltages, as shown in Fig. 12. It can be seen that the input digital word V_{ctrl} allows a coarse frequency tuning of 72% while the varactor voltage V_{Cvar} concedes fine tuning of almost 150 MHz. It means that as V_{ctrl} increases, different frequency bands are covered and, as V_{Cvar} sweeps, each standard bandwidth is provided. Note that the frequency tuning range can be increased by using MOS varactors instead of diode varactors and by simply rising the number of inverters in the proposed active inductor.

Figure 13 depicts the obtained phase noise and power consumption of the VCO when tuning the active inductor for the different frequency bands. The phase noise varies between -82 and -87 dBc/Hz at 1 MHz offset from the carrier frequency, which is relatively good for low data rate standards, but still perfectible. This is due to the large number of transistors used in this circuit. The obtained mean DC power is around 4 mW from 1.1-V supply for the different control voltages combinations.

The VCO performances are summarized in Table 2 and is compared with similar previously published works. We have used the figure of merit (FOM), derived from the ITRS reports [9], and defined as

$$FOM = L\{\Delta f\} + 10\log(P_{DC}(mW)) - 20\log\left(\frac{f_{osc}}{f_{offset}}\right) \quad (6)$$

where $L\{\Delta f\}$ represents the phase noise at the offset frequency (f_{offset}) from the oscillation frequency f_{osc} and P_{DC} is the DC power consumption in mW.

It can be noted that interesting performances have been achieved in terms of low power consumption and small area occupation. That makes our circuit suitable for low-cost and low-power IoT applications. A wide frequency tuning range is also obtained while achieving a comparable phase noise with other works. In addition, the peak-to-peak magnitude of the output signal and the setup time of the VCO are almost

constant around 400 mV and 20 ns respectively for the different control voltages.

5 Conclusion

Design and implementation of an inductorless reconfigurable VCO are presented. The proposed topology, suited for highly integrated multistandard radio receivers, achieves wide frequency tuning range of 72% from 1.22 to 2.6 GHz. The VCO uses CMOS digitally controlled inverters in the active inductor and a varactor for coarse and fine frequency tuning respectively. It displays low-power consumption with an active die area of only 0.0031 μm^2 . That makes the proposed design suitable for IoT applications and wireless multistandard systems.

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