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A Novel High Linear CMOS Fully Integrated PA for the Design of Zigbee Transmitters

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Abstract This paper describes a 863–870-MHz transmitter for wireless sensor applications. The fully integrated designed circuit is based on AMS 0.35-μm CMOS standard technology. The transmitter presented is composed by four stages: quadrature voltage-controlled ring oscillator (QVCO) controlled by a voltage (V_{CTRL}), two passive switch mixers, two combiners (a substractor and an adder), and a novel high linear power amplifier (PA). Combiners and the PA has the distinction of being based on CMOS inverter circuit. The post-layout simulation of the fully differential transmitter, at the desired oscillation frequency and under a supply voltage of 3.3 V, shows that proposed circuits satisfy specifications desired especially the output power level and PA linearity.

Keywords Fully integrated PA · Fully differential · CMOS technology · High linearity · CMOS inverter

1 Introduction

With the increasing demand for security, reliability, and autonomy for wireless sensor network (WSN) applications, low-power and low-cost wireless sensor based on highly integrated circuits are needed. The transmitter was designed for a fully integrated RF autonomous sensor for typical applications such as home automation and automatic meter reading. These sensors must meet some severe requirements such as low power consumption (to extend battery lifetime to more than 5 years), small physical size, and low unit cost [1].

In order to achieve these requirements, cost-effective CMOS technology, which enables development of true system-on-chips (SoCs), and the ZigBee standard for wireless connectivity were used [1].

The direct-conversion transmitter is designed for binary frequency-shift keying modulation, communicating a maximum data rate of 20 kb/s. This transmitter architecture requires a minimum of RF section and no image-reject filter [2]. It uses I/Q modulator and performs frequency translation in one step as shown in Fig. 1.

The typical direct-conversion transmitter presented in Fig. 1 operates as follows: the digital FSK modulator modulates the data and synthesizes, in quadrature outputs, complex frequency-hopped spread-spectrum (FHSS) base band signals. The modulator is based on direct-digital frequency synthesizer (DDFS) [3]. Then, a fixed-frequency oscillator, generating a set of four phases LO signals in quadrature with each other, up converts these outputs to the 863–870-MHz band in a single-sideband mixer.

In fact, either the upper or the lower sideband is selected, with an oscillator at 866.5 MHz in the center of the RF band, the instantaneous carrier frequency will be placed anywhere in the band. So, the output frequency of the modulator needs only to span from 0 to 3.5 MHz to cover the ISM range of 866.5 ± 3.5 MHz and so the 7 MHz bandwidth ISM band [3]. After up conversion, a fully differential power amplifier (PA) drives the antenna with the modulated hopped carrier and suppresses out-of-band signals at the transmitter output.

This method of quadrature modulation has the advantage of reducing intermodulation interferences caused by a continuous carrier near the modulation sidebands. In

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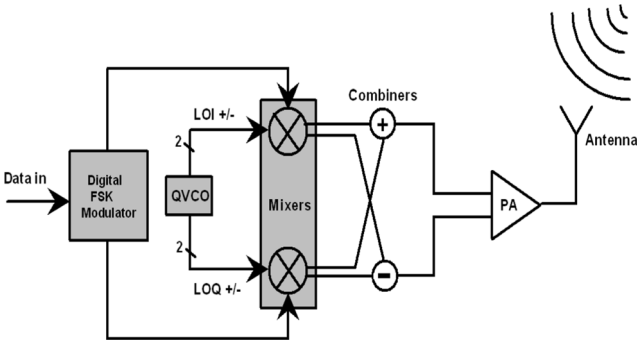

Fig. 1 The direct-conversion wireless sensor transmitter architecture

fact, the two passive mixer outputs are summed using combiners to add in-phase components and reject quadrature components. The result (without additional filtering) is a suppressed-carrier, single-sideband output voltage at a frequency that is either the sum or difference of the LO and baseband signals.

On the other side, the remnants of the LO and opposing sideband are suppressed. Since ZigBee is a low-performance standard, there is no severe restrictions for noise and sensitivity. However, the design restriction on power consumption and die area may impact design choices and performance. These issues are targeted in this paper. The result is a quadrature voltage-controlled ring oscillator (QVCO) and passive mixer design that combines excellent performances with a low power consumption and area occupation.

The rest of the paper is organized as follows: Section 2 presents the design of the proposed QVCO. In Section 3, the circuit design of passive mixer is presented. Section 4 presents the new combiner's architecture based on CMOS inverters. The novel PA architecture is detailed in Section 5. Post-layout simulation results are presented in Section 6. Finally, the conclusion is given in Section 7.

2 QVCO Design

2.1 The QVCO Architecture

The designed QVCO is fully integrated and must generate the center frequency of the 863–870-MHz ISM band. The ring fully differential proposed QVCO is based on four cascaded identical delay cells. Although ring oscillators present a relatively high phase noise, they usually have a wider oscillation frequency range, smaller die size, and lower power consumption. Therefore, ring oscillators are the most used for integration [4].

This work aims at developing an oscillator for a fully differential direct-conversion transmitter for a wireless sensor. So besides the low power consumption, lower phase noise, and smaller die size, the integrated oscillator must provide a large frequency tuning range, quadrature outputs, and current consumption decreasing with lower oscillation frequency without affecting phase noise performance.

There are some known techniques to generate quadrature signals such as frequency dividers and RC-phase shifters [5]. The technique of cross-coupled cells used in this design provides lower power consumption with a very high voltage swing, which eases the design of circuits connected to the oscillator. But, to produce quadrature outputs, a ring needs an even number of stages which has a stable operating point and does not oscillate. To overcome this problem, the solution addressed in this paper is to cross connect the output of one stage to the input of the other one [6].

Block diagram of the realized QVCO is shown in Fig. 2. To fulfill the Barkhausen criterion imposed for getting oscillations, phase offset between the differential outputs of identical delay cells has to be ±90°, and the last cell outputs have to be inverted. In fact, each delay cell is connected to the next stage in common phase while the latest cell is connected to the first one in opposite phase. This gives 180° difference in phase from QVCO outputs to QCVO inputs, and so the four delay cells synchronize in a way that the output signals differ 90° in phase.

2.2 Proposed Delay Cell

The basic structure of each cell is based on two NMOS transistors M_1 and M_2 controlled by the gate voltage of two other cross-coupled p-channel metal-oxide semiconductor (PMOS) transistors M_3 and M_4 forming a differential pair with positive feedback (Fig. 2). The voltage V_{CTRL} controls the output frequency of the structure by controllable PMOS transistors (M_5 and M_6). The polarization of the differential structure is provided by a polysilicon resistor.

The use of this resistance for the differential pair, avoids the use of current mirrors, and consequently additional transistors, which considerably minimize the circuit surface. This also enhances the phase noise performance. In fact, as detailed in [7], the current source transistor is responsible for injecting flicker noise at the harmonic frequencies of the carrier frequency to the cross-coupled transistors and hence, degrades the phase noise performance (Fig. 3).

The oscillation frequency of N stages ring oscillator is equal to $2NT_d^{-1}$, where T_d is the signal delay of each stage [2]. The oscillation frequency of the oscillator is given by the following equation:

$$F_{osc} \approx \left(2N \left[r_{03} // r_{01} // \left(\lambda K_p \frac{W}{L} \right)_5 \left((V_{CTRL} - (V_{DD} + V_T))^2 \right) \right)^{-1} \right] C_L \Bigg)^{-1} \quad (1)$$

where r_{0J} is the drain-source resistance of transistor M_J in saturate mode of operation [7]. C_L is the total output capacitance. The parameters λ, V_T, W, and L are respectively the channel length modulation factor, the threshold voltage, the

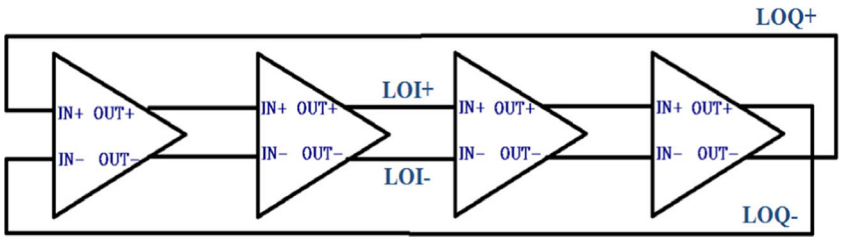

Fig. 2 Block diagram showing for identical delay cells coupled in a QVCO loop

width and length of transistors. K_P is a process parameter proportional to the product of the carrier mobility and a capacitance per unit area. As mentioned by the last equation, the oscillation frequency of this design can be simply tuned by controlling the channel conductance of transistors M_5 and M_6 via the voltage V_{CTRL}.

3 Passive Mixer Design

Although there are some drawbacks in passive mixer such as need of a large voltage drive to achieve full on/off switching, the low gain and the high LO-RF and RF-IF feed through caused by the coupling through the gate-to-source capacitor, the CMOS passive switching mixer was chosen because it has an excellent linearity performance [8].

Furthermore, it uses switches to perform the mixing operation and allows low power operation to be achieved since no bias current is required. This property has a great advantage for direct-conversion transmitters. Due to the perfect switching property of CMOS circuits, a high-performance mixer that is based on switching can be realized by CMOS transistors. Figure 4 shows the simplified circuit diagram of the designed CMOS passive mixers.

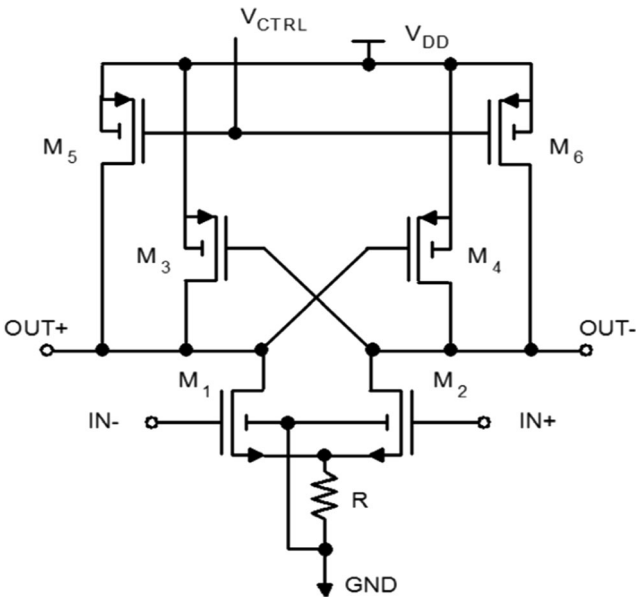

Fig. 3 Proposed delay cell implementation

There are four transistors driven by an anti-phase signal. Only two transistors which are driven by the same phase signal are on at the same time. The perfect switching property holds for the assumption of a sufficiently large input LO+ (or LO−) being used to fully turn on or off the transistors. Thus, to avoid the switch charge injection, eight dummy switches that capture the charge released by the turning-off switch and release the charge required to create the channel in the turning-on switch were added for each mixer. In this case, the sign inversion is accomplished simply by alternating the signal path using a clock LO+, and its counter phase LO−.

The charge injection, as the switch MOS changes state, is a major contributor to dynamic offset [9]. For fast switching clock waveforms, the channel charge will split equally to the source and drain terminals; hence, to compensate for the charge injection, half-sized dummy MOS with shorted drain-source are inserted in the signal path.

4 Combiners Design

This work deals with the design of new combiners based on CMOS classical inverters operating in transconductance mode. The proposed combiner topologies are shown in Figs. 5 and 6, the substractor and the adder, respectively. Each circuit uses 10 CMOS inverters.

Since circuits are fully differential, they are formed by two symmetrical branches, each of which contains four inverter

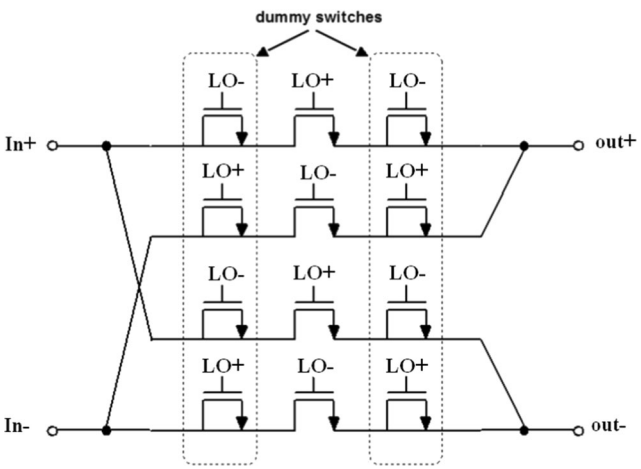

Fig. 4 Passive switching CMOS mixer architecture

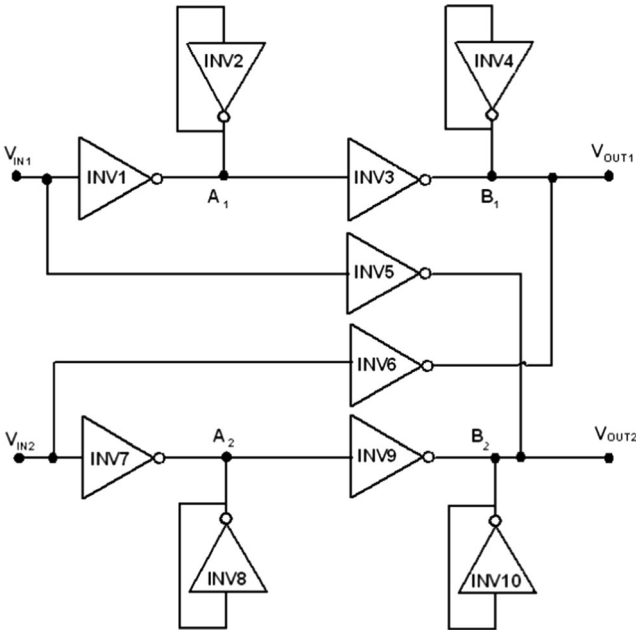

Fig. 5 Proposed substractor-based CMOS inverters

cells. Furthermore, the two branches are connected by two other inverters, each connected between the branch input and the output of the other branch as shown in Figs. 5 and 6.

All inverters are voltage supplied at V_{DD} and set in order to obtain a voltage transition around $V_{IN} = V_{OUT} = V_{DD}/2$. Thus, the inverters are in T-mode, providing a relatively high linearity compared to its digital mode operation [10] and simulate at small amplitude a transconductance. The T-mode is presented with more details in [11].

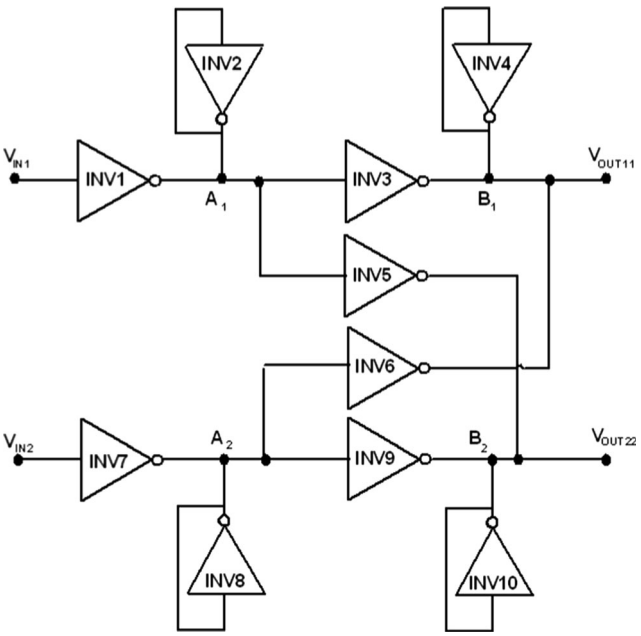

Fig. 6 Proposed adder-based CMOS inverters

Considering the transconductance g_{mi} of each inverter INVi and choosing all g_{mi} equal, the expression of the outputs V_{OUT1}, V_{OUT2}, V_{OUT11}, and V_{OUT22} can be easily extracted as explained in [12].

Inverters INV2 and INV4 in each path (respectively INV8 and INV10) are shunted as resistors by connecting the output and the input nodes. The values of these resistors are $1/g_{m2}$ and $1/g_{m4}$ (respectively $1/g_{m8}$ and $1/g_{m10}$) [11].

By reasoning in a similar way, we obtain the following:

$$V_{OUT1} = V_{IN1} - V_{IN2} \text{ and } (V_{OUT2} = V_{IN2} - V_{IN1}).$$
$$V_{OUT11} = V_{IN1} + V_{IN2} (\text{and } V_{OUT22} = V_{IN2} + V_{IN1}).$$

5 PA Novel Architecture

The PA design must take into consideration and simultaneously several criteria. Indeed, PA, placed just before the antenna, must convert a DC power into RF power amplified and transmitted by the antenna to enable it to achieve maximum distances. The PA must, therefore, present in addition to the sufficient power output, better efficiency, gain, linearity, stability and should be able to operate at low supply voltages. All these parameters govern the PA design during all stages. So, PA is the most critical element of the transmitter because it is the component that consumes the most power.

PAs may be categorized in several ways, depending on different criteria. Usually, they are classified according to their circuit configuration and operating conditions into different classes, from class A to class S. We studied a number of these monolithic structure amplifiers, but it is clear that the realization of a PA following specifications desired for our application remains difficult.

5.1 The PA Design Challenge

The study of PA classes showed that the linearity and efficiency cannot be achieved simultaneously. Therefore, it is necessary to determine priority between these two criteria depending on the application. In fact, classes A, B, or AB allow obtaining a high power level. For these classes, the drain voltage is maintained sinusoidal by the use of a selective load circuit at the operating frequency. Indeed, these classes are most used when linear amplification is required.

Unfortunately, the switched classes (D to S) having some good efficiency performances cannot have a good linearity. When using CMOS technology without any off-chip components or wire-bond inductors for the fully integrated PA for our application, several problems arise.

For example, to illustrate these problems, a CMOS transistor can be used to design, switching or linear-mode amplifiers up to high frequencies. Unfortunately, the low breakdown transistor voltage limits the maximum voltage swing at their

drains. These voltage swing limitations make a large impedance transformation necessary in order to deliver a high output power to 50 Ω loads.

Another issue is the drain impedance control at the fundamental frequency and at the harmonic frequencies taking into account the transistor parasitic capacitances. To achieve the desired harmonic suppressions at the output and to improve the drain wave shaping for better power efficiency, an impedance control is required even in class-A operation [13].

However, it is known that the on-chip CMOS inductor presents a very low-quality factor and occupies a large area on the silicon chip compared to transistors.

Since the state of the art shows the ineffectiveness of conventional architectures to provide power and linearity on CMOS fully integrated technology, a new PA structure was developed and is presented in the next section.

5.2 The PA Proposed Architecture

We propose a novel PA structure based on the CMOS inverter, as shown in Fig. 7. The completely differential structure developed is formed essentially by the two identical amplification stages (Ampli 1 and Ampli 2), the amplifier, the reference voltage, and the buffer. Figure 8 shows the amplification stage. In the amplifier structure transistors M1 and M2 form a CMOS inverter characterized by the transconductance gain g_{m1}. Transistors M3 and M4 form a shorted inverter and realize an active resistance having a value of $1/g_{m2}$. Thus, the amplifier achives the following voltage gain:

$$G_V = \frac{\mathrm{OUT}}{\mathrm{IN}} = \frac{g_{m1}}{g_{m2}} \tag{2}$$

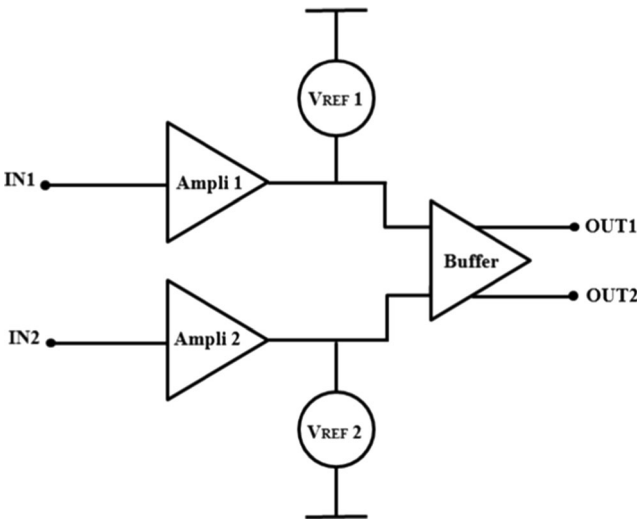

Fig. 7 Novel PA developed structure

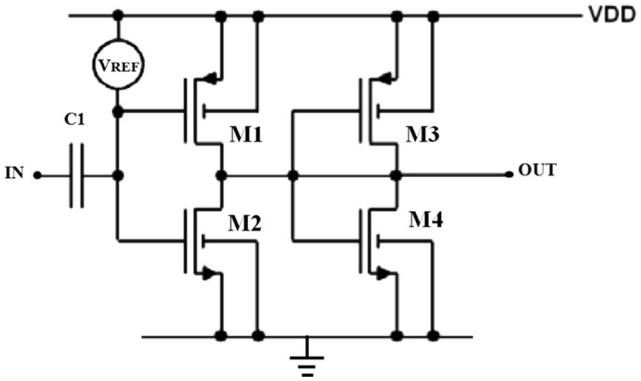

Fig. 8 Amplifier structure

Transistors of the amplifier stage have been sized to meet the trade-off low power consumption/high output resistance. In fact, we are interested in having the lowest current consumption without increasing the output resistance of the output amplifier stage, as explained previously.

Amplifiers (Ampli 1 and Ampli 2) are polarized via the reference voltage V_{REF} generated by the circuit shown in Fig. 9. The bias circuit V_{REF} (the same for V_{REF1} and V_{REF2}) consists of two PMOS transistors (M22 and M23) connected to the input of a shorted CMOS inverter [14].

The two identical PMOS have substrate connected to the voltage V_{DD} and gates connected to ground. The transistors M24 and M25 realize an inverter configured as an active resistance. This process allows fixing the value of the bias voltage close to half of the supply voltage, in our case $V_{REF} = 1.6$ V. The transistors M22 and M23 have a gate length of 1 μm and thus realize a resistance equivalent value of approximately 8.2 MΩ. This circuit allows us to make a correct inverters' polarization at V_{REF} output, around half of the supply voltage without consuming power.

The capacitor C_1 (Fig. 8) performs a static polarization coupling to connect several stages without disturbing this

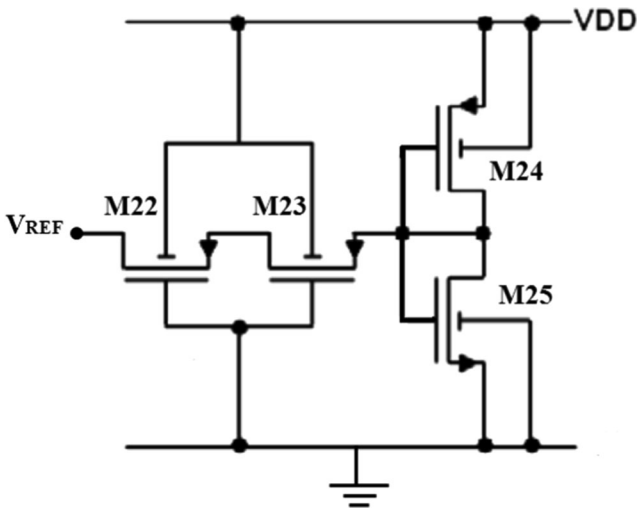

Fig. 9 Reference voltage circuit

polarization. However, it causes the appearance of a low cut-off frequency related to the value of C_1 (1 pF) and the value of the equivalent resistance of the reference voltage circuit.

The last PA stage is the buffer which aims to realize the interface between the PA and the antenna. It must be linear and have enough gain to satisfy application specifications. Instead of using a second amplifier stage, this stage is based on the differential common source structure presented in Fig. 10. It provides simultaneously improved linearity and produces the necessary gain with acceptable power consumption. In order to maintain the gain of the previous amplifier PA stage, the buffer must have the lowest input capacitance as possible [15].

The simplified expression of the buffer stage gain is given by the following equation [15]:

$$G_{\text{Buffer}} = \frac{g_{m12}+g_{m13}}{g_{m12}+g_{mb12}+\frac{1}{r_{012}}+\frac{1}{r_{013}}+\frac{1}{Z_L}} \quad (3)$$

where g_{mb} is the transistor's transconductance to the substrate, r_0 their output impedance, and Z_L the impedance load.

This gain can be considered as a function of the ratio g_{m3}/g_{m1}.

To have gain higher than 1, we have to respect this condition $g_{m13} > g_{m12}$. However, the compensation of current variation of the transistor M12 (M14) by the transistor M15 (M13) requires that transconductances of M12 and M13 were equal. This condition is not in concordance with the Eq. 3. Therefore, it is difficult to maintain a very good linearity with a high gain. The input buffer capacitance is high. Indeed, for example, at the IN_M input, the capacitor C_1 in series with the C_{GS} of transistor M13. The output impedance Z_{OUT} of this stage is given by the following:

$$Z_{OUT} = \left(\frac{1}{g_{m12}+g_{mb12}+{}^{1}/_{r_{012}}}\right)//r_{013} \quad (4)$$

Table 1 presents size parameters of the optimized PA architecture. These sizes were calculated using equations already presented and taking into account the optimization of the output power and the power consumption. The bias current value was 5.4 mA. The polarization of gates of input transistors is effected via the voltage reference circuit which is equivalent to a resistance of high value.

Table 1 PA transistors sizes

Component	Sizes (W/L) [μm]
M1	90/1
M2	30/1
M3	3/1
M4	1/1
M12, M14	150/0.5
M13, M15	90/0.5
M22, M23	0.5/1
M24	1.5/9
M25	0.5/9
C_1	35/35

6 Post-layout Simulation

The circuit was fabricated in a 0.35-μm CMOS standard process with four metal layers [16]. It operates under a 3.3 V supply voltage. In order to minimize phase and gain errors,

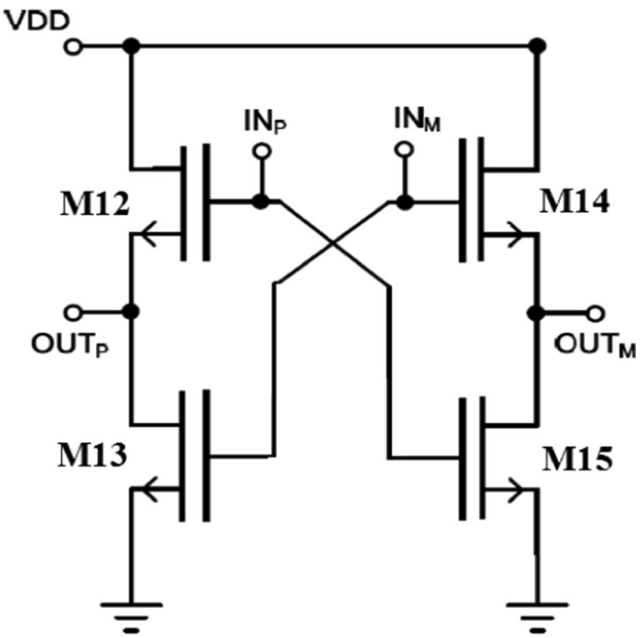

Fig. 10 The buffer architecture

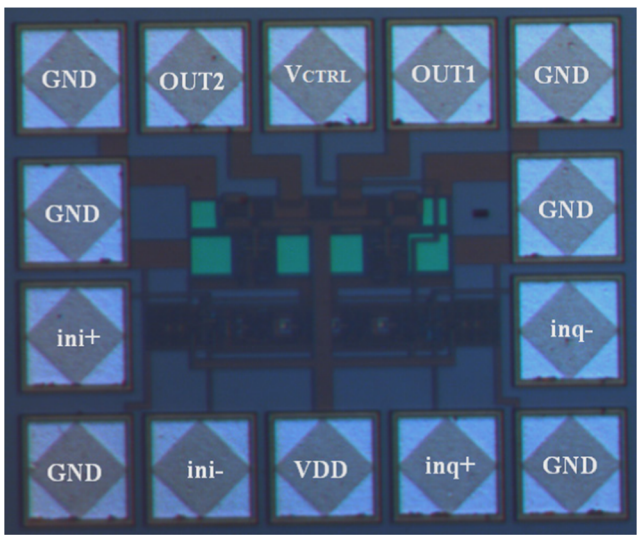

Fig. 11 Die microphotograph of the transmitter prototype

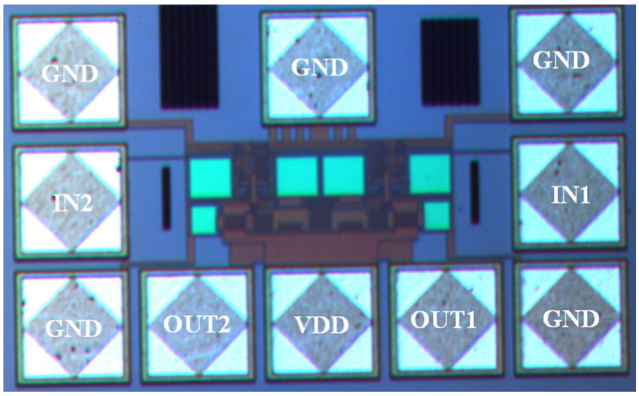

Fig. 12 Die microphotograph of the PA

the layout is as symmetrical as possible. Furthermore, the layout of our circuits has been accomplished by taking into consideration the differential character of the transmitter. To reduce the effect of eventual mismatches, differential blocks were used such as differential pairs or the amplifier stage. Furthermore, a very strict attention was carried out.

For some structures, as the PA, cancelation of the input offset can be accomplished by making the gain of the amplifier as large as possible. Furthermore, to reduce the value of the amplifier imperfection reflected to the input of the amplifier, transistors are oriented in the same direction.

In addition, the voltage reference circuit used at the input and the output of the amplifier stage has the advantage of keeping a constant voltage which is independent of the variation in the manufacturing process.

The transmitter chip micrograph is shown in Fig. 11. The chip size is about 516 μm × 310 μm including testing pads. Since the transmitter circuit is very small, we did not have the ability to place a test pad for each input or output signal. So we decided to make sub-circuits for characterizing the most important blocks separately as QVCO and PA.

Circuits were simulated after the extraction of the layout of the circuit with input and output pads taking into account

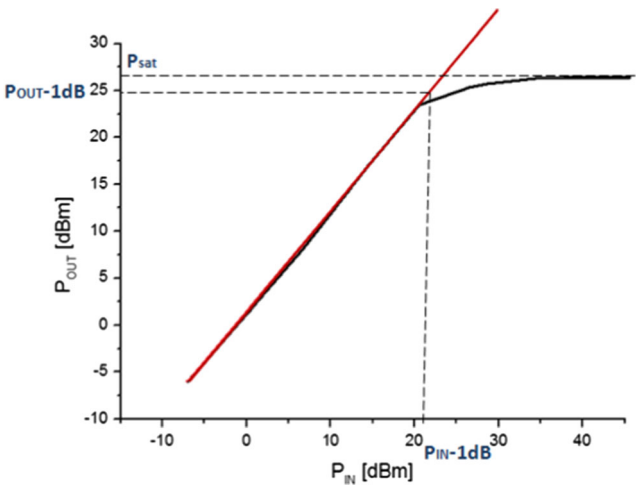

Fig. 13 Linearity curve of the PA (P_{out} as a function of P_{in})

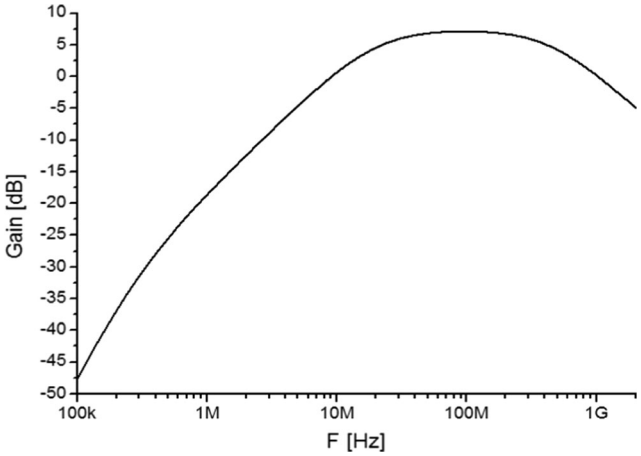

Fig. 14 Conversion gain curve of the PA

resistive and capacitive parasites. Then, the post-layout simulations were performed by applying a load to each output. This charge, formed by a 50 Ω resistor in parallel with a capacity of 10 pF, models cables and materials used in the tests. Post-layout simulation was done to ensure that even with process variations, circuits keep their performances.

The sub-circuit characterizing the PA is shown in Fig. 12; it has an area of 515 μm × 430 μm and 10 pads for two inputs (IN1 and IN2) and two outputs (OUT1 and OUT2).

The post-layout simulation results of the PA are illustrated by the following figures. The circuit consumes 18.95 mA. Figure 13 shows the output power P_{out} plotted as a function of the input power P_{in}. The −1 dB compression point is obtained for an input power of 21 dBm and an output power of 25 dBm.

The saturation power is P_{sat} = 27 dBm. These results reflect good performance in terms of linearity. The conversion gain (Fig. 14.), for the requested frequency band, is more than 4 dB and the maximum value is close to 8 dB. The transient response of the PA is shown in Fig. 15.

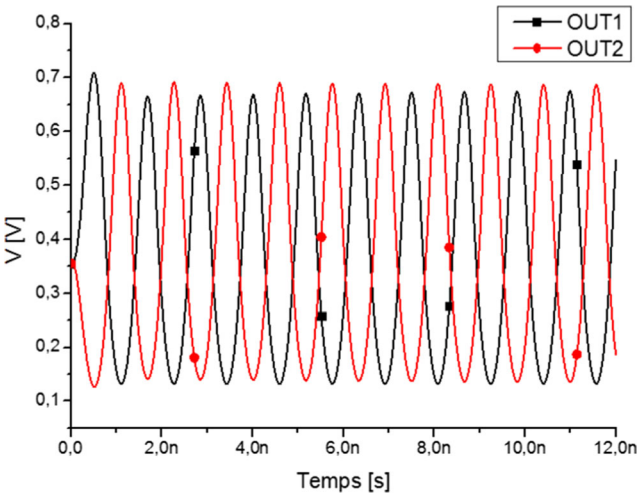

Fig. 15 The transient response curve of the PA

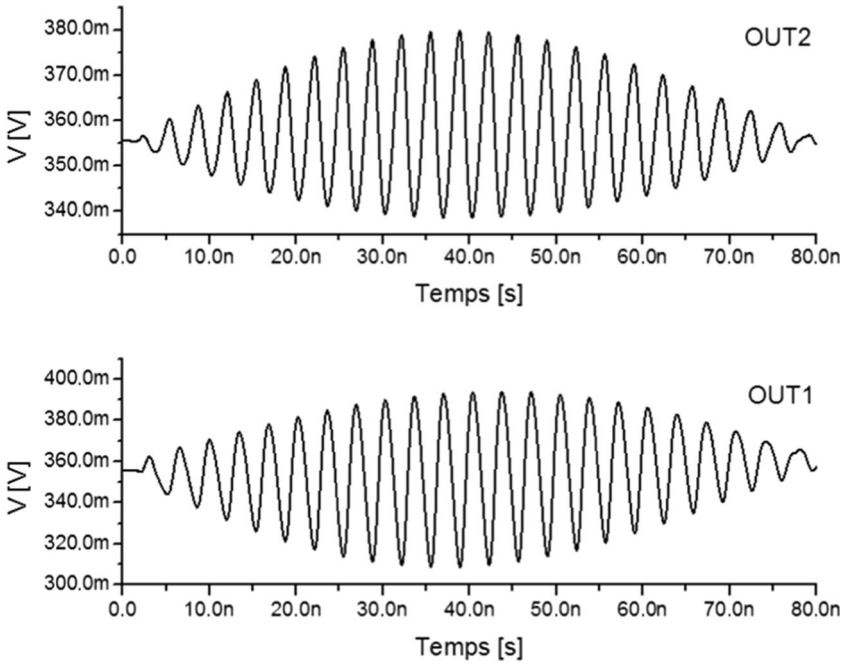

Fig. 16 The transient response of the transmitter (OUT1 and OUT2)

The PA circuit, in Fig. 11, comprises four pads for quadrature inputs which are respectively ini+, ini−, inq+, and inq−, two pads for outputs OUT1 and OUT2, the V_{CTRL} pad for the voltage controlling the QVCO and the supply voltage pad V_{DD}. The rest of the pads is dedicated to the ground. The DC simulation results give the value of the circuit consumption current 26.76 mA. Transient and frequency analysis are illustrated by Figs. 16 and 17. As an example of post-layout simulation results: for input signals having an amplitude of 200 mV, a frequency of 8.25 MHz, and a control voltage of 1.7 V, the QVCO oscillation frequency is about 297 MHz. Thus, outputs OUT1 and OUT2 are respectively at 288.75 and 305.25 MHz. To more characterize the designed transmitter, in Table 2, our transmitter is compared to others operating in similar frequency bands and used in various applications.

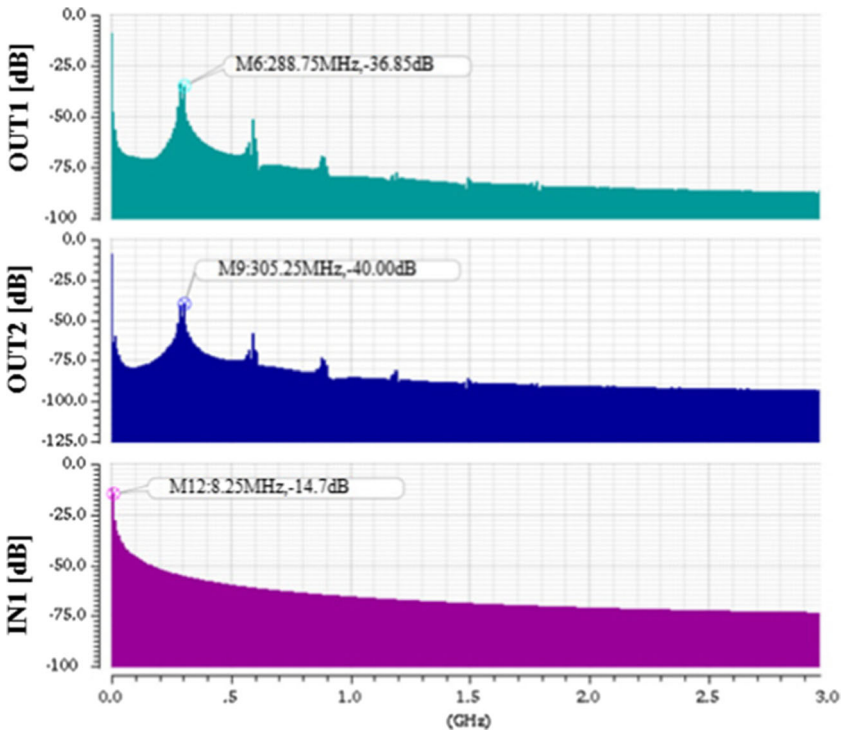

Fig. 17 The spectrum curve at transmitter outputs (OUT1 and OUT2)

Table 2 Comparison with other transmitters

	Application	Frequency [MHz]	Technology	Transmitter consumption	Area [mm^2]	Output power [dBm]
[17]	Zigbee TX	900	0.18-µm CMOS	14 mA at 1.8 V (−VCO)	0.8 × 1.5	0
[18]	GSM TX	900	0.35-µm BiCMOS	17.4mA at 2.5V (−PA, VCO 13 mA)	1.7 × 2.1	12.3
[19]	RFID RX/TX	900	0.35-µm BiCMOS	300m A at 2.5 V (RX + TX)	3 × 3	17.5
[20]	RX/TX	915	0.18-µm CMOS	22.5 mA at 1.8 V (QVCO 5 mA)	10	0
[21]	FSK/ASK RX/TX	868	0.25-µm CMOS	20 mA at 3 V	–	10
[22]	Polar TX	GSM/EDGE	65-nm CMOS	28 mA/32 mA at 1.8 V	0.7	3/1
		WCDMA		40 mA at 1.8 V		0
[23]	8-Band CMOS RX/TX	WCDMA	130-nm CMOS	566.4 mW	6.5 × 6.5	14.6
		GSM/EDGE		407.4 mW		7.0 (GMSK) 3.5 (8-PSK)
[24]	UHF RFID RX/TX	860–960	180-nm CMOS	143.4 mA at 1.8 V	18.3	10.4
[25]	UHF RFID RX/TX	902–928	180-nm CMOS	31 mA at 1.8 V (−QVCO)	4.5 × 5.3	4
This work	Zigbee TX	863–870	0.35-µm CMOS	26.8 mA at 3.3 V	0.52 × 0.43	22

The designed transmitter occupies the smaller area compared to those designed in [17, 18] and [22]. It is almost equal to one third of the smaller area although being manufactured using the most recent technology (65 nm).

Compared to the most recent circuit described in [22], the current consumption of our transmitter is lower with a much higher linearity. For the circuits presented in [18] and [19], which have been designed in the same technology, the transmitter in [19] consumes a current of 17.4 mA when the novel transmitter presented in this work consumes (without the PA) 7.85 mA.

With a power consumption of 89 mW, our transmitter is more autonomous than those in [23] and [24] although they operate at lower bias voltages.

Furthermore, this work gives the higher output power of about 22 dBm. Further simulation was done to ensure that even with process variations, the circuit keeps its performances. Therefore, two other cases were considered taking into account worst simulation conditions like the MOS behavior.

The first case (WS) considers that all transistors use the worst case speed condition model. In the second case (WP), all transistors use the worst case power condition model.

Simulation results at these two worst cases prove that the QVCO can always oscillate at required frequency by a simple adjustment of the value of V_{CTRL}. Furthermore, the transmitter has always a gain greater than unity and an output power which exceed always 17 dBm. This verifies the desired specifications for the circuit, despite the slight deterioration in terms of performances.

7 Conclusion

A novel ZigBee fully integrated transmitter operating in the 863–870-MHz ISM band has been presented. The circuit was designed and simulated using a 0.35-µm CMOS standard process. The proposed circuit operates under a 3.3 V supply voltage and is composed by a ring QVCO, two passive switch mixers, two novel combiners, and a novel PA.

Compared to similar transmitters, the design exhibits excellent performances as low power dissipation, high linearity, small area, and output power level. The circuit has a small die area and this has been achieved by avoiding the use of inductors and exploiting polysilicon resistance for the polarization of the QVCO delay cell and by the use of CMOS inverter for combiners and PA architectures.

The future work will be focused on realizing measurement of the circuit to determine real transmitter performances.

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