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Nano-Crossbar Memories Comprising Parallel/Serial Complementary Memristive Switches

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Abstract This work explores anti-serial (anti-parallel) memristive switches—ASMs (APMs)—as potential cross-point elements in nano-crossbar resistive random access memory arrays. The memory operation principles for both device combinations are shown in detail. The effectiveness of these memristive structures to the solution of the parasitic conducting (current sneak paths) problem is presented via an analytical approach which is based on the basic setup of resistive crossbar memories. Simulation results of crossbars of up to 4,096 elements, arranged in quadratic configurations, are conducted. The provided results supplement this comprehensive analysis of APMs and ASMs, outlining their overall performance characteristics and commenting on their applicability to the practical realization of large crossbar memory systems. Finally, a special array topology is applied to an ASM-based crossbar memory. Its performance is compared to the performance of the pure ASM-based memory. The conducted simulations reveal significantly improved read-out voltage margins which further contribute to addressing the parasitic current paths which prevent the reliable operation of memristive crossbar circuit topologies.

Keywords Memristor · Nano-electronics · Crossbar · Current sneak paths · Resistive random access memory

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1 Introduction

Many emerging memory technologies, like phase change memory (PCM) [1] and resistive random access memory (ReRAM) [2, 3], are nowadays being investigated as promising candidates to overcome the scaling limits of the charge-based flash memory. As far as ReRAM is concerned, this type of storage devices is based on two-terminal resistance switching elements called memory resistors (memristors). The memristor is a nonlinear device that exhibits a "pinched" hysteresis loop between current and voltage (I–V), satisfying the Ohm's law with a nonconstant resistance [4]. The existence of the memristor as the fourth fundamental circuit element was predicted by Leon Chua in 1971 via an axiomatic approach based on symmetry and on a missing relationship between the four fundamental circuit variables, namely, current, voltage, charge, and flux linkage [5].

Although it has been almost 6 years since the experimental realization of the first "modern" memristor prototype by Strukov et al. at Hewlett Packard Laboratories [6], many details of the internal memristive mechanisms of the reported materials are still unknown [7]. Nevertheless, recent experimental demonstrations are very encouraging for the potential utilisation of memristors in a variety of emerging applications [8–11]. Among others, such applications mostly include non-volatile memories [12], large scale associative and content-addressable memories [13, 14], as well as new configuration memory cells for FPGAs in embedded applications [15, 16]. Specifically, ReRAM storage elements, i.e. memristors, with scalability down to sub-10 nm, comparable read/write times with present day memories and good retention time projected to >10 years [17], prove up to now to be the most promising solution for future storage systems. Nevertheless, when ReRAMs are implemented in the nano-crossbar geometry [18], parasitic conducting (current sneak paths) disturbs reading operations and makes the use of large sensing circuits

inevitable. Sneak paths are an inherent disadvantage of passive crossbar arrays and significantly limit the size of the grid, i.e. the maximum achieved number of rows and columns [19]. Some of the proposed solutions to this problem include additional nonlinear elements in series with the memristors. Actually, introducing diodes to each cross-point structure appears as one of the most attractive candidates [20], but diodes with sufficiently high forward current density and stable unipolar memristive elements are still under investigation. Moreover, adding diodes to the array will increase the delay of the system by adding capacitive loads, and diode threshold voltages will decrease the output swing [21]. A programming scheme was developed in [22] where parallel current paths were blocked using external diodes at the outside of the array and asymmetric protecting voltages which were applied to the unselected word and bitlines. However, intrinsic current-rectifying characteristic of the cross-point resistance switching elements plays a crucial role in making this approach feasible. Also, using CMOS transistors for gating the memristors will certainly solve the sneak paths problem. On the other hand, this method will ruin the high density of memristive memory, since the size of the CMOS switches is much larger than that of a memristor [23]. Moreover, a cross-point cell structure consisting of one bipolar selector, with nonlinear resistance, and one memristor shows to be able to best utilize the stable bipolar memristive properties while the read process remains non-destructive [24]. However, the reported bipolar selectors so far have limited nonlinearity, only sufficient for small array sizes, and significant improvements on the selector characteristics are needed for high-density crossbar arrays.

Recently, anti-serial memristive switches (ASMs) were proposed as cross-point devices to address interfering current paths between neighbouring memory cells, where each ASM device consists of two memristors connected in series with opposing polarities [25]. However, anti-parallel memristive switches (APMs) have been also fabricated and characterized [26], where each APM comprises two memristors with opposing polarities connected in parallel. Therefore, it was proved that anti-parallel-connected memristors can be effectively combined, and hence, they could be potentially used in memory applications as well. The resulting *I–V* characteristics of both the aforementioned device combinations strongly depend on the parameters of the individual switches. However, their unique feature which appears in simulation and in fabrication testing as well is their symmetric *I–V* curve made out of asymmetric *I–V* curves of single memristors.

In the present work, we discuss the notion of introducing APMs or ASMs as potential cross-point elements in nano-crossbar memory arrays. We present the corresponding memory operation principles for both device combinations according to the switching characteristics that the individual memristive elements may have. Moreover, we compare the effectiveness of these memristive structures to the addressing of the current sneak path problem via an analytical approach which is based on the basic setup of a resistive crossbar memory. Using a memristor device model, developed by the present authors [27], we also include simulation results of crossbar memory arrays with up to 4,096 elements. We provide a comprehensive and comparative presentation between APMs and ASMs, commenting on their overall performance and the most appropriate switching characteristics that the structuring memristors should have in order for their parallel or serial combinations to better fit to memory applications. Finally, we employ a special crossbar topology pattern [28], which introduces insulating junctions inside the grid, and evaluate its impact on the memory read-out voltage margins of ASM-based memories. The presented mathematical analysis, supported with the provided simulation results, constitutes a useful tool for electronic engineers and circuit designers from academia and industry who wish to experiment with such memristive structures in emerging memory applications.

2 Memristor Modelling and Memory Cell Operation Principles

In this section, we analyze the composite behaviour of circuits comprising memristors connected in a serial or a parallel manner; we provide the operation principles for both types of memristive switches when they are used as cross-point storage structures in crossbar memory arrays. Depending on their internal state, their polarity, and the device-specific properties, which are represented by the values of the parameters of the employed model, the simulation results reveal that such compositions of memristors respond in a much unexpected manner. Such response is particularly exploited when memristors are used as memory cells.

In this work, all simulations are conducted using the MATLAB® environment employing a memristor device model which explains memristive behaviour by investigating the occurrence of quantum tunnelling as the primary electronic transport mechanism [27]. More specifically, it is a threshold-type switching model of a two-terminal voltage-controlled electronic device that exhibits memristive behaviour, whose general definition is given by the following equations:

$$I(t) = G(L,t)V_{\mathrm{M}}(t) \tag{1}$$

$$\dot{L} = f(V_{\mathrm{M}}, t). \tag{2}$$

We define as L the tunnel barrier width and also the single state variable of the system, indicating the internal memristor state. G is the conductance of the device and parameters I and V_{M} represent current and applied voltage, respectively. We define

as R_t the tunnelling resistance (memristance) of the device for a certain restricted range of the state variable L. We calculate it using the following equation:

$$R\_t\left(L_{V_M,t}\right) = f_0 \cdot \frac{e^{2L_{V_M,t}}}{L_{V_M,t}} \tag{3}$$

where f_0 is a model fitting parameter. The resistance of such devices as a function of L illustrates an exponential behaviour. Moreover, we developed a heuristic equation which qualitatively gives the response of the tunnel barrier width as a function of the applied voltage. Its mathematical formula follows:

$$L(V_M, t) = L_0 \cdot \left(1 - \frac{m}{r(V_M, t)}\right) \tag{4}$$

where L_0 is the maximum value that $L(V_M, t)$ can attain and m is a fitting parameter that determines the boundaries of the barrier width. By considering tunnelling as the dominant physical mechanism, Eq. (4) introduces the initial as well as the current position of the tunnelling barrier which is limited within two boundary values. This model is based on the assumption that the switching rate of L is small below (fast above) a threshold voltage (V_{SET} or V_{RESET}), which is viewed as the minimum voltage required to impose a change on the physical structure of the device. This assumption is encapsulated in the use of the voltage-dependent function $r(V_M, t)$ whose time derivative, given by the following expression, is slow or fast depending on the applied voltage.

$$\dot{r}(V_M, t) = \begin{cases} a \cdot \dfrac{V_M + V_{th}}{c + |V_M + V_{th}|} & , V_M \in [-V_0, V_{RESET}) \\ b \cdot V_M & , V_M \in [V_{RESET}, V_{SET}] \\ a \cdot \dfrac{V_M - V_{th}}{c + |V_M - V_{th}|} & , V_M \in (V_{SET}, V_0] \end{cases} \tag{5}$$

Several thresholds can be programmed by tuning the shaping parameters of $r(V_M, t)$, namely, a, b, and c. Equation (5) incorporates sigmoid functions in the regions above the voltage thresholds, whereas a linear relation of the applied voltage is used for the region below the thresholds. Parameters a, b, and c are fitting constants that are used to shape the intensity of the state variable dynamics, i.e. the rate of memristance change, with $a >> b$ and $0 < c < 1$. Setting b equal to zero imposes a hard switching behaviour, i.e. there is no state change in the memristor unless a certain voltage threshold is exceeded. Consequently, parameter $r(V_M, t)$ defines both the device dynamics and the corresponding state. Its value is monitored at each time step and maintained within a valid defined range; i.e. in cases when $r < r_{min}$ or $r > r_{max}$, it is set equal to r_{min} or r_{max}, respectively. As a consequence, the device memristance is correspondingly set to R_{ON} or R_{OFF}.

Figure 1 illustrates the response of a single memristor under ac voltage bias according to the used model. Model parameter values are used as given in $\{\alpha, b, c, m, f_o, L_o, V_{RESET}, V_{SET}\} = \{3 \times 10^4, 5, 0.1, 83, 180, 8, -1\ V, 2\ V\}$, and the resulting resistance ratio is set to $R_{OFF}/R_{ON} \approx 10^3$ with $R_{OFF} \approx 2$ MΩ and $R_{ON} \approx 2$ KΩ. We note here that, according to the mathematical formulation of the model, when $\{a, b\} > 0$, then a positive (negative) voltage applied to the top terminal with respect to the bottom terminal, denoted by the black thick line (see inset of Fig. 1 for the corresponding schematic), always tends to decrease (increase) the memristance. In this context, hereinafter we will refer to forward (reversely) polarized memristors as FPMs (RPMs). Single memristors with opposite polarities present a flipped I–V characteristic and generally demonstrate reversed behaviour to the applied signals; in brief, a positive applied voltage tends to SET (RESET) an FPM (RPM) device from OFF to ON (from ON to OFF). Therefore, during a single period of an applied ac voltage, the complementary devices will be likely changing their states in a reciprocal way. The characteristics demonstrated in Fig. 1 will serve as a reference when studying the composite behaviour of APMs and ASMs throughout this paper, under similar applied voltages of the same frequency. Whenever different values are applied to the parameters of the model, it will be clearly stated.

2.1 Anti-Serial Memristive Switch (ASM)

In the anti-serial memristive switch (ASM) concept, a memory cell is formed by two memristors vertically stacked in an anti-serial manner on top of each other. In an individual memristor, logic values '0' and '1' can be represented with high (OFF) and low (ON) resistance states, respectively. However, the unique aspect of ASMs is in using a combination of low and high resistances to represent the aforementioned binary values; i.e. using the following notation to denote the placement of the devices as UPPER/LOWER, then an ON/OFF combination could represent logic '1' and the opposite one, namely, OFF/ON, could respectively represent logic '0'. Since the memristance change behaviour is dependent on the initial state of the devices, their initial memristances should be set to either of the aforementioned boundary value combinations directly after manufacturing by appropriate biasing, prior to further processing.

In the simulation results presented in Fig. 2, an ASM is subjected to a triangular ac voltage sweep of appropriate magnitude (here 5 V) to make sure that the corresponding voltage drop will cause both memristors to change their state. Three different cases are examined, considering switching threshold voltages for both memristive elements set to the following values: (a) $V_{RESET} = -1$ V with $V_{SET} = 2$ V, (b) $|V_{RESET}| = |V_{SET}| = 2\ V$, and (c) $V_{RESET} = -2$ V with $V_{SET} = 1$ V. In

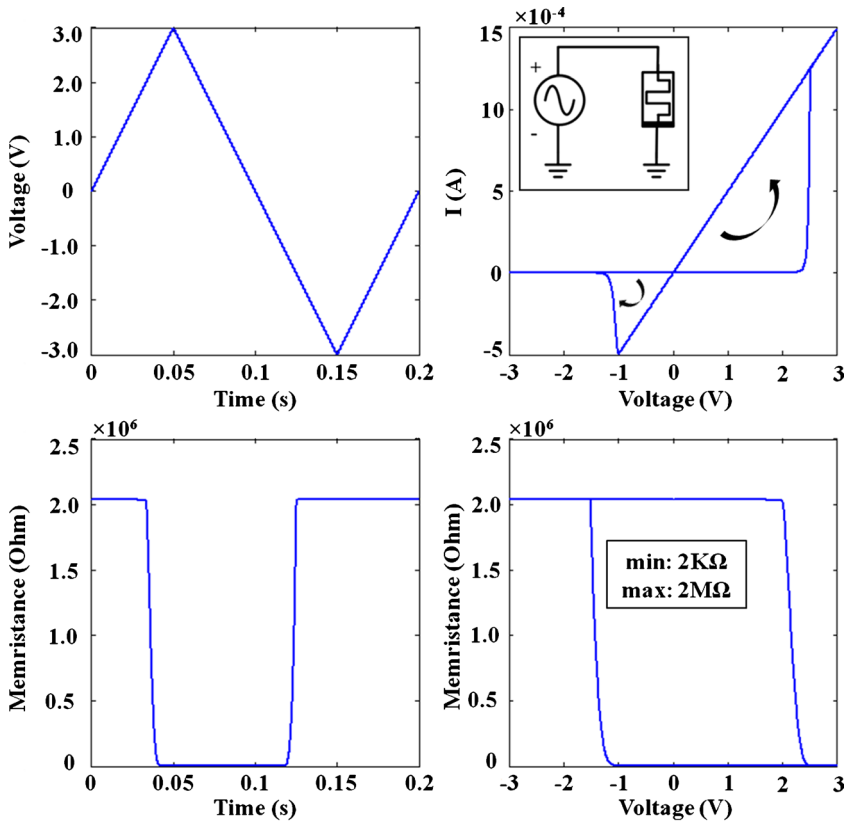

Fig. 1 Simulation results from the response of the memristor model [27] to a triangular ac applied voltage, showed in the *upper-left* graph. The hysteretic current–voltage (*I–V*) characteristic of a device with (V_{RESET}, V_{SET})=(−1, 2 V) is demonstrated in the *upper-right* graph, and the corresponding change of the resistance (memristance) with time and with the applied voltage is shown in the graphs which are placed below

particular, first a positive voltage is applied, thus creating the necessary conditions to either change the state of the RPM (i.e. the lower placed device) from ON to OFF or to change the state of the FPM from OFF to ON. As it can be seen in the corresponding graphs, when voltage reaches a particular point, then the state of the FPM changes first and the current rises to very high values until the RPM finally switches to the OFF state. At this point, the initial state configuration FPM/RPM=OFF/ON of this complementary switch has been flipped to ON/OFF. Next, the circuit exhibits an ohmic behaviour until the voltage reaches a specific negative value, when the RPM first changes to the ON state. As the negative voltage sweep continues, the FPM is also flipped and the circuit continues exhibiting ohmic behaviour again until the end of the voltage sweep. An important observation regarding the resulting *I–V* characteristic of the anti-serially connected memristors is that the current is linear with the applied voltage, except in two finite voltage intervals where it remains linear but with different gradient due to the much higher observed conductance.

In such memristive element configurations, the switching voltages cannot be formerly known exactly. The connected devices form a voltage divider circuit; therefore, the voltage drop over each element depends on the total external applied voltage, on the internal states of the devices and on their particular switching characteristics. In order to utilize an ASM as a memory cell, starting from its corresponding *I–V* graph of Fig. 2, appropriate programming voltages and reading voltages need to be selected. The first must exceed the voltage limits where the state transitions are completed, whereas the latter must be selected within the specific region where presence of high (low) current will determine reading an OFF/ON (ON/OFF) binary state. Here, we choose to programme the device using ±5 V pulses, whereas reading their state could be done by applying pulses whose amplitude falls within the voltage window specified by the limits of the observed high conduction lobes. However, as shown in Fig. 2, the width of these reading windows depends on the threshold voltage values of the individual memristors. The cases where $|V_{RESET}|>|V_{SET}|$ or $|V_{RESET}|=|V_{SET}|$ are definitely preferable because the high conduction intervals are better defined, compared to the case of having $|V_{RESET}|<|V_{SET}|$. Proper selection of the devices will be useful in order to overcome inevitable process, voltage, and temperature (PVT) variations between different individual devices. Nevertheless, in all conducted simulations here we consider individual memristive elements with identical switching characteristics (i.e. threshold voltages, memristance value limits, model parameters). Starting with the ASM preprogrammed at the state OFF/ON, if we apply a read pulse, then the measured current will result high. This happens because when reading this specific logic state, the internal state of the ASM changes to the intermediate state ON/ON, which is why this has been identified in the literature as a destructive read-out operation [29]. Therefore, after

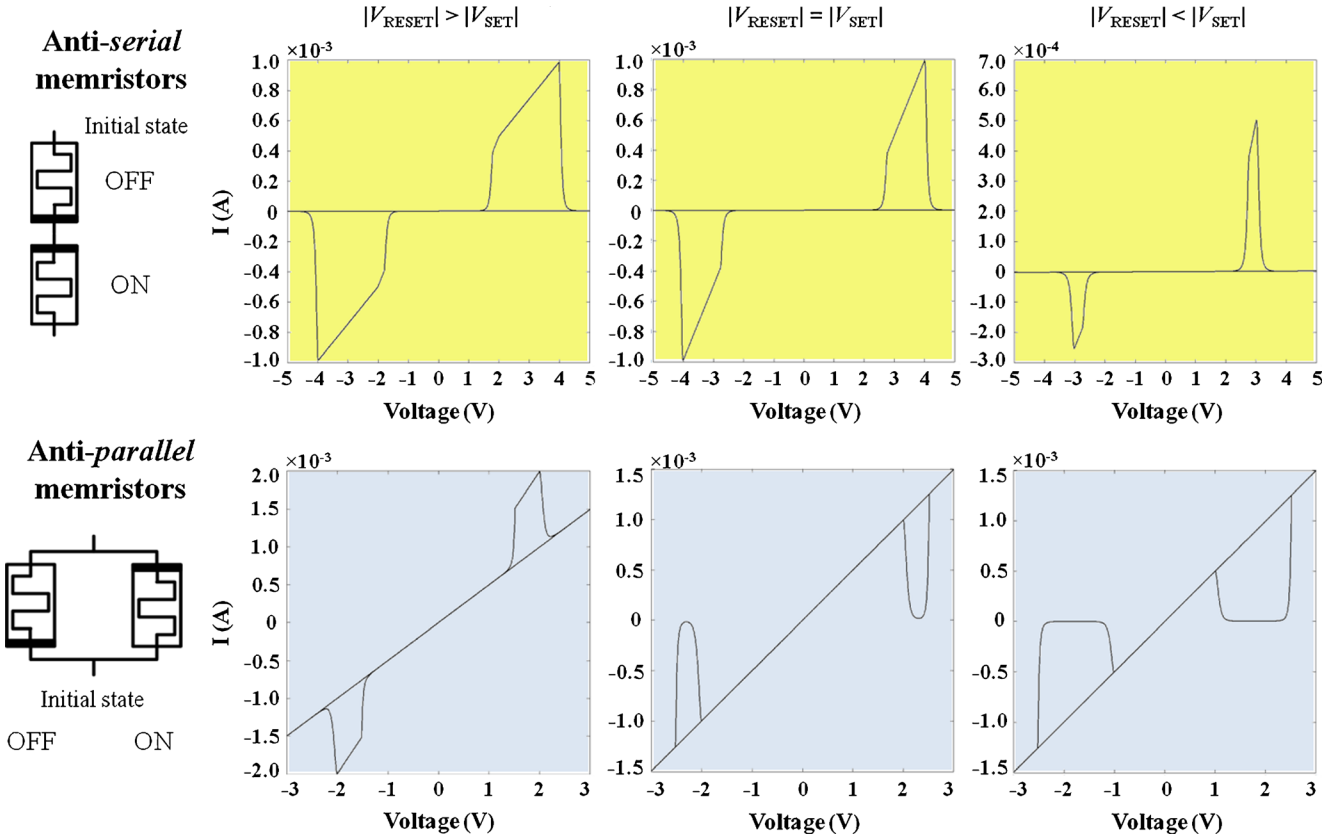

Fig. 2 Simulation results for the current–voltage (*I–V*) characteristics of anti-serial and anti-parallel memristive switches under a single triangular voltage sweep of appropriate amplitude and the same frequency as in Fig. 1. The switches are initialized to the given state configurations. Three different cases are examined regarding the threshold voltages of the individual elements, namely, $|V_{RESET}|>|V_{SET}|$ with $V_{RESET}=-2$ V and $V_{SET}=1$ V, $|V_{RESET}|=|V_{SET}|$ with $V_{RESET}=-2$ V and $V_{SET}=2$ V, and $|V_{RESET}|<|V_{SET}|$ *with* $V_{RESET}=-1$ *V and* $V_{SET}=2$ *V, respectively*

reading the OFF/ON state, it is necessary to restore the ASM immediately afterwards by rewriting it; thus, we should apply a negative write pulse (here −5 V). Whenever this procedure is repeated, the less resistive combination occurs, i.e. the ON/ON state; hence, there is always an instant current peak which is characteristic of this transition. Finally, if we wish to change the state of the ASM from OFF/ON to ON/OFF, we have to apply a positive programming pulse (here +5 V). Then, a reading pulse will identify the cell's state with the measured current being low this time, given that no change is induced to the state of the cell during read-out.

2.2 Anti-Parallel Memristive Switch (APM)

Considering again a single memristive device as a structural element, we analyze the behaviour of two connected memristors with opposing polarities, this time in parallel, forming an APM. In the rest of the paper, whenever necessary, we will use operator '||' to denote two memristors connected in parallel. Likewise in the ASM case, a combination of low and high resistances is used for the representation of the stored digital values. More specifically, the combination (FPM, RPM)=(OFF, ON) could denote logic '1', whereas the opposite combination could denote logic '0'. The initial memristances of individual memristors should be set to either of the aforementioned boundary value combinations after manufacturing, prior to further processing. In the APM case, since the same voltage is simultaneously applied to both memristors, we do not notice any induced shift in the switching threshold voltages that dominate the composite behaviour of APM structures, compared to the response of the individual structuring elements. However, unlike the series connection, in the parallel connection, the lower resistance values (R_{ON}) will dominate the total resistance of each APM.

In Fig. 2, the simulation results of a pair of anti-parallel memristors are shown. Compared to the previously described case, we now notice a major difference in the overall composite memristance switching; the memristance is kept at low values except for two certain intervals. This is because, as we have concluded before, devices with opposite polarities have opposite switching characteristics; each time a voltage is applied, one of the devices tends to switch to the OFF state and the other to the ON state, respectively. Hence, there will almost always be a device at the ON state, dominating this way the total memristance. The resulting *I–V* characteristic looks like a truncated Ohm's law; the current is linear with the

voltage exclusive of two finite intervals, where both devices are found at the OFF state. The (FPM, RPM)=(OFF, OFF) state combination is found only as an intermediate state during the state transitions of the circuit components, likewise happened with the ON/ON combination in ASMs. This behaviour is opposite to the *I–V* characteristic of the in-series complementary configuration of memristors forming ASMs. Of course, proper selection of devices which demonstrate appropriate threshold voltages (or carefully engineering the desired threshold values [30]) will correspondingly affect the period of duration of the OFF/OFF combination. Nevertheless, according to Fig. 2, the case where $|V_{RESET}|<|V_{SET}|$ seems to be the only viable option in APMs which guarantees the expected operation. When $|V_{RESET}|=|V_{SET}|$, we again notice a short period of very low conduction, even though practically, no such conducting state is expected since both memristors switch simultaneously, and hence, the equivalent resistance of the APM remains the same ($R_{OFF}\|R_{ON}=R_{ON}\|R_{OFF}$). On the other hand, different switching rates for SET (OFF to ON) and RESET (ON to OFF) operations could be attributed to the interaction of the external applied field, the internal field of the concentrated defects (e.g. charge traps, mobile ions, oxygen vacancies in metal-oxide material stack configurations, etc.), and the diffusion, all acting in the same or in opposite directions according to the applied voltage bias [4], [6]. In our model, the RESET process is completed faster than the SET counterpart, which is where the aforementioned short low conduction periods are derived from. Nonetheless, given that such differences in the switching rates are device-dependent, $|V_{RESET}|=|V_{SET}|$ is not considered an appropriate option in order to form well-defined APMs.

Furthermore, if the threshold voltages of individual memristors belong to the case where $|V_{RESET}|>|V_{SET}|$, then the APM operation is completely ruined. Indeed, it is quite intriguing to notice that two memristors with $|V_{RESET}|>|V_{SET}|$, when connected in an anti-parallel configuration forming an APM, actually behave like an ASM. This particular choice, however, compared to really anti-serially connected memristors, although it is obviously well defined, with the composite threshold voltages being equal to those of the individual structuring memristors, it delivers a much smaller ratio between the two distinct conducting states and thus will be less useful when used as storage element in large crossbar memory arrays, whose basic operation we describe later in this work.

2.3 Pulse Properties of ASMs and APMs

Figure 3 presents the simulation results of a pulse driven memory cell when comprising either an ASM (a, b) or an APM (c, d) switch. As described previously, single memristors with opposite polarities generally demonstrate reversed behaviour to the applied signals; therefore, for any applied voltage, the complementary devices will be changing their states in a reciprocal way. Starting with the ASM preprogrammed as FPM/RPM=OFF/ON, a positive read pulse will result in high measured current because the internal state of the ASM changes to the intermediate state ON/ON; i.e. the FPM changes its state first as a result of the voltage divider between the FPM and the RPM. High measured current is always indicative of the transition to the less resistive combination (i.e. ON/ON). Afterwards, both memristors remain unaffected since the corresponding voltage drop on each of them does not surpass the voltage thresholds. On the contrary, in APMs, the (FPM, RPM)=(OFF, OFF) state combination is the intermediate state during the state transitions of the circuit components; their behaviour is opposite to that of ASMs (the device initially found in the less resistive state changes first to the high resistive state).

In our case, first, a read pulse is applied to check the state of the memristive switch. In general, such a read pulse must be of appropriate amplitude and duration so as to switch the ASM (APM) to the intermediate ON/ON (OFF/OFF) state, as discussed previously. In our simulations, we assume the most convenient threshold voltage conditions for each device combination, i.e. $|V_{RESET}|>|V_{SET}|$ with $V_{RESET}=-2$ V and $V_{SET}=1$ V for ASMs and $|V_{RESET}|<|V_{SET}|$ with $V_{RESET}=-1$ V and $V_{SET}=2$ V for APMs, respectively. Therefore, based on the particular *I–V* characteristics of Fig. 2, we choose to apply read pulses of 3 V and 2 V to ASMs and APMs, correspondingly, so as to approximate the centre of the reading voltage windows and hence to ensure a secure reading operation. As shown in Fig. 3e, f, the resistance switching for both ASMs and APMs is completed within less than 7 ms. However, here the duration of the applied pulses is chosen to be 10 ms so as to facilitate better distinction between the reading currents in the corresponding graphs demonstrated in Fig. 3b,d. As high (low) current is detected, the ASM (APM) is initially found in the FPM/RPM=OFF/ON state. In the next step, a negative write pulse is applied which restores the initial state of the devices. We note here that the amplitude of the write pulses was selected to be ±5 and ±3 V for ASMs and APMs, respectively. Their duration was set to the minimum value which guarantees a complete transition of the composite memristance, as shown in Fig. 3e, f; in specific, it is 12 ms for ASMs and 7 ms for APMs. Then the same procedure is repeated, i.e. a read pulse is applied which results in the same current measurements, and next, a negative write pulse restores the "destroyed" state of the storage elements. As during the read process, one of the memristors changes from OFF to ON (ON to OFF) in the ASM (APM), the stored information is destroyed and needs to be rewritten. Next, a positive write pulse is applied which sets the switches to the FPM/RPM= ON/OFF state. The following read pulse results in measurable current for the APM and in almost non-detectable current in the ASM, which are indicative of reading the FPM/RPM=

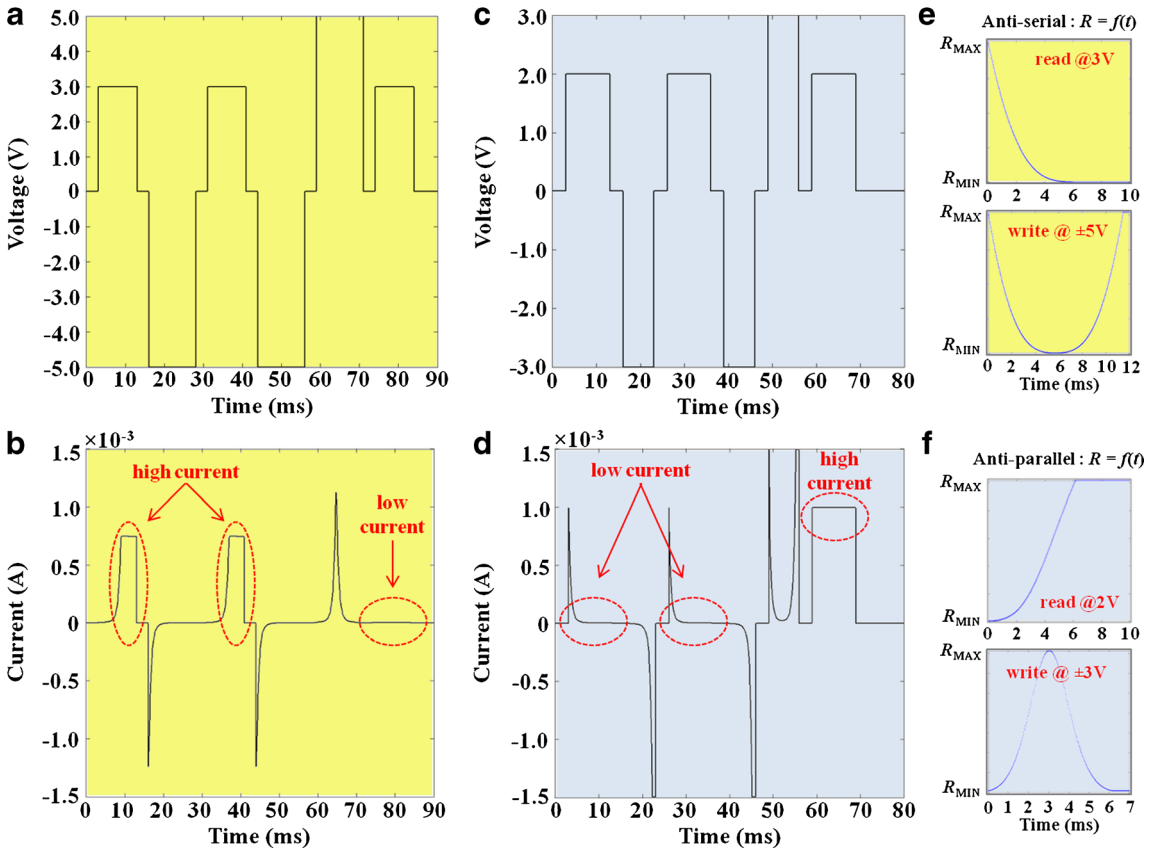

Fig. 3 Pulse properties of anti-serial (*yellow background*) and anti-parallel (*light blue background*) memristive switches. The voltage pulses applied to an ASM and an APM cell are shown in (**a**) and (**c**), whereas the resulting currents are shown below in (**b**) and (**d**), respectively. After the first two read pulses, as the stored information is destroyed, a write back of the initial state is performed right afterwards. The induced change to the composite resistance by the read and write pulses when applied to ASMs and APMs is shown in (**e**) and (**f**), respectively

ON/OFF state. At this point, it is worth mentioning that all assumptions regarding both threshold and programming voltage values have been made only in the context of this study of ASMs and APMs as memory cells in crossbar arrays; thus, they do not relate to any real, manufactured or measured devices. Nevertheless, current experimental device characteristics [31] demonstrate that memristors and crossbar arrays can be integrated with existing advanced, nanometric CMOS technologies with a nominal voltage of around 1 V.

3 Memristor-Based Passive Crossbar Memories

The crossbar structure possesses many attractive features as it offers the highest possible device density and the simplest interconnect configuration that still allows external access to each nano-device. In this work, we study a nano-crossbar memory system that uses compositions of anti-parallel (APM) or anti-serial (ASM) memristors as memory elements. Such system does not utilize the kind of devices (diodes or transistors) that are normally used to isolate the cell being written to and read from in conventional memories.

The simplest circuit approach for reading information from the memristor-based crossbar, whether it is based on single memristors, APMs or ASMs, is by applying a certain read voltage across a junction and transforming the current flow into a voltage. The basic setup of a nano/CMOS crossbar memory system is shown in Fig. 4. Column and row decoders drive the necessary selection switches in order to form a voltage divider circuit with the corresponding pull-up resistor and the resistance of the accessed node. Typically, the pull-up resistors are implemented in a CMOS layer or in a form of nanowire resistors. The output of the voltage divider is then driven to a CMOS sense amplifier, and the state of the device is distinguished by comparing this voltage to a reference value. The voltage swing at the output of the crossbar read circuit, between reading distinct binary stored data in form of different impedance states, should be large enough for the two states to be easily distinguishable.

In the rest of this section, we first summarize the fundamentals of passive crossbar memories comprising single memristors as cross-point storage cells and later, extend our analysis to include the cases of ASMs and APMs. The general equivalent circuit of a read operation in a passive crossbar, regardless of the cross-point cell type, is given in Fig. 5a. In

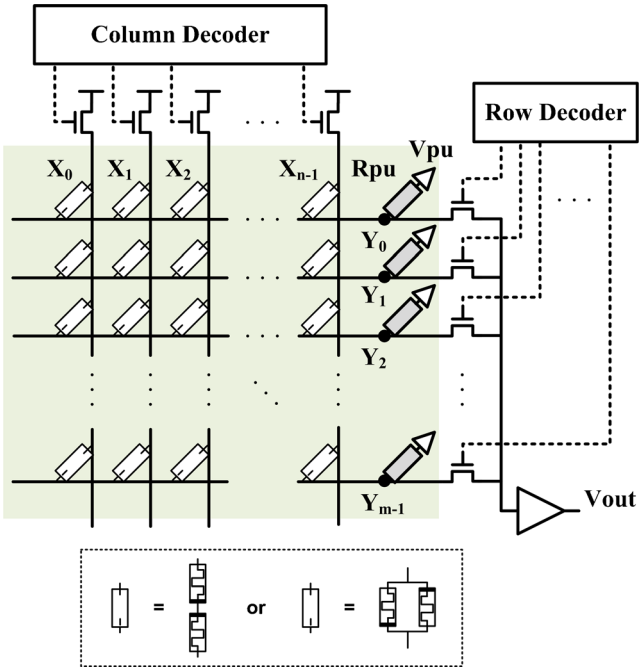

Fig. 4 Basic setup of a passive nano/CMOS crossbar memory system. Column and row decoders drive the corresponding selection devices and the voltage drop on the accessed element is then sensed and compared to a reference value by appropriate CMOS sensing circuits. In our work, the cross-point storage elements can consist of anti-serial or anti-parallel configurations of memristors

the ideal reading case, where no current sneak paths are present, the equivalent circuit for the read operation is a simple voltage divider formed by a pull-up resistor R_{PU} and the accessed element (Fig. 5b). Considering a single memristor at each cross-point, then for a given $\beta=R_{OFF}/R_{ON}$ ratio, the achieved voltage swing ΔV for a certain applied pull-up voltage V_{PU} is calculated as follows:

$$\frac{\Delta V}{V_{PU}}=\frac{V_{OFF}-V_{ON}}{V_{PU}}=\frac{R_{OFF}}{R_{OFF}+R_{PU}}-\frac{R_{ON}}{R_{ON}+R_{PU}} \tag{6}$$

This normalized detection margin of the two possible states of a memory cell is maximized if the pull-up resistor R_{PU} is optimally chosen to be the geometric mean of the two bistable resistances of the memristors. However, for large R_{OFF}/R_{ON} ratios, the optimal R_{PU} is close to the less resistive state, i.e. R_{ON}. Unfortunately in a real reading operation, with parasitic current paths in parallel to the accessed memristor, the effective R_{OFF}/R_{ON} ratio results substantially smaller (Fig. 5c). The impact of parasitic sneak paths definitely depends on the way the crossbar is accessed. Here, a crossbar-setup with m wordlines and n bitlines is assumed, where the resistance of the selection transistors and interconnects is neglected. Among different approaches of accessing the crossbar, one is to select one wordline, pull up one bitline and leave the other bitlines floating, whereas another way is to select one wordline and pull up all bitlines simultaneously. In this study, the first approach is used, and thus, the reading operation assumes accessing one bit at a time. The worst-case scenario for reading the crossbar is the following: when reading a memristor found in the OFF state and the parasitic resistance is as small as possible, the crossbar output voltage notably degrades. This is the case where all non-accessed memristors are set to ON, i.e. $R_{sneak}=R_{ON}$ (see Fig. 5). One could similarly consider the corresponding worst-case scenario when reading a memristor found in the ON state to assume that all non-accessed nodes are set to the OFF state (i.e. $R_{sneak}=R_{OFF}$), thus resulting in smaller measured current, although the impact is less severe to the reading output in this case. The parasitic worst-case resistance for an $n\times m$-crossbar can be computed using the equivalent circuit shown in Fig. 5c. This resistance is connected in parallel with the accessed memristor, and as a result, the maximum achievable read voltage margin gets significantly smaller with increasing crossbar size, as well as it strongly depends on the distribution of the stored information in the array [32, 33].

In the case of having ASMs as cross-point devices, the equivalent circuit of a real read operation is the same, only that now the composite resistance at each node is equal to the sum of the FPM and the RPM resistance values, i.e. $R_{OFF}+R_{ON}$, regardless of the specific stored data. Considering a high enough resistance ratio $\beta>>1$, then the composite resistance at each node is approximately equal to R_{OFF}. As a consequence, it is also $R_{sneak}=R_{OFF}$. Therefore, based on Fig. 5c and assuming a quadratic crossbar grid with $m=n$, without loss of generality and in order to simplify our calculations, the parasitic resistance connected in parallel with the accessed ASM is calculated as follows:

$$R_P=2\frac{R_{OFF}}{m-1}+\frac{R_{OFF}}{(m-1)^2}=\frac{2m-1}{(m-1)^2}R_{OFF}=\lambda R_{OFF}. \tag{7}$$

Parameter λ in Eq. (7) only depends on the crossbar size of the quadratic array m and its approximate value for the sizes of interest in this paper, namely, for $m=n=\{8, 16, 32, 64\}$, is, respectively, $\lambda\approx\{0.31, 0.14, 0.07, 0.03\}$. The equivalent measured resistance which results by combining the resistance of the accessed node with the parasitic resistance, when the stored state of the ASM during read-out becomes FPM/RPM=ON/ON, i.e. when the composite resistance becomes $2\times R_{ON}$, is as follows:

$$R_{EQ,1}=2R_{ON}\left|\right|R_P=\frac{2R_{ON}\lambda R_{OFF}}{2R_{ON}+\lambda R_{OFF}}\xrightarrow{R_{OFF}=\beta R_{ON}}\frac{2\lambda\beta {R_{ON}}^2}{2R_{ON}+\lambda\beta R_{ON}} \tag{8}$$
$$=\frac{2\lambda\beta}{2+\lambda\beta}R_{ON}=\frac{2\lambda}{\frac{2}{\beta}+\lambda}R_{ON}.$$

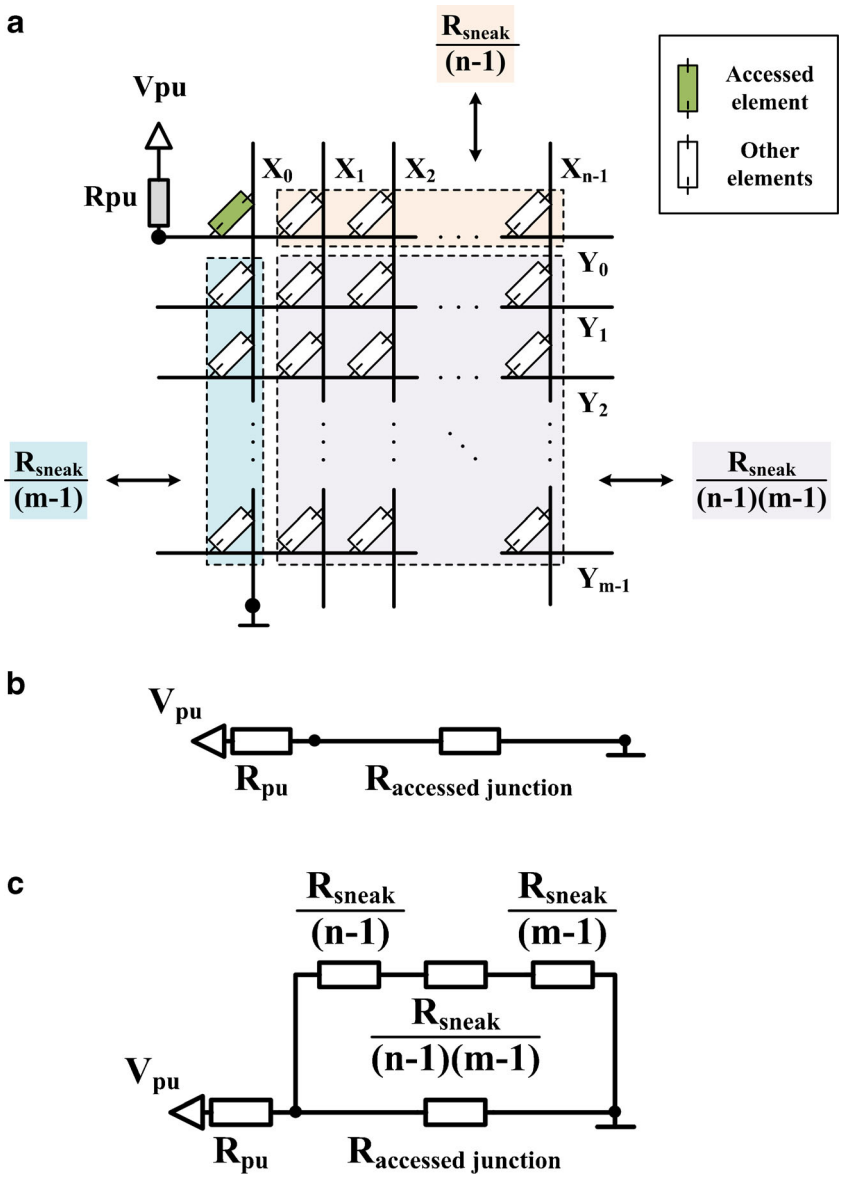

Fig. 5 **a** Read operation equivalent circuits in passive crossbar where all non-accessed cells are set to the same resistive state R_{sneak}. **b** The ideal reading case with the accessed device forming a simple voltage divider with the pull-up resistor. **c** The more realistic case with the inevitable parasitic resistance

Assuming a high enough resistance ratio β, from Eq. (8), we have $R_{EQ,1} \approx 2 \times R_{ON}$. This means that the result of reading this state only involves the less resistive state of the memristors and is almost independent of the crossbar size and the stored data distribution within the rest of the memory array. Similarly, when the stored state of the ASM is the opposite, i.e. which remains unaffected during read-out, the corresponding equivalent resistance is as follows:

$$R_{EQ,2} = (R_{ON} + R_{OFF} \approx R_{OFF}) \Big|\Big| R_P = \frac{R_{OFF} \lambda R_{OFF}}{R_{OFF} + \lambda R_{OFF}} = \frac{\lambda}{1+\lambda} R_{OFF}. \tag{9}$$

According to Eq. (9), the result of reading this stored state appears to exclusively depend on parameter λ, i.e. on the crossbar size. In particular, for large crossbar arrays where $\lambda << 1$, it is $R_{EQ,2} \approx \lambda \times R_{OFF}$. Hence, in this case, the measured resistance involves the most resistive state of the memristors. In overall, the resulting general ratio between the two equivalent resistances becomes as follows:

$$\frac{R_{EQ,2}}{R_{EQ,1}} = \frac{\lambda R_{OFF}}{2R_{ON}} \overset{R_{OFF}=\beta R_{ON}}{\rightarrow} \frac{\lambda \beta}{2}. \tag{10}$$

According to Eq. (10), since each of the binary states involves different resistive states, then a high enough ratio β between these values is necessary and will certainly play a crucial role for the effective distinction between them during

read-out, compensating the effect of the larger crossbar sizes represented by the small values of parameter λ.

Relative to having APMs as cross-point devices, we use again the same equivalent circuit of Fig. 5c, only that now the composite resistance at each node is equal to the resulting resistance of the two parallel connected devices, i.e. $R_{OFF} \parallel R_{ON}$:

$$R_{ON}\Big|\Big|R_{OFF} = \frac{\beta}{\beta+1}R_{ON} \overset{\beta>>1}{\rightarrow} \approx R_{ON} \tag{11}$$

regardless again of the particular stored information. As a consequence for the entire grid, it is $R_{sneak}=R_{ON}$. Therefore, considering again a high enough resistance ratio $\beta>>1$ as well as also assuming a quadratic crossbar array with $m=n$, then the parasitic resistance connected in parallel with the accessed APM is calculated as follows:

$$R_P = 2\frac{R_{ON}}{m-1} + \frac{R_{ON}}{(m-1)^2} = \frac{2m-1}{(m-1)^2}R_{ON} = \lambda R_{ON}. \tag{12}$$

This parasitic resistance, compared to that of Eq. (7) which was derived for ASM-based crossbar, it results significantly smaller involving the less resistive state of the memristors, i.e. R_{ON}. Combined with parameter λ, which gets smaller for larger array sizes, this resistance will quickly reach very small values, and thus, it is expected to affect dramatically the overall memory function. The equivalent measured resistance which results by combining the resistance of the accessed node with the parasitic resistance, when the stored state of the APM during read-out becomes FPM/RPM=OFF/OFF, i.e. when the composite resistance becomes $R_{OFF}/2$, is as follows:

$$R_{EQ,1} = \left(\frac{R_{OFF}}{2}\right)\Big|\Big|R_P = \frac{\left(\frac{R_{OFF}}{2}\right)\lambda R_{ON}}{\left(\frac{R_{OFF}}{2}\right)+\lambda R_{ON}} \overset{R_{OFF}=\beta R_{ON}}{\rightarrow} \frac{\lambda\beta}{2\lambda+\beta}R_{ON} = \frac{\lambda}{\frac{2\lambda}{\beta}+1}R_{ON}. \tag{13}$$

Assuming a high enough resistance ratio β, from Eq. (13) we have $R_{EQ,1}\approx\lambda\times R_{ON}$, i.e. the measured resistance results the same with the parasitic resistance, affected only by the crossbar size (parameter λ) but not by the stored data distribution within the rest of the memory array. Similarly, when the stored state of the APM is the opposite, hence, during read-out it remains unaffected, the corresponding equivalent resistance is as follows:

$$R_{EQ,2} = \left(R_{ON}\Big|\Big|R_{OFF}\approx R_{ON}\right)\Big|\Big|R_P = \frac{R_{ON}\lambda R_{ON}}{R_{ON}+\lambda R_{ON}} = \frac{\lambda}{1+\lambda}R_{ON}. \tag{14}$$

Equation (14) shows that the result of reading this stored state, likewise in the case of ASMs, depends only on parameter λ and for large crossbar arrays, where $\lambda<<1$, it will be $R_{EQ,2}\approx\lambda\times R_{ON}$. Hence, in this case, the measured resistance involves again the less resistive state of the memristors. Therefore, the resulting general ratio between the two equivalent resistances becomes as follows:

$$\frac{R_{EQ,1}}{R_{EQ,2}} = \frac{\frac{\lambda}{\frac{2\lambda}{\beta}+1}R_{ON}}{\frac{\lambda}{1+\lambda}R_{ON}} \overset{\beta>>1 \quad \lambda<<1}{\rightarrow} \approx 1. \tag{15}$$

According to Eq. (15), regardless of the high resistance ratio that the memristors may exhibit, since both binary states involve only R_{ON}, then for large crossbar arrays (i.e. when $\lambda<<1$) the effective distinction between the different stored states during read-out becomes totally impractical.

4 Simulation Results for APM/ASM-Based Crossbar Arrays

For evaluation and comparison purposes, read-out performances of several sets of crossbar memory designs are compared in this section. For all design sets, detection margins are normalized with respect to the applied readout voltage V_{PU} since their values will be always proportional to V_{PU}. Simulation results for the floating memristor array, considering either of the proposed cross-point memristive solutions, are shown in Fig. 6. Model parameter values are used as given in $\{\alpha,\ b,\ c,\ m,\ f_o,\ L_o\}=\{5\times10^4,\ 0,\ 0.1,\ 82,\ 310,\ 5\}$, and the limiting values of parameter r are selected as $r_{min}=100$ and r_{max} equal to either of the following values {170, 390, 600, 900} corresponding to $R_{ON}\approx2$ KΩ and $R_{OFF}\approx$ {20, 200, 400, 600} KΩ, respectively. The latter result in four different memristance ratios $\beta=\{10, 100, 200, 300\}$. Moreover, the threshold voltages for ASMs and APMs are set in such a way so as to result in a wider (hence clearer) reading window, as explained earlier and shown in Fig. 2. In all read-out measurements, we assume common values for the pull-up resistors, namely, we set $R_{PU}=2\times R_{ON}$ for ASMs (i.e. equal to the less resistive state of an ASM) and $R_{PU}=R_{ON}/2$ for APMs (i.e. equal to the less resistive state of an APM), respectively. Also, different array sizes and/or different $\beta=R_{OFF}/R_{ON}$ ratios affect the measured equivalent resistance. Therefore, taking into consideration the in-series sense resistor R_{PU} as well as the composite switching behaviour that ASM and APM devices exhibit when studied inside the crossbar array (likewise we did for the stand-alone devices and presented in Fig. 3), here we selectively adjust the amplitude and the duration of the applied reading pulse V_{PU} in order to achieve the largest possible voltage margins. Table 1

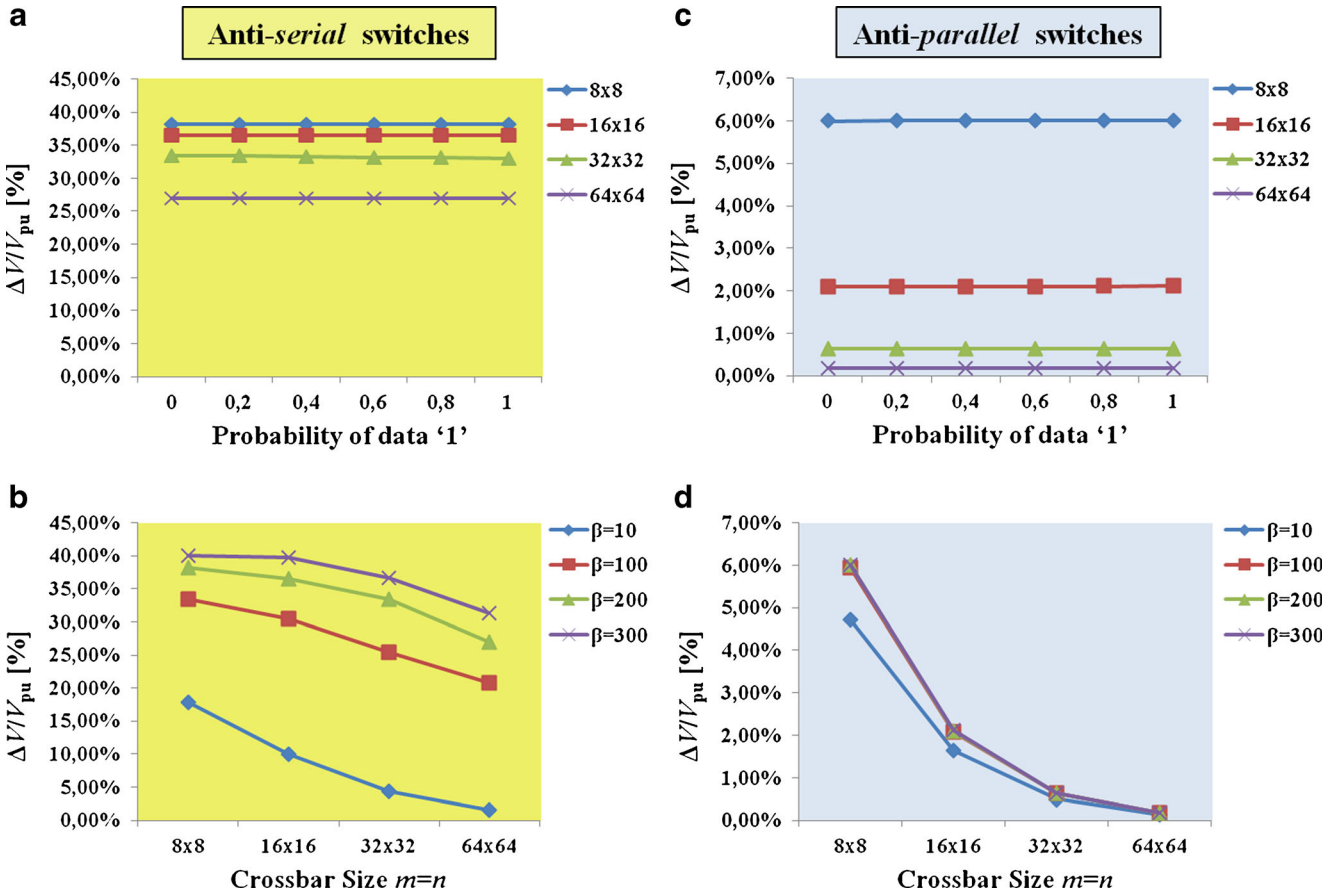

Fig. 6 Read voltage margins for ASMs and APMs (**a**, **c**) and normalized read voltage margin $\Delta V/V_{PU}$ versus the stored data distribution in the grid for four different array sizes with up to 64×64 elements (**b**, **d**). Normalized read voltage margin $\Delta V/V_{PU}$ versus crossbar size (quadratic array where columns=rows) for four different $\beta=R_{OFF}/R_{ON}$ ratios. We consider reading one cross-point element/time and assume using $R_{PU}=2\times R_{ON}$ for ASMs and $R_{PU}=R_{ON}/2$ for APMs, respectively. Graphs presented in subfigures (**a**) and (**c**) correspond to ratio $\beta=200$

summarizes the used V_{PU} pulse characteristics for each simulation scenario. It can be noticed that, although the necessary pulse duration seems comparable, there is a huge difference between the voltage amplitudes; unlike ASMs, APMs require much higher operation voltages which increase for larger crossbar arrays, regardless of the β ratio. As it was previously mentioned, the absolute values of the voltages presented in Table 1 are used only in the context of this survey since it is inacceptable to use such high voltages for any concrete memory application or non-volatile embedded memories.

In specific, the voltage margins for different distributions of the stored information in the memory array are calculated, for different grid sizes and for different $\beta=R_{OFF}/R_{ON}$ ratios. With the used voltage scheme, we make sure that the corresponding voltage drop approximates the middle of the reading window only at the accessed device. Voltages at all non-accessed cells are limited to values below the threshold voltages of the reading window for both serial and parallel memristive cross-point configurations; thus, these storage cells are not affected during read-out. Our calculations, without loss of generality, neglect the word and bitline resistance R_{LINE}, which in general should be small compared to R_{ON} in order to be able to operate large crossbar arrays (for practical arrays, optimization between the array size and the R_{ON}/R_{LINE} ratio has to be worked out). In pure passive memristive crossbar arrays, the noise margins almost vanish very quickly as the array size gets larger regardless of the chosen resistance ratio [33]. Moreover, the measured voltages strongly depend on the distribution of the stored information in the memory. In this context, as shown in Fig. 6a, c, ASMs and APMs could efficiently address the sneak path problem since they exhibit measured resistances which are independent of the stored data distribution within the memory array. However, although ASM-based arrays exhibit high enough noise margins, this is not true for APM-based arrays where normalized voltage margins not only are lower but also decay with increased array sizes faster than in ASM-based architectures. Furthermore, in Fig. 6b, d, we notice the minor effect that high β values have on the APM-based array performance. In fact, examining each array size separately, in ASMs seemingly there is some improvement in the voltage margin when moving from lower to higher memristance ratios, whereas in the APMs case, there is no significant change; indeed for larger arrays, there is no evident difference at all.

Table 1 V_{PU} pulse characteristics

Memristance ratio β	Anti-*serial* memristors					Anti-*parallel* memristors				
	Amplitude (V)				Duration (ms)	Amplitude (V)				Duration (ms)
	8×8	16×16	32×32	64×64		8×8	16×16	32×32	64×64	
10	3.7	5	8	14	2.4	5	8	14	25	2.4
100	2.2	2.4	2.7	3.4	7.2	4	6.5	12	22	8.4
200	2.1	2.2	2.4	2.7	12	4	6.5	12	22	13.2
300	2.1	2.2	2.3	2.5	18.6	4	6.5	12	22	20.4

Thereupon, although both ASMs and APMs could seemingly address the sneak path problem, based on our mathematical analysis and the presented simulation results, the effectiveness of anti-parallel memristors fails to compensate the devastating effect that large memory arrays have on the read-out voltages. The maximum achievable read voltage margin gets significantly smaller with increasing crossbar size and seems to approximate zero very quickly, regardless of the exhibited resistance ratio β of individual memristive devices. It is therefore evident that, unless some innovative techniques are found which will enlarge significantly the measured voltage margins, thus resulting in more effective read-out memory operations, APM-based crossbars are considered inappropriate for the practical realization of large passive crossbar memory systems.

5 Application of Alternative Topologies for ASM-Based Crossbar Memories

In [28] the present, authors introduced a set of novel topologies for passive memristor-based crossbar memories. Such alternative topologies comprise a certain percentage of insulating nodes, placed between mutually perpendicular wires, which are spread out inside the array according to specific distribution patterns. The motivation is to restrain current sneak paths and thus improve the voltage margins by replacing (hence "sacrificing") some memory cells. Such a practice is considered a viable solution given the huge device density that the crossbar geometry offers compared to other circuit architectures. All patterns were tested in 32×32 and 64×64 memory arrays for the worst-case scenario when accessing only a single cell per read operation, and their performance was compared to that of the full memristive crossbar. As far as the amount of the inserted insulators is concerned, three different cases were examined where their number approximates 10, 25 or 50 % of the total nodes of the grid under consideration. In each case, the selected distribution of the insulating junctions aims to uniformly cover the entire area of the grid, as much as this is possible, depending on the specific pattern and the actual grid size. The introduced patterns delivered up to 4× better read-out voltages for this type of reading approach. In particular, the uniformly distributed insulating junctions of the "uniformly distributed" pattern restrained better the current sneak paths, and thus, this topology had the best performance. In this pattern, the insulating nodes are placed in such a manner in order to be uniformly distributed both horizontally and vertically inside the grid. For each insulator, the closest neighbouring insulating nodes are always found at equal horizontal and vertical distances. A schematic representation of the aforementioned pattern is depicted in Fig. 7a where red dots denote insulating nodes, placed between mutually perpendicular wires, and simple wire crossings denote memristive cross-points.

In the present work, we applied the most efficient one of the tested topologies to ASM-based memory arrays. We then evaluated the performance of the pattern by comparing the read-out voltage margins with those of the pure ASM-based grid. In our simulations, we use the same model parameter values and the same voltage pulsing characteristics, as previously shown in Section 4, though here we examine only the case where the memristance ratio is set to β=200. More specifically, the calculated voltage margins are normalized to those of the grid without insulators, and their relation is presented in Fig. 7b. Both 32×32 and 64×64 memory arrays were employed, and the read-out operation was performed to the leftmost cell of the upper row of the grid where no insulating node is found (see Fig. 7a). The resistances of the interconnects, the sensing elements, and the voltage source/s are not taken into consideration here in order to reduce the total complexity of the system and minimize simulation runtime, given that their effect has already been examined before [32]. As shown in Fig. 7b, the new voltage margins are improved incrementally when increasing the percentage of the inserted insulating nodes and the notable improvement reaches up to 21 % (42 %) for 32×32 (64×64) arrays when half of the existing nodes are insulators. Another interesting observation concerns the resulting ratio between the measured voltages for corresponding percentages of insulated nodes in the two considered grid sizes. Particularly, one can observe that for each one of the examined percentage rates, doubling the size of the side of the square lattice results in almost

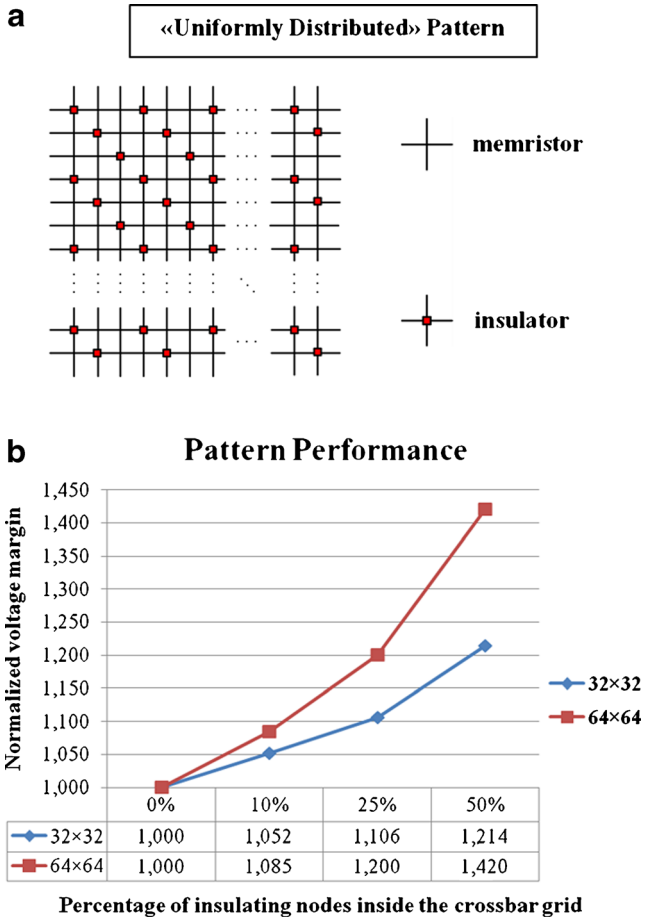

Fig. 7 Application of a novel topology to an ASM-based crossbar memory. A schematic representation of the applied pattern is shown in (**a**) with the insulating junctions being uniformly distributed across the array. In (**b**), the normalized read voltage margin for the worst-case reading scenario for both 32×32 and 64×64 grids is shown. The tested pattern introduces 10, 25, or 50 % insulators, and its performance is compared to the corresponding performance of the pure ASM-based grid with 0 % insulating nodes with the memristance ratio set to β=200

doubling the rate of improvement in the measured voltages. Therefore, it is assumed that such important improvement of the measured voltages is kept when moving to much larger quadratic memory crossbar arrays.

The induced voltage margin enhancements are uniform for the entire grid, though the actual measured voltages are expected to slightly decay as we move away from the voltage sources, taking into consideration the resistances of the word and bitlines [32]. The alternative crossbar topology should be also proven useful in large hierarchical memory organizations where the option of dividing a memory lattice into a number of smaller-sized sub-arrays exists, in order to maintain sufficient voltage margins. According to simulation results shown in Fig. 6, the smaller the memory array size, the larger the voltage margin gets. Therefore, pure memristive arrays need to get divided in much smaller sub-arrays so as to deliver voltage margins which surpass the ones offered by arrays including insulators. Given the possible voltage margin improvements offered by the novel array topology, the necessary sub-arrays composing a larger collective memory should be less in number and larger in size, thus reducing the overhead of extra peripheral circuits. The current sneak path problem is better addressed by following the presented novel approach, thus providing a viable option for the enhancement of the measured read-out voltage margins which will allow for the better distinction of the different stored memory states of ASM-based resistive crossbars.

6 Conclusions

In this work, we studied and compared the anti-serial (ASM) and anti-parallel (APM) memristors concept towards the possible solution of the current sneak path problem of crossbar memory arrays. We presented the memory operation principles for both cross-point memristive configurations and described the fundamentals of resistive memories comprising the proposed types of storage cells. Through mathematical analysis and simulations, we explored the performance and efficiency of various crossbar arrays using either ASMs or APMs and derived their pros and cons. We reported how ASMs and APMs could efficiently address the sneak path problem by exhibiting measured resistances which are independent of the stored data distribution within the rest of the memory array. Nevertheless, exclusive of their simpler configuration and operation principles, we finally proved that APMs do not allow for excessive memory scaling because the resulting read-out voltage margins substantially decay with crossbar array size. A novel architectural topology for passive resistive memory systems was also applied to an APM-based crossbar grid and delivered significantly improved read-out voltages, thus contributing even more to address the parasitic conducting problem. The presented comprehensive analysis will certainly be useful to engineers and scientists willing to study the composite operation of serial/parallel memristive configurations and explore their usefulness in a variety of emerging applications.

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