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REVIEW ARTICLE

A comprehensive review and feasibility study of DC–DC converters for different PV applications: ESS, future residential purpose, EV charging

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Abstract

In this paper, a comprehensive review of existing high gain DC–DC converter topologies (cascaded, interleaved and coupled inductor technology) is carried out. This consists of the quantitative, qualitative study of all the converters reviewed. Further, the selection method of converters for photovoltaic (PV) based applications is also accomplished reckoning to the concept of critical duty ratio and practical voltage gain. As the critical duty ratio of any DC–DC converter is depending upon the equivalent series resistance (ESR) of the circuit components, the available methods to determine the values of ESR are also discussed in this article. Again, the feasibility study of such reviewed converter topologies are executed in consideration with the PV application fields such as energy storage system (ESS), residential supply, electric vehicle (EV) charging. At last, the review of the available standards in connection with DC distributed generation system is encapsulated in this article.

Keywords Critical duty ratio · ESS · EV charging · ESR · Feasibility study · Residential supply · Selection of DC–DC converter

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Abbreviations

V_{in}	Input voltage
L_x	Inductor; $x = 1, 2, 3,\ldots$
L_{px}	Primary inductance; $x = 1, 2, 3,\ldots$
L_{sx}	Secondary inductance; $x = 1, 2, 3,\ldots$
S_x	Active switch; $x = 1, 2, 3,\ldots$
D_x	Diode; $x = 1, 2, 3,\ldots$
D	Duty ratio
D_{crit}	Critical duty ratio
V_0	Output voltage
V_{DSx}	Switch voltage; $x = 1, 2, 3,\ldots$
R	Load resistance
R_{Lx}	ESR of L_x; $x = 1, 2, 3,\ldots$
N_{xp}	Primary number of turns; $x = 1, 2$
N_{xs}	Secondary number of turns; $x = 1, 2$
N	Turns ratio
C_x	Capacitor; $x = 1, 2, 3,\ldots$

1 Introduction

In recent days, distributed generation (DG) like grid connected renewable energy sources (RES) has shown a promising solution towards sustainable energy generation. However, penetration of such DG's into AC utility grid may cause voltage rise and protection failure in a large scale. Due to this, the utility grid security, quality, reliability will be of a great challenge. To address these issues, microgrid and smart-grid concepts have been developed for ensuring future electrical power systems. A micro-grid is a concept of accomplishing low voltage (LV) power network with distributed energy sources such as Solar photovoltaic (PV), wind energy, fuel cell, energy storage system (such as battery, super capacitor, flywheel etc.) by offering enhanced controlling feature through network operation. There can be a bidirectional power flow between microgrid and utility grid subject to demand – supply characteristics. While fault occurs on either of the grids, microgrid becomes disconnected from the utility grid and operates as in islanding mode. This enables the microgrid with enhanced power security, reliability and quality of the grid and the customers connected to the grid as well [1–3].

The requirement of energy storage in electricity networks arises especially when RES is used to generate more capacity because of inherently intermittent behavior of renewable sources. Maintaining power quality with increased renewable inputs becomes inefficient and needs proper optimization. These solutions are expensive and complex. However, energy storage in batteries becomes attractive because of their compactness, user friendly nature, cost effectiveness, fast response in battery to network and vice versa. Various other features also intend the use of batteries to the grid that offers reliable, economic solution to be adapted for various energy storage applications [4].

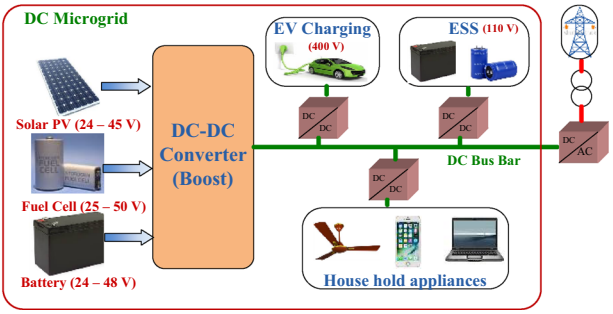

Fig. 1 Building block of DC microgrid system connected with ESS, residential supply, EV charging

Moreover, nine countries and regions, including the United States, the European Union have taken up standards for passenger cars and light-weight vehicles emission [5]. In European Union, CO_2 emission per driven kilometer is confined to an average of 95 g for a passenger car registered after 2020. To meet this goal to reduce emissions sufficiently, vehicle manufacturers are required to electrify the fuelling system of most of the cars they produce [6, 7]. Thus the world is now moving towards a revolution of electric vehicles (EV) and their impactful connections with the LV distribution is substantially enhanced. Further, in the industries and residences, several adjustable AC drives are used, increasing the use of multistage conversion with AC-DC and DC-AC converters. These multiple conversion can lead to the decrement of overall efficiency and reliability. However, the reduction in conversion stages can aggravate the efficiency level implementing DC–DC converters which can be connected directly to the DC grid. It seems recent development in power system can be empowered through ESS, future residential supply and EV charging through microgrid and smart grid. The basic block diagram of DC microgrid system along with ESS, EV charging and residential supply network is shown in Fig. 1.

Further, high usage of fossil fuels has led to adverse environmental effect, such as Greenhouse Effect [8–10] and its excessive usage does not contribute to sustainable development for future generation. This leads to searching of alternative energy source, i.e., RES. Among the RES, solar photovoltaic (PV) is a promising alternative and readily available in a mass. But this solar energy is extracted in an unregulated form; at the same time, few other issues like weather and shading effects are the key constraints while extracting solar energy. Other renewable energy sources like fuel cell (25–50 V) are required to be lifted up to a standard dc bus voltage of 380–400 V [11]. Likewise, 14 V or 42 V from energy storage devices are required to be boosted up to 200 V DC or 500 V DC during various modes of operation in Hybrid Electric Vehicle (HEV) and other electric traction systems [12]. The emergence of 380 V DC distribution systems instead of conventional 48 V DC distribution systems for data and communication centre subsequently increases demand for high step-up DC–DC converters [13]. Thus there is an increasing demand for high gain DC–DC converters for various applications. [15–17].

Overall, there are various other advantages of DC grid system as stated here:

- According to the requirement of environmental agencies, the emission of harmful gases like CO_2 has to be minimized that caused because of the combustion of fossil

fuels. Use of RES can compensate such emissions caused during power generation. Though the efficiency of solar PV is around 17% [18], the overall efficiency can be increased with reducing the number of conversion stages. This can be achieved by DC grid system [19–21].

- Since skin effect is not appearing in the case of DC grid system, current can flow through the whole cable uniformly. This increases efficiency of transmission and also the cost of transmission and distribution can be minimized by using a thinner cable for the same amount of current [22].
- Complexity of the system can be reduced as there is no requirement of synchronization of RES with grid system and reactive power control as well [1].
- A better control, stable and reliable operation, improved power quality of the system can be attained with DC microgrid even at any grid disturbances [1].

There are various technologies and topologies of DC–DC converters available for attaining high voltage gain purpose. But every topology itself has some limitations. All such topologies are not capable of providing sufficient voltage gain or may be achieved with larger duty ratio. Now, this also can cause various disturbances including reduced efficiency, increased voltage and current ripples. This further compels the designer to increase the size of the filter components making the converter bulky with substantial cost hike. Hence, the DC–DC converter has to be wisely chosen for specific application. This paper introduces some critical factors which are to be considered during selection of DC–DC converters for PV application. Among various available technologies, this review has selected only the cascaded, interleaved and coupled inductor technology for the application in ESS, residential supply and EV charging purposes.

There are a number of review related article of DC–DC converters which are available in the existing literature; some of these are discussed in [123, 135, 136]. A review of coupled inductor boost converters in connection with derivation methods, interconnections, pros and cons are discussed in [123]. In [135] the recent developments of DC–DC converter topologies, design and applications are reviewed. The performance analysis of different high gain non-isolated DC–DC converters is reviewed in [136]. However, this paper reviews the cascaded, interleaved and coupled inductor based DC converter technologies which are included in Sect. 2. Along with this, estimation of critical duty ratio is carried out in Sect. 3. In Sect. 4, various methods of ESR estimation are suggested. Further, the selection method of DC–DC converters for solar PV based application considering the critical duty ratio, maximum practical voltage gain of the converter is suggested in Sect. 5. In addition to that, different existing standardization techniques of DC distributed power generation system are included in Sect. 6. The conclusion part is discussed in Sect. 7.

2 Review of converter topologies

2.1 Conventional boost converter technique

The basic high step up DC–DC converter is the Conventional Boost converter (BC) as shown in Fig. 2, where V_{in} is the input voltage, V_0 is the output voltage. Ideally

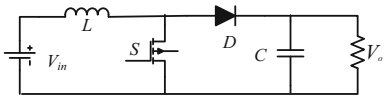

Fig. 2 Conventional boost converter

with extreme high duty ratio (i.e. D almost equal to 1), infinite gain can be obtained. However, practically, BC performance is not satisfactory; like it has poor efficiency with large output diode reverse recovery loss. The current and voltage ripple increases with the increase in duty ratio, leading to greater conduction loss. The size of the inductor and capacitor needs to be large so as to compensate high current and voltage ripple. Owing to increased filter inductor, Electromagnetic Interference (EMI) value and converter size increased. Also voltage stress on switch is equal to the output voltage which makes the switch and converter expensive. Due to these limitations, improved topologies having lesser losses and hence, higher efficiency are introduced [23–25]. Applying volt-sec balance on the inductor, steady state parameters (in ideal condition) of the converter can be achieved as,

$$\text{Voltage gain, } M = \frac{V_0}{V_{in}} = \frac{1}{1-D} \tag{1}$$

$$\text{Voltage stress on switch, } V_{DS} = \frac{V_{in}}{1-D} \tag{2}$$

So it is reasonably accepted that BC is simple and has adequate capacity to voltage build up in the applications where higher voltage gain is not essential. Thus, it is recommended for low or medium voltage range applications.

2.2 Cascade technology

The drawback towards attaining high gain of basic boost converter can be eliminated using a cascade connection of two or more BC with a consideration of increase in power loss and control complexity [26–30]. Cascade boost converter (CBC) [30] as shown in Fig. 3a has the capability to provide large voltage gain, though this converter has a limitation of large input inductor current conduction that causes considerable power loss. A modified topology is suggested in [29] to reduce the inductor conduction losses and thus to increase efficiency shown in Fig. 3b. This topology has the advantage of reduced input current root-mean-square (RMS) value. At the same time, the second inductor (L_2) ripple current is also reduced compared with CBC leading to reduced inductor size. In practical case, it is seen that the voltage output of this converter is somehow more compared to conventional CBC because of the effect of less ESR value pertaining to smaller inductor size. However, CBC has some disadvantages like use of more active and passive elements, enhances the chance of reduced efficiency. To address these issues, a new converter is proposed in [34–38] namely quadratic boost converter (QBC) as shown in Fig. 3c with a reduced number of active switch but maintained the same voltage gain. Now this converter still faces the difficulty of increased voltage and current stress on the switch [24]. In [39], a new methodology proposed to further enhance the voltage gain of QBC with a reduced voltage stress on the switch.

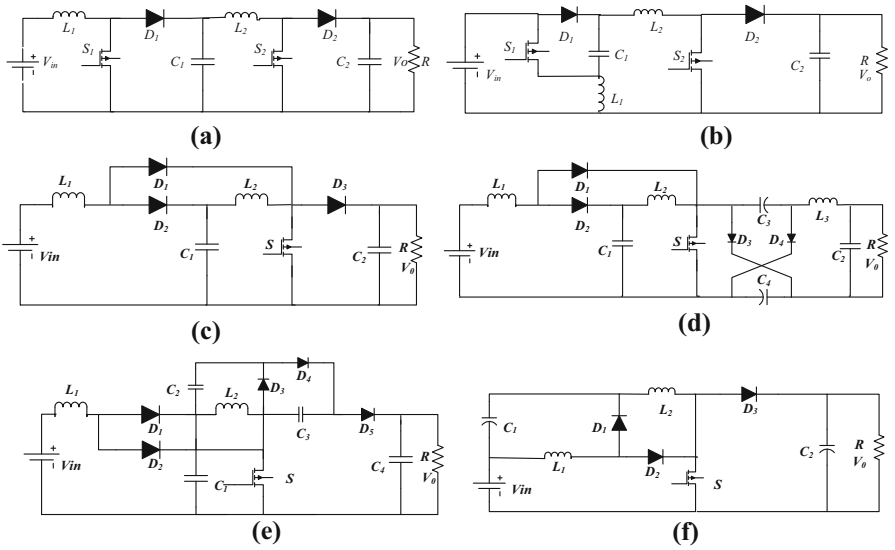

Fig. 3 **a** Cascade boost converter [30]. **b** Modified cascade converter [33]. **c** Quadratic boost converter [37], **d** QBC with CLD [39], **e** QBC with voltage lift technique [41], **f** QBC with reduced voltage stress on buffer capacitor [46]

The modification is proposed with an add-on namely capacitor–inductor–diode (CLD) cell with the conventional QBC as shown in Fig. 3d. The voltage stress on the switch is reduced in comparison with QBC. The control strategy for this QBC-CLD converter is discussed in [40]. However, a further higher voltage gain i.e. double of that of QBC is obtained with a converter proposed in [41]. The modified voltage lift circuit shown in Fig. 3e is used to achieve this higher voltage gain. But the analysis shows that the advantages of such converter are available when duty ratio is more than 0.59. A two phase interleaved QBC technique is analyzed in [42] with a consideration of different inductor models. Few control topologies such as average current control method [38], voltage mode control [43], current mode control [44] and sliding mode control [47] of cascaded technology are available in the literature.

A modified topology is proposed in [46] to minimize the voltage stress on the buffer capacitor C_1 as shown in Fig. 3f. This will reduce the capacitor rating and thus the cost of the capacitor.

Apart from the advantages mentioned for QBC–CLD topology, it has some genuine disadvantages such as increased component count of QBC–CLD topology incurs lower efficiency and higher cost compared to CBC. At the same time, QBC with buffer capacitor also faces the difficulty of higher inductor current rating for L_2 as voltage applied to it is $(V_{in} + V_{C1})$ which is more compared in the case of CBC. This leads to increased size of the inductor and cost investment.

2.3 Interleaved technology

Basic Boost converters or cascade converters face a difficulty of higher input current ripple leading to increase the size of the inductor as well as cost. A solution to this

problem is the interleaved connection of N number of switching legs where the gate signal for each leg is shifted by an angle $360°/N$. The current of each leg becomes $1/N$ times of input current with a numerous benefit of reduced switch rating, as well as inductor size. Further, voltage ripples are also reduced by a factor $1/N^2$ due to the phase shifting feature of the gate signals [47].

The conventional interleaved boost converter (IBC) proposed in [48, 49] is a two leg configuration as shown in Fig. 4a. This configuration reduces the current stress on the switches and inductor ripple current. Though the disadvantages such as voltage stress on the switches and the diodes equals with the output voltage and the reverse recovery problem on the diodes does not appreciate converter efficiency. The main issue is with the voltage gain that remains equal to conventional BC. Thus basic IBC is not appreciable for high power applications [50].

As the conventional IBC is the parallel combination of two basic BC sharing the same input and output voltage, current sharing among them becomes a great trouble for high power application. The converter with larger duty ratio may be operated in continuous conduction mode (CCM) and smaller duty ratio converter in discontinuous conduction mode (DCM). Such mismatches in duty ratio create a problem with current sharing [51]. A coupled inductor based IBC is proposed in [51] shown in Fig. 4b with a proper current sharing characteristics even when large duty ratio mismatch appears. There are few other advantages of this topology [51] like zero reverse recovery loss of the converter, current sensor is not required, inductor cost reduces as both the inductors use the same core.

A generalized steady state analysis for multi-phase IBC with coupled inductor is shown in [54]. However, the use of coupled inductor topology faces the difficulty caused due to leakage energy release. Few topologies proposed in [55, 56] uses passive clamp circuit shown in Fig. 4c–d, respectively which leads to recycling of leakage energy. Moreover, the voltage stress on the semiconductor switches is also reduced with these modifications with increased overall converter efficiency.

In [47], a new approach was suggested with 3 leg configuration of IBC useful for high power applications. The configuration is shown in Fig. 4e. Nine times reduction in input current ripple and three times reduction in current through each interleaved leg are observed with this modification. A reduced inductor size also enabled an easy installation of it onto the PCB [47].

The topologies shown in Fig. 4a, b, e are not appreciated for higher voltage gain as their output voltage equals with the conventional BCs. A method to enhance the voltage gain using diode–capacitor voltage multiplier cell (VMC) is proposed in [57]. The use of one VMC can add two times more voltage as that of a conventional IBC. Thus the use of m number of VMC stages can provide a voltage gain of $(2m+1)$ times as that of conventional IBC. But a trade-off between number of VMC stages and efficiency is a great concern in this regard. Besides, it shows a lower voltage stress on the semiconductor devices comparing with output voltage. Advertently, the use of VMC may lead to reduced voltage stress on components compared to BC, CBC and Flyback converters topologies too. But the floating position of the load is a disadvantage to the system. A single stage VMC-IBC is shown in Fig. 4f.

A topology shown in Fig. 4g is proposed in [58] with a further voltage gain based on coupled inductor concept combined with voltage doubled module, but with reduced

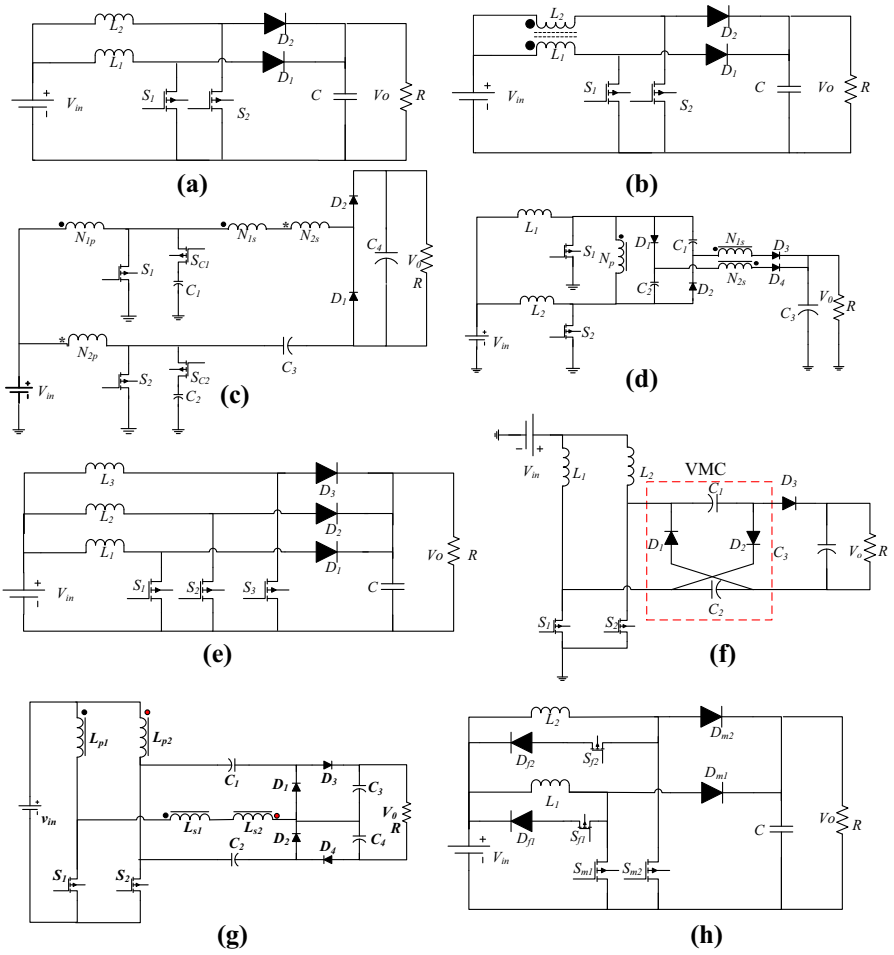

Fig. 4 **a** Conventional IBC [48], **b** IBC with couple inductor [51], **c** topology proposed in [55], **d** passive clamp circuit based topology [56], **e** three leg IBC [47], **f** topology with single stage VMC [57], **g** IBC with voltage doubled module [58], **h** interleaved tri-state boost converter [59] with eliminated RHP zero

circuit element. This also provides a reduced voltage stress on the semiconductor switches and diodes resulting in a cost efficient solution of high voltage gain using IBC technology.

IBC has a common problem of non minimum phase as seen when control to output transfer function is derived in CCM operation. This happens due to the presence of Right Half Plane (RHP) zero in the transfer function. A solution to it is provided with a parallel combination of two Tri-state boost converters (TBC), leading to elimination of RHP zero as stated in [59]. This topology has all the basic benefits of IBC with TBC and thus named as Interleaved TBC (ITBC) shown in Fig. 4h.

Apart from all these topologies, a family of two-phase IBC topology combined with VMC is proposed in [60] for high gain purpose.

2.4 Coupled inductor technology

The Coupled inductor based boosting technique has emerged as it shows two degree of freedom introduced by assigning turns ratio in addition to duty cycle to attain high voltage gain [61–65]. However, proper snubber circuit is required to be installed in this type of converters to absorb stored energy in the leakage inductors leading to complex circuit and reduced efficiency [64]. Few solutions are cited in [66–71] using active clamp technique to suppress voltage spikes and leakage energy recycling to the load. Still the effect of resonance is possible between leakage inductor and parasitic capacitor of load side diode. Modelling of coupled inductor based power converters is shown in [72].

The basic (conventional) non-isolated coupled inductor (CI) based boost converter is proposed in [73] as shown in Fig. 5a. It can be seen that a passive clamp circuit is introduced in between the two coupled inductors. However, this clamp circuit also works as a snubber circuit to protect the switch from over voltages caused due to the non-ideal coupling between the inductors. However, the leakage inductance and the parasitic capacitor of the output diode can introduce EMI problem because of resonance resulting in reduced efficiency. A modified circuit is proposed in [74] with a switched capacitor and a diode to handle this issue. The diode reverse-recovery problem is also minimized with this solution. Further, the voltage stress on the switch and the diode is reduced along with an increase in the voltage gain. The circuit is shown in Fig. 5b. Some of the similar kind of topologies are proposed in [75–78] adopting different voltage multiplier techniques. The authors of [79–81] have shown different three winding techniques to develop higher voltage gain.

An integrated CI and switched capacitor (SC) based converter is proposed in [82] where the capacitors are charging in parallel and discharging in series (Fig. 5c). This results in an enhancement of voltage gain and the leakage energy is recycled with a passive clamping circuit. Further the use of soft switching in conduction state transition of the switch and the diodes increases efficiency of the converter.

Another modification is suggested in [83] combining the concept of CI with SC as shown in Fig. 5d. This improvement enhances the voltage gain, along with absorption of leakage energy rather than employing additional snubber circuit.

A switched coupled inductor topology is derived in [84] as shown in Fig. 5e. Apart from high voltage gain, this converter adopts higher efficiency owing to the use of less number of components. This converter can be utilized to achieve further higher voltage gain by connecting in cascaded form.

The conventional flyback converter is the basic isolated coupled inductor (CI) technology having a high gain capacity with reduced efficiency as the leakage energy cannot be recycled. This feature does not appreciate the use of this converter in low power applications. In [85], the boost converter is combined with the flyback converter where the outputs of both the converters are cascaded as shown in Fig. 5f and thus the voltage gain is enhanced. Here, BC acts as a clamp circuit when active switch gets turned OFF [86].

The authors of [87] derived a modification to the topology proposed in Fig. 5f where clamped capacitors were used at the secondary coupled inductor. Thus the voltage gain

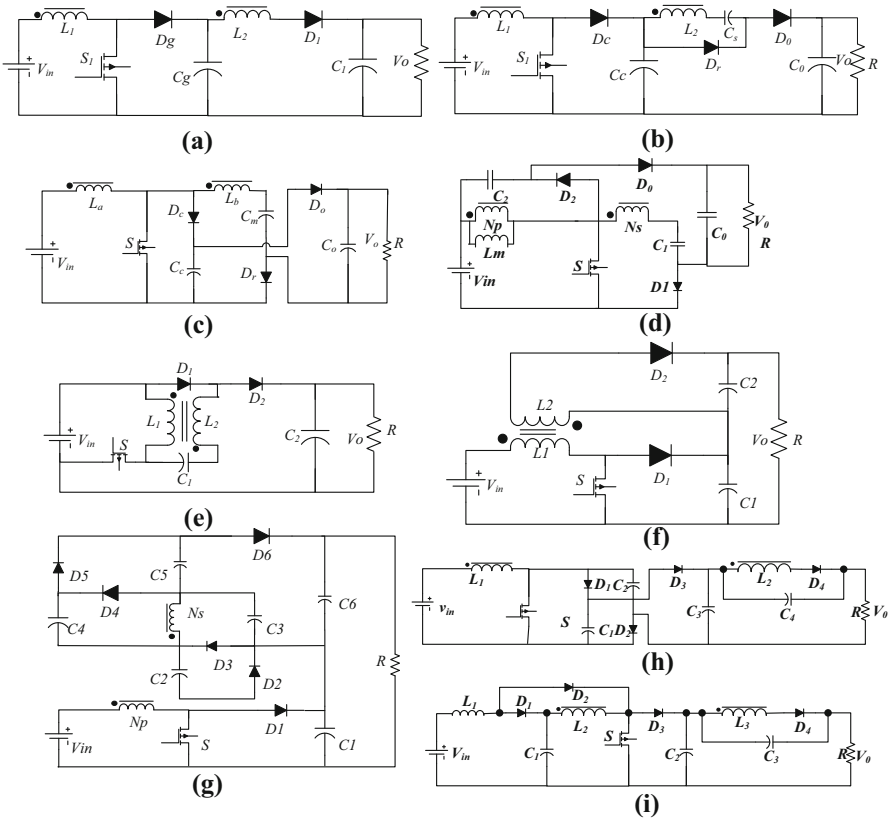

Fig. 5 **a** conventional coupled inductor BC [73], **b** coupled inductor with clamped circuit [74], **c** SC combined topology [82], **d** topology proposed in [83], **e** topology proposed in [84], **f** flyback based topology [85], **g** flyback with clamped capacitor [87], **h** CI-SC based converter [88], **i** QBC-CI combined topology [97]

is enhanced. The voltage stress of the switch is clamped in this circuit appreciating the use of low rated switches leading to reduction in switch conduction loss as well as efficiency enhancement. The circuit is shown in Fig. 5g.

In [88], a derived topology of BC fly-back incorporating SC is shown in Fig. 5h. The capacitors C_1 and C_2 are charged is parallel and discharged in series. Thus voltage gain is increased compared to Fig. 5f and the leakage energy is recycled through the switched capacitors. The circuit complexity is reduced in this topology compared to Fig. 5g. Some converters are proposed in [89, 90] using coupled inductors and three output voltage stacking leading to circuit complexity.

The topologies discussed in [73–96] are not capable of gaining extremely high voltage gain. This problem is addressed with a solution proposed in [97] (Fig. 5i) using a combination of QBC with CI concept. This circuit has the advantages of input current ripple reduction and leakage energy recycling reduces the voltage stress on the active switch. Meanwhile, some derived topologies of QBC-CI based diode clamped solutions are provided in [98–100].

Table 1 Comparative study of number of components and maximum efficiency attained

Technology	Topology	Component count (*S/FI/CI/C/D*)*	Voltage gain, $\frac{V_0}{V_{in}}$	Switch voltage stress, V_{DS}	%efficiency
Boost	BC [23]	1/1/0/1/1	$1/(1-D)$	V_0	–
Cascaded	CBC [30]	2/2/0/2/2	$1/(1-D)^2$	$V_{DS1} = V_0(1-D)$ $V_{DS2} = V_0$	94
	Modified CBC [33]	2/2/0/2/2	$1/(1-D)^2$	$V_{DS1} = V_0(1-D)$ $V_{DS2} = V_0$	98
	QBC [37]	1/2/0/2/3	$1/(1-D)^2$	V_0	–
	QBC-CLD [39]	1/3/0/4/4	$(1+D)/(1-D)^2$	$V_0/(1+D)$	88
	QBC-voltage lift [41]	1/2/0/4/5	$2/(1-D)^2$	$V_0/2$	–
	Topology [46]	1/2/0/2/3	$1/(1-D)^2$	V_0	96
Interleaved	IBC [48]	2/2/0/1/2	$1/(1-D)$	V_0	98.5
	IBC-coupled [51]	1/0/1/1/2	$1/(1-D)$	V_0	93
	Topology [55]	4/0/2/4/2	$1/(1-D)$	$V_0/2(n+1)$ (all switches)	97
	Topology [56]	2/2/1/3/4	$1/(1-D)$	$V_{DS1} = V_0/(2+n) = V_{DS2}$	97
	3 leg IBC [47]	3/3/0/1/3	$1/(1-D)$	V_0	99
	IBC-VMC [57]	2/2/0/3/3	$3/(1-D)$	$V_0/3$	–
	Topology [58]	2/0/2/4/4	$4(1+n)/(1-D)$	$V_o/4(n+1)$	96
	ITBC [59]	4/0/1/1/4	$(4+D)/2(1-D)$	V_0	75
Coupled inductor	Conventional CI [73]	1/0/1/2/2	$(1+nD)/(1-D)$	V_0/nD	95
	Diode Clamp CI [74]	1/0/1/3/3	$(1+n)/(1-D)$	$V_0/(1+n)$	97
	SC based CI [82]	1/0/1/3/3	$(2+n)/(1-D)$	$V_0/(2+n)$	93.5

Table 1 continued

Technology	Topology	Component count (*S/FI/CI/C/D*)*	Voltage gain, $\frac{V_0}{V_{in}}$	Switch voltage stress, V_{DS}	%efficiency
	Topology [83]	1/0/1/3/3	$(2+n)/(1-D)$	$V_0/(2+n)$	96.5
	Topology [84]	1/0/1/2/2	$(2+n-D)/(1-D)$	–	97.2
	BC-flyback [85]	1/0/1/2/2	$(1+nD)/(1-D)$	$V_0/(1+nD)$	96.5
	Topology [87]	1/0/1/6/6	$\frac{1+nD+2n}{1-D}$	$\frac{V_0-nV_{in}}{1+n}$	95
	Topology [88]	1/0/1/4/4	$(2+nD)/(1-D)$	$V_0/(2+nD)$	–
	QBC-CI [97]	1/0/1/3/4	$(1+nD)/(1-D)^2$	$V_0/(1+nD)$	93

Table 2 Summary of the features of converters reviewed

Technology	Topology	Literature	Figures	Remarks	Disadvantages
Cascade	CBC	[30]	Figure 3a	Higher voltage gain capability compared to BC	Increased input inductor current leads to more conduction losses Use of two active switches reduces efficiency, increases cost
	Modified CBC	[33]	Figure 3b	Reduced input RMS current, thus less conduction loss Reduced size of inductor L_2 Practically, converter provides little bit more voltage compared to CBC due to less ESR	Control circuit becomes costlier
	QBC	[37]	Figure 3c	Single active switch reduces cost, switching loss Increased efficiency compared to CBC	Enhanced switch current stress
	QBC-CLD	[39]	Figure 3d	Improved voltage gain compared with conventional QBC Reduced switch and diode voltage stress	Lower efficiency Higher component cost
	QBC-voltage lift	[41]	Figure 3e	Remarkably improved voltage gain i.e. double of QBC Switch voltage stress comes down to half of QBC	Increased component count Reduced efficiency
	QBC with reduced buffer capacitor	[46]	Figure 3f	Reduced buffer capacitor voltage stress Voltage gain is same as QBC	Increased L_2 current rating causing bigger inductor size and cost
Interleaved	IBC	[48]	Figure 4a	Reduced switch current stress, as well as inductor current ripple Smaller inductor size reduces EMI effect Voltage gain and switch voltage stress is same as BC	Output diode reverse recovery problem persists

Table 2 continued

Technology	Topology	Literature	Figures	Remarks	Disadvantages
	IBC-coupled	[51]	Figure 4b	Small input current ripple and nullified reverse recovery loss No need of current sensor Reduction in cost as both inductors uses the same core	Small unbalance in current sharing observed even with a large duty ratio mismatch
	Topology	[55]	Figure 4c	Reduced conduction and switching loss Leakage energy from the coupled inductor is recycled Reduced voltage stress on the semiconductor devices	Higher component count Bulky
	Topology	[56]	Figure 4d	Reduced input current ripple and voltage stress on switch Leakage energy recycled through passive clamp circuit	Higher component count Bulky
	3 leg IBC	[47]	Figure 4e	Nine times reduction in input current ripple Three times reduction in current through each interleaved leg Overall efficiency increased	Bigger size Reduced power density
	IBC-VMC	[57]	Figure 4f	High voltage gain with reduced input current ripple Very less voltage stress compared to output voltage	Floating output may need digital isolation during voltage feedback
	Topology	[58]	Figure 4g	High gain obtained with less component usage Better current sharing with minimized current ripple	Increased voltage stress of the components
	ITBC	[59]	Figure 4h	RHP zero eliminated	Dynamic response is hampered due to non-minimum phase problem

Table 2 continued

Technology	Topology	Literature	Figures	Remarks	Disadvantages
Coupled inductor	Conventional CI	[73]	Figure 5a	Voltage gain depends on duty ratio as well as turns ratio Use of passive clamp circuit acts as a snubber circuit protecting the switch from over voltages	Leakage energy recycling does not possible
	Diode clamp CI	[74]	Figure 5b	Voltage gain more than [73] Reduced EMI problem Leakage inductor energy recycled	Higher component count
	SC based CI	[82]	Figure 5c	Highly efficient Leakage energy recycled through the passive clamp circuit	Ideal capacitor is charged from an ideal voltage source, causing a risky operation
	Topology	[83]	Figure 5d	High voltage gain Leakage energy recycled without any additional clamp circuit	Common grounding problem
	Topology	[84]	Figure 5e	Highly efficient Leakage energy recycled through the passive clamp circuit	Difficult to design C_1 value due to parasitic influence
	BC-flyback	[85]	Figure 5f	High voltage gain achieved without higher duty ratio High efficiency Low switch voltage stress	Higher gain is achieved with increased turns ratio which is uneconomical
	Topology	[87]	Figure 5g	High voltage gain compared to [85] Increased efficiency achieved with reduced on state resistance of the switch Voltage spike of the switch is clamped	Higher component count

Table 2 continued

Technology	Topology	Literature	Figures	Remarks	Disadvantages
	Topology	[88]	Figure 5h	More voltage gain and reduced switch voltage stress compared to [85] Leakage energy recycled to SC capacitor leads to increased efficiency	Charging of capacitor is accomplished without any current limiting arrangement
	QBC-CI	[97]	Figure 5i	High voltage gain with appropriate duty ratio Low switch voltage stress Leakage inductor energy recycled to output capacitor	Higher switching current stress

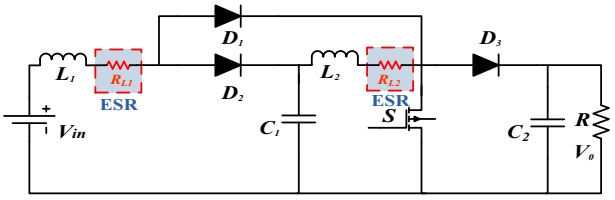

Fig. 6 QBC with inductive ESR

The comparative study and the features of the reviewed converters are summarized in Tables 1 and 2 respectively.

3 Estimation of critical duty ratio

Ideally a DC–DC converter (e.g. QBC mentioned in [37]) can provide infinite voltage gain when D closes to unity as shown in the voltage gain equations in Table 1. But practically, the components used in the converter possess parasitic resistance, i.e. ESR connected in series with each element. This ESR may be the value of wire resistance also and hence becoming very less. Still considering their presence in the circuit, the voltage equation cannot be same as shown earlier. However, the ideal equation can be achieved by considering all parasitic values equal to 0. In this section, the impact analysis of ESR is carried out taking into account the inductive ESR values R_{L1} and R_{L2} for inductors L_1 and L_2 respectively of QBC as shown in Fig. 6.

Applying volt-sec balance on the inductors L_1 and L_2, the voltage gain of the converter shown in Fig. 6 can be derived as in [23],

$$\frac{V_0}{V_{in}} = \frac{(1-D)^2 R}{R_{L1} + (1-D)^4 R + (1-D)^2 R_{L2}} \tag{3}$$

Eqn (3) states clearly that the voltage gain of the converter cannot be infinite even with unity value of D. The relation of voltage gain with variation of duty ratio is shown in Fig. 7a, where the gain is estimated in ideal condition as well as with different ESR values. It is apparent that the voltage gain of the converter reduces with the increase in ESR value. In practical case, the voltage gain of this converter will further be reduced by considering the parasitic value of all elements. However, the voltage gain becomes maximum with a duty ratio called critical duty ratio, D_{crit}. In normal mode there are three regions of duty ratio:

- $D < D_{crit}$: positive voltage gain in connection with the same characteristics of ideal condition.
- $D = D_{crit}$: maximum voltage gain obtained.
- $D > D_{crit}$: negative voltage gain area where gain reduces with increase in duty ratio.

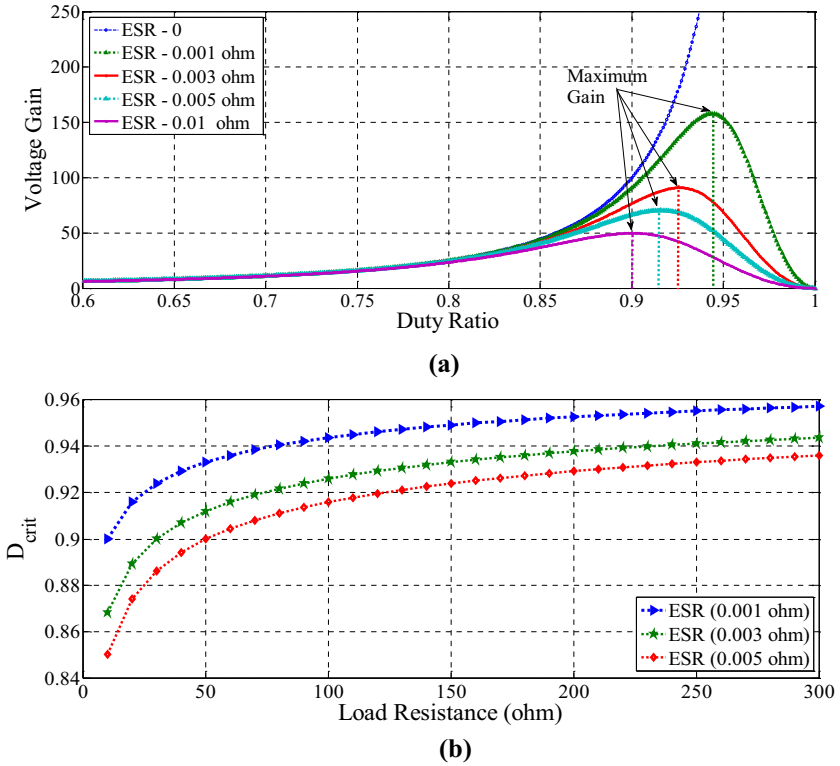

Fig. 7 Variation of **a** voltage gain with different ESR value, **b** D_{crit} with load resistance considering inductive ESR value of QBC

So the relation between D_{crit} and the parasitic elements can be obtained when $\frac{d\frac{V_0}{V_{in}}}{dD} = 0$. The relation is obtained as,

$$D_{crit} = 1 - \sqrt[4]{\frac{R_{L1}}{R}} \tag{4}$$

The relationship is shown in Fig. 7b where it is seen that the value of D_{crit} reduces with increase in ESR value. However, for any specific ESR value, the duty ratio range increases with increase in load resistance. Looking into such constraints, the maximum duty ratio of any converter has to be confined within 0.8 or less than that. Here for simplicity and understanding purpose, the critical duty ratio, D_{crit} has been limited to 0.8 for all the converters in this paper.

Inserting D_{crit} into Eq. (3), the relation between voltage gain and ESR value is obtained as,

$$\frac{V_0}{V_{in}} = \frac{\sqrt{RR_{L1}}}{2R_{L1} + \sqrt{\frac{R_{L1}}{R}R_{L2}}} \tag{5}$$

For simplification of calculation, $R_{L1} = R_{L2}$ is considered in Eq. (5) and thus obtained as,

$$\frac{V_0}{V_{in}} = \frac{\sqrt{R}}{\sqrt{R_{L1}}\left(2 + \sqrt{\frac{R_{L1}}{R}}\right)} \tag{6}$$

The ratio R_{L1}/R shown in Eq. (6) is very small and can be ignored. So for a given load resistance,

$$\text{Voltage gain} = \frac{V_0}{V_{in}} \propto \frac{1}{\sqrt{R_{L1}}} = \frac{1}{\sqrt{\text{ESR}}} \tag{7}$$

Eqn (7) shows the relation between voltage gain and ESR value of the component(s). It is apparent from the relation that the voltage gain reduces with enhanced value of ESR. Thus for any high gain converters, where more number of passive elements are used, can face the difficulty of voltage gain reduction with increase in ESR value.

So to select a converter for any specific application, the concept of critical duty ratio, impact of ESR with number of elements used is the key attribute to trade-off.

4 Methods for estimation of ESR value

For wise selection of a DC–DC converter, range of critical duty ratio selection is an essential requirement. To accomplish this properly, the estimation of ESR value is also important. Since the value of ESR is an inherent part of any element, it is tough to measure the value directly. Thus there are few indirect methods available to get estimation about this parameter.

Recently, the concern over ESR estimation has been proven with a numerous research going on in this matter. The ongoing research estimates the electrolytic capacitor health condition and/or aging effect with an estimation of ESR values. Usually, the generic curves provided by manufacturers show the temperature effect on ESR for their products. The values for the components of the model can be estimated by using these curves with ripple current multipliers. But a more accurate result is achieved by experimentally measuring the ESR over a range of temperature and frequency.

Mainly there are two techniques available as per literature survey for ESR estimation—offline method and another is online method or based on a combination of signal monitoring and signal processing.

The first technique was implemented by Riz et al. [101] where the related measurements were taken up by using inner gas pressure. A method to predict bus capacitor life addressing the problems with an ESR estimation model out of inner gas pressure and temperature was proposed by Gasperi et al. [102] and Sankaran et al. [103]. In [104], a simple offline method is proposed with a resistor—capacitor network. The ESR value is estimated by the resultant impedance vector through Fast Fourier Transform (FFT). Another approach discussed in [105] using Least Mean Square (LMS) algorithm to

estimate ESR. These methods are cheaper, simple and accurate but are not feasible for real time monitoring.

Second technique is established with real time signal monitoring and signal processing principle to estimate the value of ESR. Most of the methods in this technique are used for power converter's health condition monitoring. Buiatti et al. [106] proposed an approach for ESR estimation using simplified regression model. This method has the advantage of faster calculation. Even it has been suggested for BC due to reliability factor and effectiveness of ESR extraction using this method. Leite et al. [107] suggested an identification methodology considering simple continuous time model and some recursive prediction error models. A Kalman filter based real time approach is proposed by Abdennadher et al. [108]. Pang et al. [109] proposed an ESR estimation method by predicting current waveform. In this method, capacitor current waveform was predicted without any current sensor using repetitive sampling on the switch current at capacitor nodes. The acquired voltage is then used to predict the ESR value. Anderson et al. [110] designed an online capacitor health monitoring system where the component current and voltage were measured and sampled at higher frequencies. The ESR is ultimately calculated using FFT (Fast Fourier transform) of the frequency spectra of these sampled quantities. Empirical Mode Decomposition (EMD) [111] is a popular method used in multidisciplinary signal analysis. ESR analysis using an improved EMD algorithm is proposed by Wang et al. [112]. This method focuses on detection of changes online in real time ESR values of electrolytic capacitors. EMD algorithm provides number of Intrinsic Mode Functions (IMF) from the output voltage and current The ESR values are then computed based on the analyzed values of ripple voltage and current signals using Hilbert transform. This method is advantageous as it can deal with online non-linear data, where dc power is a combination of linear and non-linear coupling. A high resolution spectral analysis technique based on Short Time Least Square Prony's (STLSP) is proposed by *Laadjal* et al. [113]. This method has the quality of tracking all the harmonic attributes (frequency, amplitude, phase, damping factor) accurately. This is extracted from a short data record signal allowing the consideration of non- stationary aspect of the problem. The ESR value is achieved with the ratio of amplitudes of voltage and current of switching frequency harmonics. A band pass—filter based technique is proposed by Sundararajan et al. [114] which uses switching frequency component of DC link voltage and current to estimate ESR. Agarwal et al. [115] proposed a quasi online method for health monitoring of capacitor in solar inverters. In this method, inverter injects current as per IEEE 929-2000 standard with different odd harmonic frequencies. The impedance of DC link capacitor is evaluated at various frequencies. Thus these impedance values are used in LMS algorithm to find ESR values. Arya et al. [116] proposed a method to find ESR using DC—link voltage oscillations in inverters. This method apprises for estimation of ESR value by evaluating capacitor impedance at twice the grid frequency i.e. at low frequency. Amaral et al. [117] describes a method using input current and output voltage ripple in step down DC–DC converter for fault detection of capacitors. Several other methods related to ESR estimation are also depicted in [23], [118–122].

Table 3 Feasibility study of duty ratio and voltage stress of cascaded boost converters in different application areas

Application area	ESS (110 V)		Future residential supply (350 V)		EV charging (400 V)	
Topology	D	V_{DS} (V)	D	V_{DS} (V)	D	V_{DS} (V)
CBC [30]	0.53	$V_{DS1} = 51$ $V_{DS2} = 110$	0.74	$V_{DS1} = 92$ $V_{DS2} = 350$	0.76	$V_{DS1} = 96$ $V_{DS2} = 400$
Modified CBC [33]	0.53	$V_{DS1} = 51$ $V_{DS2} = 110$	0.74	$V_{DS1} = 92$ $V_{DS2} = 350$	0.76	$V_{DS1} = 96$ $V_{DS2} = 400$
QBC [37]	0.53	110	0.74	350	0.76	400
QBC-CLD [39]	0.44	76	0.66	211	0.68	238
QBC-voltage lift [41]	0.34	55	0.63	175	0.65	200
Topology [46]	0.53	110	0.74	350	0.76	400

Table 4 Feasibility study of duty ratio and voltage stress of interleaved converters in different application areas

Application area	ESS (110 V)		Future residential supply (350 V)		EV charging (400 V)	
Topology	D	V_{DS} (V)	D	V_{DS} (V)	D	V_{DS} (V)
IBC [48]	0.78	110	0.93	350	0.94	400
IBC Coupled [51]	0.78	110	0.93	350	0.94	400
Topology [55]	0.78	28	0.93	88	0.94	100
Topology [56]	0.78	37	0.93	117	0.94	133
3 leg IBC [47]	0.78	110	0.93	350	0.94	400
IBC-VMC [57]	0.35	37	0.79	117	0.82	133
Topology [58]	NA	NA	0.45	44	0.52	50
ITBC [59]	0.51	110	0.83	350	0.85	400

5 Selection of DC–DC converter

In this section, the selection method for DC–DC converter topologies based on cascaded, interleaved and coupled inductor technology are discussed. Initially, a feasibility study of the reviewed converters [30–97] is carried out (Table 3 for cascaded converters, Table 4 for interleaved technique and Table 5 for coupled inductor technique) in terms of the required duty ratio and the voltage stress on the active switch. This study is taken place in consideration with the application in ESS (110 V), residential supply (350 V) and EV charging (400 V). The converters are supposed to step up the 18-36 V (nominal voltage of 24 V) to the above mentioned application voltage levels. The relevant equations for all the converter topologies are shown in Table 1. Additionally, a summary of the reviewed topologies are shown in Table 2.

Table 5 Feasibility study of duty ratio and voltage stress of coupled inductor converters in different application areas

Application area	ESS (110 V)		Future residential supply (350 V)		EV charging (400 V)	
Topology	D	V_{DS} (V)	D	V_{DS} (V)	D	V_{DS} (V)
CCI [73]	0.64	172	0.87	402	0.89	449
Diode clamped CI [74]	0.56	55	0.86	175	0.88	200
SC CI [82]	0.35	37	0.79	117	0.82	133
Topology [83]	0.35	37	0.79	117	0.82	133
Topology [84]	0.44	–	0.79	–	0.87	–
BC-FB [85]	0.64	66	0.87	187	0.89	212
Topology [87]	0.28	43	0.74	163	0.77	188
Topology [88]	0.46	45	0.81	125	0.83	141
QBC-CI [97]	0.44	76	0.66	211	0.68	238

While selecting any converter the following benchmarks are to be taken into account:

- Critical duty ratio as it is the maximum allowable duty ratio for any practical DC–DC converter. The applied duty ratio if crosses this limit, the gain of the converter is reduced. However, according to the authors of [123], the maximum duty ratio for a converter to be set to 0.65.
- ESR estimation is an inherent part to obtain D_{crit} judiciously. Use of ambiguous or haphazard value of ESR can lead to wrong judgment of D_{crit}.
- For wise and efficient selection of DC–DC converter, the practical voltage gain of the converter with the knowledge of D_{crit} is a must. As can be seen from the feasibility study taken place in Table 3 – 5. Most of the converters are incapable of boosting the desired voltage level and thus are not suitable for the specified application.

The duty ratio and voltage stress on active switch for cascaded technology DC–DC converters are displayed in Table 3. It is observed that all the converters are feasible for ESS application. In case of residential supply or EV charging purpose the converters are unsuitable except the converter proposed in [41] with 24 V input voltage. However, this converter is also marginally suitable as the duty ratio is close to 0.65 or equal in ideal condition and there is possibility of increased duty ratio in practical application. The highlights in 'green' colour signify the suitability and that with 'pink' colour are unsuitable cases. The feasibility study shown in Tables 4, 5 also follows the same principle for interleaved and coupled inductor technology respectively. However, coupled inductor based technologies may be capable of further voltage gain with increased turns ratio 'n'.

Here for all the converters where coupled inductor is used, a turns ratio of $n = 1$ is considered and studied the feasibility. But these converters may be useful if n value considered as 2, 3, 4 and so on, but looking into the constraints of EMI effect, size of the transformer.

As the impact of inductive ESR is more compared to capacitive ESR [23] on the voltage gain, the number of inductors is also required to be kept in mind while selecting any converter. Furthermore, use of increased number of passive elements can contribute more ESR effect, leading to reduction in voltage gain.

6 Standardization of DC distributed power generation system

One of the purposes of DC–DC converters is to supply power to DC micro-grid system and thus such integration immensely requires some standardization aspects to be adopted. These aspects are mainly focusing on voltage standardization for specific application, protection, safety and quality of power to be readily useful. With the increased demand, various National and International bodies have started working in setting up of standardization methods. This section gives some idea about few such standardization prospects.

International Electrotechnical Commission (IEC)—IEC founded IEC founded in 1906 and became World's leading organization by making several International standards for electrical, electronic technologies [124]. It has formed System Evaluation Group (SEG) for setting up standards for low voltage DC applications, distribution and safety for use in developed and developing countries. This mainly works on evaluating the voltage standards, application areas, future applicability etc. [125] Some of their published standards related to LVDC (within 1500 V) are as follows:

- IEC 62040-5-3: 2016—uninterruptible power systems (UPS)-DC output, performance and test requirement
- IEC 61643-32: 2017—Surge protective devices connected to the DC side of PV application.
- IEC 61851-23: 2014—DC electric vehicle charging station.
- IEC 61851-1: 2017-EV conductive charging system—general requirements.

The Institute of Electrical and Electronics Engineering Standard Association (IEEE SA)—IEEE-SA is a leading organization to deal with to maintain unanimity to nurture, develop and advance global technologies under the banner of IEEE. [126] The mission of this organization is to standardize quality and market relevance and to be followed by world-wide. The main goal of this association is to standardize financial sustainability being a learning community [127].

There are various ongoing activities based on the utilization and/or application of DC distributed generation system, some of these are,

- WG 946—the standards set by this working group (WG) has recommended various practices for stored energy based DC auxiliary power system. This mainly focuses on the guidelines to select number of batteries, capacity, level of voltage, maintenance, testing, control mechanism. Few ideas about grounding effect on operation of such DC systems are also described on that [128]. A revised version of this standard is published in 2005 [129].

- P 2030.10—this standard mainly looks after the possibility of Dc micro-grid utilization in remote places where decentralized utility system only exists. This standard provides idea about design, operational and maintenance aspects of DC micro-grid in remote areas. This standard is further useful for fulfilling requirements in low voltage DC/AC power to off-grid loads [130].
- 2030.1.1-2015—this standard is made to fulfill the requirements of DC fast charging methods. The fast charging is associated with rapid energy transfer to plug in vehicles from electric grid [131].

Bureau of Indian Standard (BIS)—looking into the energy efficiency and promotion of renewable energy (mainly solar), in India, BIS has felt the need of preparation of code of practice in guiding and governing the system parameters. In view of this, Electrotechnical Department (ETD) has published ETD 50 aiming to the installation guideline of DC appliances and wiring of DC in residential premises. It is suggested to keep the maximum level of residential supply to 60 V. However, 48 V is selected for distributed generation voltage for DC in consideration with safety, distribution losses. This standard is developed in recognition with DC primary voltage according to IS 12360:1988/IEC 60038 [132].

EMerge Alliance—this standard organization is joint venture of a group of companies, Universities and research laboratories worldwide with a motto to promote the DC distribution system in residential applications. EMerge Alliance provides unexampled design and space flexibility. New options are opened with reduction in energy usage and improved sustainability using these standardization methods. This organization has developed the following standards –

- EMerge Alliance occupied space standard—this standard is focused on 24 V DC distribution system in residential or commercial buildings [1], [133].
- EMerge alliance data/telecom centre standard—the recommended voltage level of this standard is 380 V DC for data centre or telecom applications for reduction of loss and improvement of reliability [1], [134].

7 Conclusion

High gain DC–DC converters are often used for the solar PV applications such as ESS, residential supply and EV charging. Again such use of renewable sources is also a mission for the Government of every Nation. Thus selection of appropriate converter is an essential propaganda for every country promoting solar energy. This paper is so organized to provide the knowledge for selection of DC–DC converter taking into account of critical duty ratio and thus maximum practical voltage gain. In determining the critical duty ratio, the role of ESR value is also demonstrated in this paper. Since ESR value cannot be determined directly, few methods of determining ESR value are also alleviated here. A feasibility study on the reviewed topologies is also carried out citing ESS, residential supply and EV charging application. It is apparent from the feasibility study that most of the reviewed converters are feasible for ESS application with input voltage considered as 24 V and unity turns ratio; but not for residential supply or EV charging. However, these converters can also be made

feasible to be operated with an increase in the turns ratio without considering the effect of EMI, size of the transformer. Furthermore, a compromise is a must to consider the higher value of turns ratio as the EMI effect and the size of the transformer is also plays a major role while selecting a converter. As the standardization is a foremost requirement to design and/or select any converter for any specific application, some available standards related to the above cited application fields are also included in this paper. Thus this paper is helpful in selecting the DC–DC converter judiciously.

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