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ORIGINAL RESEARCH

Design and analysis of low power 8-bit ALU on reversible logic for nanoprocessors

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Abstract
A low power reversible 8-bit ALU using single electron transistor (SET) for Nano processors is designed in this paper. Since there is a possibility in reversible logic to build circuits from many-port gates that do not destroy the capacity to store information, the basic blocks of ALU are constructed using one of the assuring many port gates called DKGP reversible gate. Then the blocks are technologically advanced to the transistor level using CMOS technology. The outputs are verified for given input frequency with the operating voltage of 5 V using SPICE simulation. It is also observed that the output glitches are obtained with low operating voltage of less than 2 V in CMOS technology. The same blocks of ALU are constructed using SET technology and the outputs are verified through simulation. The simulation results have shown that the same output response with no glitches is obtained for the same input frequency as in CMOS, with very low operating voltage of 25 mV. It is inferred that there is a drastic difference in power dissipation with SET and CMOS technology. Therefore SET technology has the potential toward the development of Nano-electronic components and can be adopted for various low power digital applications. This is the first attempt to design reversible ALU using pure SET technology from our study.

Keywords ALU · CMOS · Reversible logic · Single electron transistor

1 Introduction

Today all the VLSI circuits performs on low power with high speed. The ALU operations are essential for low power high speed applications which includes digital signal processing, microprocessor, microcontroller, ASIC, etc., ALU is an onliest combinational logic circuit which entails that the output changes with changing of the input. The ALU is a functional device in microprocessor, performs various logical and arithmetic operations (Rani et al. 2011). Also it represents the fundamental building block of the central processing unit (CPU) of a computer. In this paper, a reversible 8-bit ALU using 8-bit complementing reversible adder, 8-bit reversible multiplier, 4 × 1 reversible multiplexer and other logic gates are designed.

The rapid decrease in the size of the chips has lead to the exponential increase in the number of transistors per unit area. As a result, the energy dissipation is becoming a major obstacle in the evolving Nano-computing era. An operation is said to be physically reversible if there is no energy to heat conversion and no change in entropy. In reversible logic, the state of the computational device just earlier to an operation is solitarily determined by its state just after the operation. In other words, no data about the computational state can ever be lost. Hence the reversible logic can be perceived as a deterministic state machine. Landauer (1961) has shown that for every bit of information that is nullified during an irreversible logic computation kTln2 joules of heat energy is generated, where k is the Boltzmann constant and T is the temperature in Kelvin at which the system is operating. Bennett (1973) showed that the kTln2 amount of energy dissipation would not occur if a computation is carried out in a reversible way. The function f(x1, x2 … xn) of n Boolean variables is known as reversible if:

1. The number of outputs is equal to the number of inputs.
2. Any input pattern maps to a unique output pattern.

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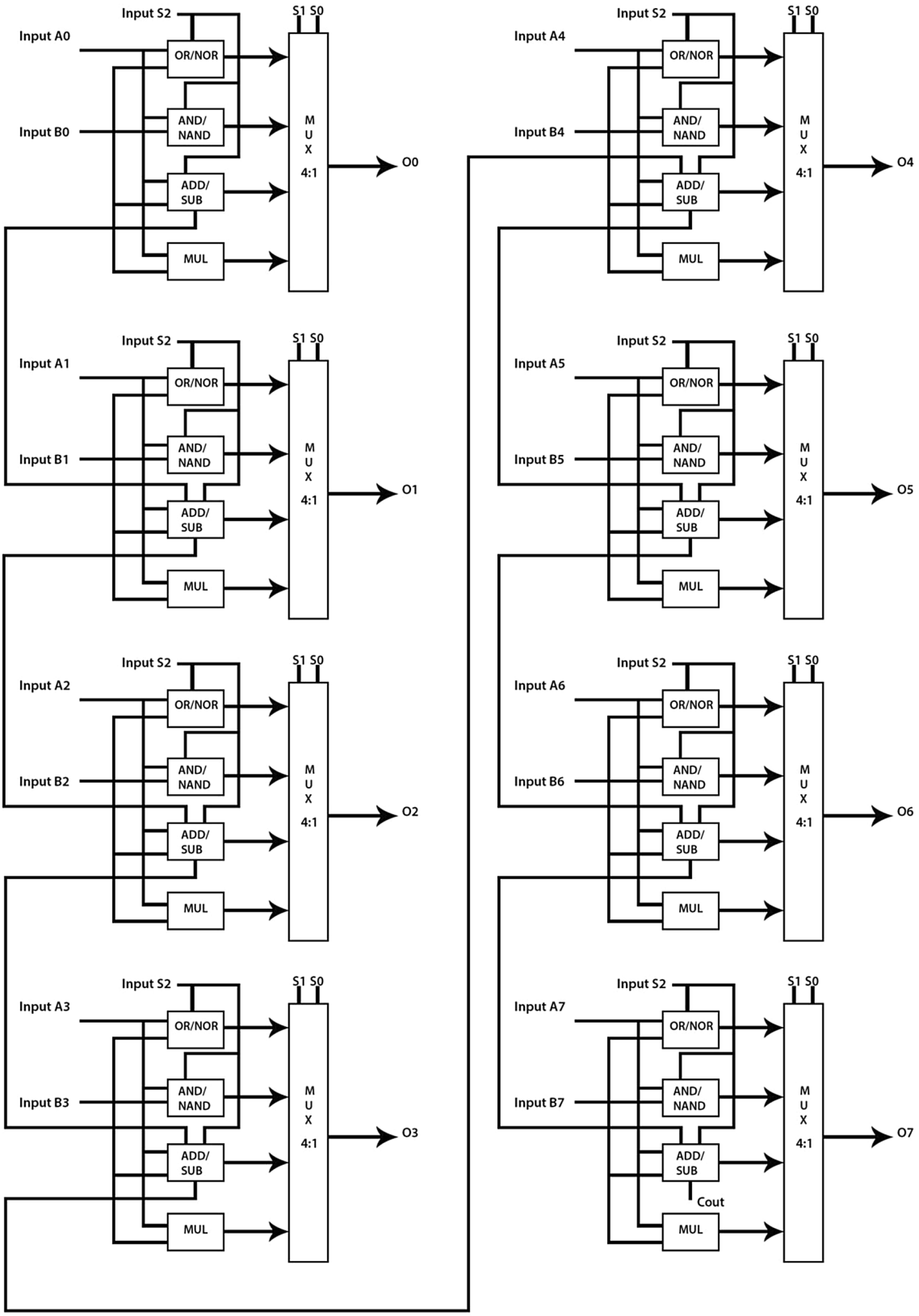

Fig. 1 Block diagram of 8-bit arithmetic and logical unit

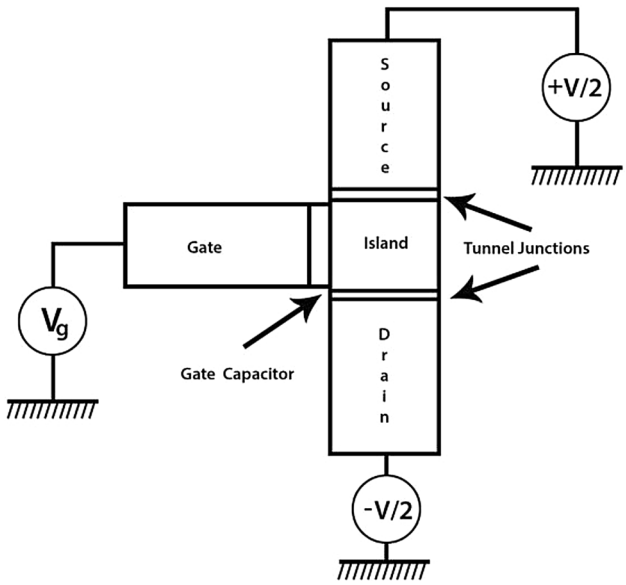

Fig. 2 Schematic structure of SET

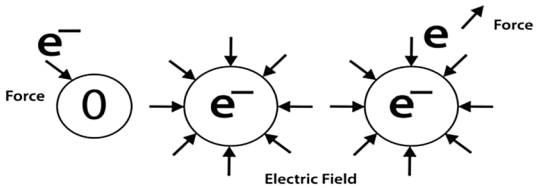

Fig. 3 Concept of single electronics

There are numerous reversible gates available in the market and to name a few such as Peres gate, Tofoli gate, Feyman gate, Fredkin gate, etc., In this paper, one of the reversible gates known as DKGP gate is used. The speciality of DKGP gate is that it can singly function as half adder, half subtractor, full adder and full subtractor. The basic blocks of ALU such as complementing adder, multiplier and multiplexer are first developed using this DKGP gate.

The single electron transistor or SET is a switching device that uses controlled tunneling of electrons to amplify current. This device was chosen due to its Nano feature in size, coulomb blockade characteristics and less power consumption. There are various SET analytical models based on orthodox theory for metallic SETs. An analytical SET model designed for resistively symmetric devices (RS = RD) and valid for $|Vds| < e/C_{\Sigma}$, $C_{\Sigma} = C_S + C_D + C_{G0} + C_{G1}$ (Uchida et al. 2000). Later Inokawa and Takahashi (2003) extended this model to asymmetric SETs but does not account for the background charges effect (see Fig. 1).

A compact MIB model for SET device, which is appropriate for $|Vds| < 3e/C_{\Sigma}$ and temperature of various ranges, and very relevant to single/ multiple gate symmetric/asymmetric device, is chosen for oneway direction flow to reduce the number of exponential terms. MIB model can be adopted for both digital and analog SET circuit design and for both pure SET and hybrid CMOS-SET circuit simulation (Mahapatra et al. 2004). A current conduction model based on the physical properties of the tunnel junctions has been proposed to explain the deviations observed at high temperature between the empirical data and Monte Carlo simulations. The extension of the model consists of thermionic and a field assisted emission component (Dubuc et al. 2009). Another analytical model for SET which describes the drain source current and gate source of single electron transistor at high temperature and it consists on summing up of tunnel current and thermionic current contribution (Touati et al. 2012). In this work,

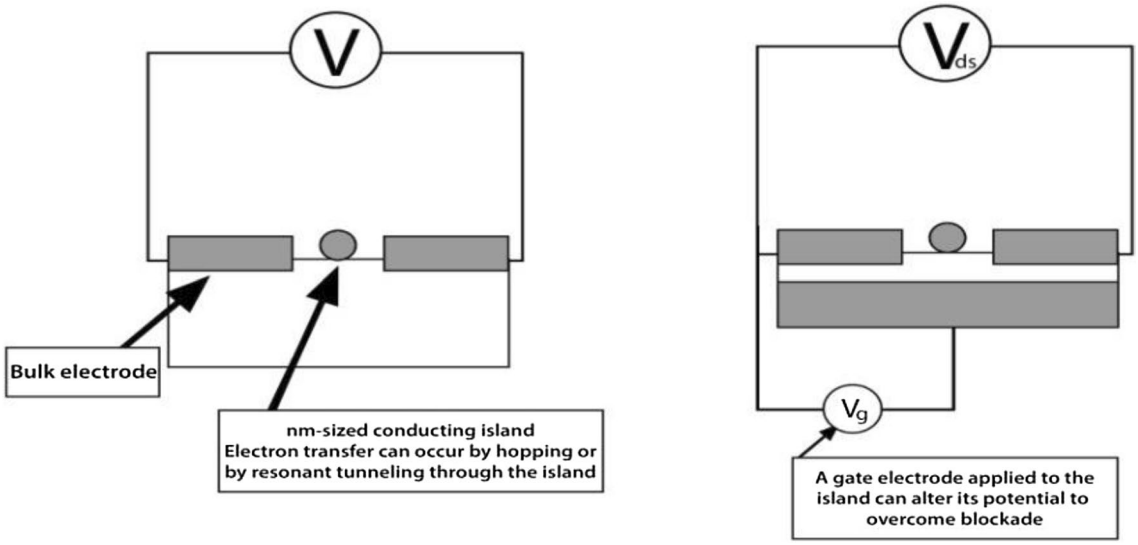

Fig. 4 Coulomb blockade

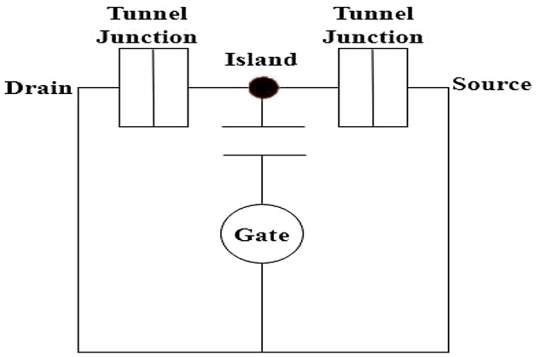

Fig. 5 Single-electron transistor

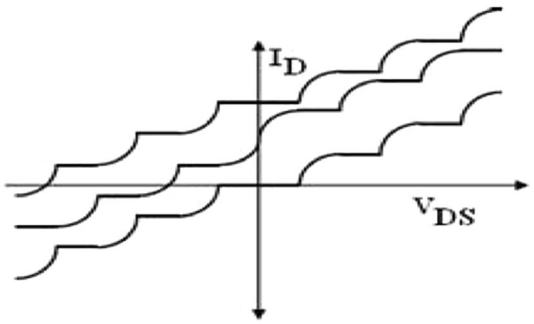

Fig. 6 Coulomb blockade of IDS-VDS. Characteristic as a function of gate voltage

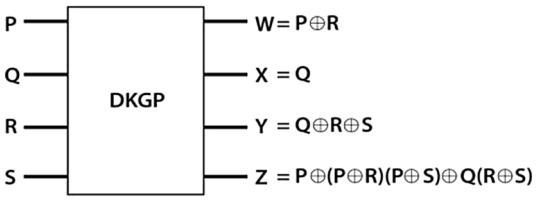

Fig. 7 A DKGP gate

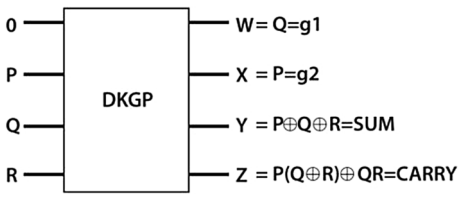

Fig. 8 DKGP gate as a full adder

the basic blocks of ALU based on DKGP gate are advanced to the transistor level by using CMOS and SET technology. The MIB model for SET and available MOS models for CMOS are used. The complete 8-bit reversible ALU block on CMOS and

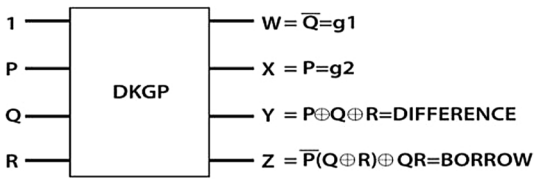

Fig. 9 DKGP gate as a full subtractor

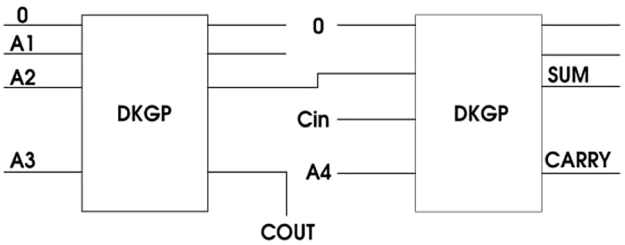

Fig. 10 4:2 compressor using DKGP gate

SET is simulated and verified using SPICE simulation. The Nano processors based on this Nano-ALU can be developed in future which will be more advantageous in three dimensional image technology to speed up the processing and to increase stability(Li and Shiau 2018).

2 Literature survey

For SET modeling and simulation, the electron tunneling and its transition probabilistically are treated by master equation method. The probability of electron tunneling is used to determine the current density in compliance with parameters of selected input (Willy and Darma 2016). In analog switch technique select input logic is used as a control logic and passes through another input signal from the gate terminal (Parihar et al. 2014). FA is a fundamental building block

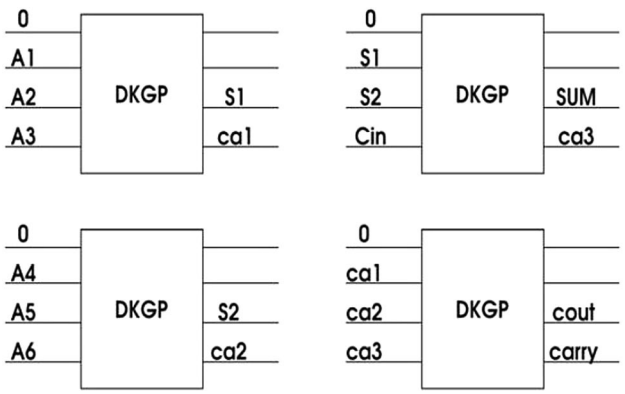

Fig. 11 6:2 compressor using DKGP gate

Table 1 Truth table of DKGP gate

P	Q	R	S	W	X	Y	Z
0	0	0	0	0	0	0	0
0	0	0	1	0	0	1	0
0	0	1	0	0	0	1	0
0	0	1	1	0	0	0	1
0	1	0	0	1	1	1	0
0	1	0	1	1	1	0	1
0	1	1	0	1	1	0	1
0	1	1	1	1	1	1	1
P	Q	R	S	W	X	Y	Z
1	0	0	0	1	0	0	0
1	0	0	1	1	0	1	1
1	0	1	0	1	0	1	1
1	0	1	1	1	0	0	1
1	1	0	0	0	1	1	0
1	1	0	1	0	1	0	0
1	1	1	0	0	1	0	0
1	1	1	1	0	1	1	1

for designing ALU. There are numerous FAs available for dissipation of low power such as hybrid FA, low power 10 transistors FA and 11transistor FA. FA performing in low power mode by using subthreshold current and dissipates low power (Gangadhar Reddy and Ramireddy 2014; Ravindra et al. 2013). FA is made from low power XOR gates and 2 is to 1 multiplexer (Tiwari and Deshmukh 2014). ALU using FinFET technology has two gates which are electrically independent, which results minimum complexity and low power consumption due to the reduction of leakage current. In FinFET technology, a thin silicon "Fin" which mould the body of the device (Dhulipalla and Deepak 2011). The reconfigurable logic of multi input floating gate metal oxide semiconductor (MIFG-MOS) transistor is used for ALU design which improves the circuit functionality. MIFG-MOS transistor gives ON and OFF states of the transistor by observing the sum of the weighted inputs. MIFG-MOS transistor reduces the transistor number, complexity and delay which leads to low power dissipation (Srivastava and Srinivasan 2002). Metal gate and high-k dielectric gives extra channel length without modifying the leakage current (Vaishnav and Moyal 2012). Digital logic gates, synchronous and asynchronous counters, low power 8-bit ALU using full adder and multiplexer have been designed using hybrid CMOS-SET (Sharma and Tiwari 2016; Jana et al. 2013a, b). Buffered threshold logic gates have been used to design 4:1 multiplexer for the feedback effect and to increase the stability (Jain and Sarkar 2012). The low power 16 bit ALU has been designed using hybrid CMOS-SET combinational logic (Jana et al. 2014). The phase-modulated counters with less number of MOSFETs and multi-gate SETs has been designed to deal with temperature effect and reliability improvement (Deng and Chen 2013). The stability analysis of full adder using SET has been analyzed (Mahima et al. 2017).

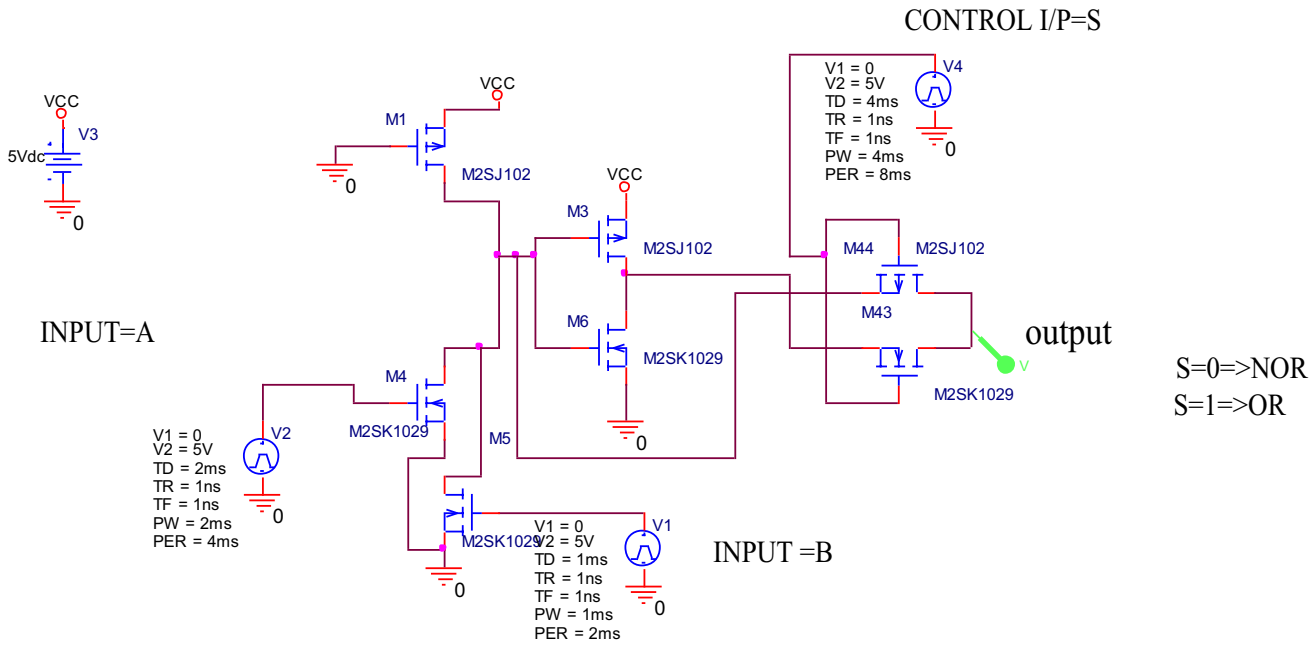

Fig. 12 NOR/OR gate using CMOS

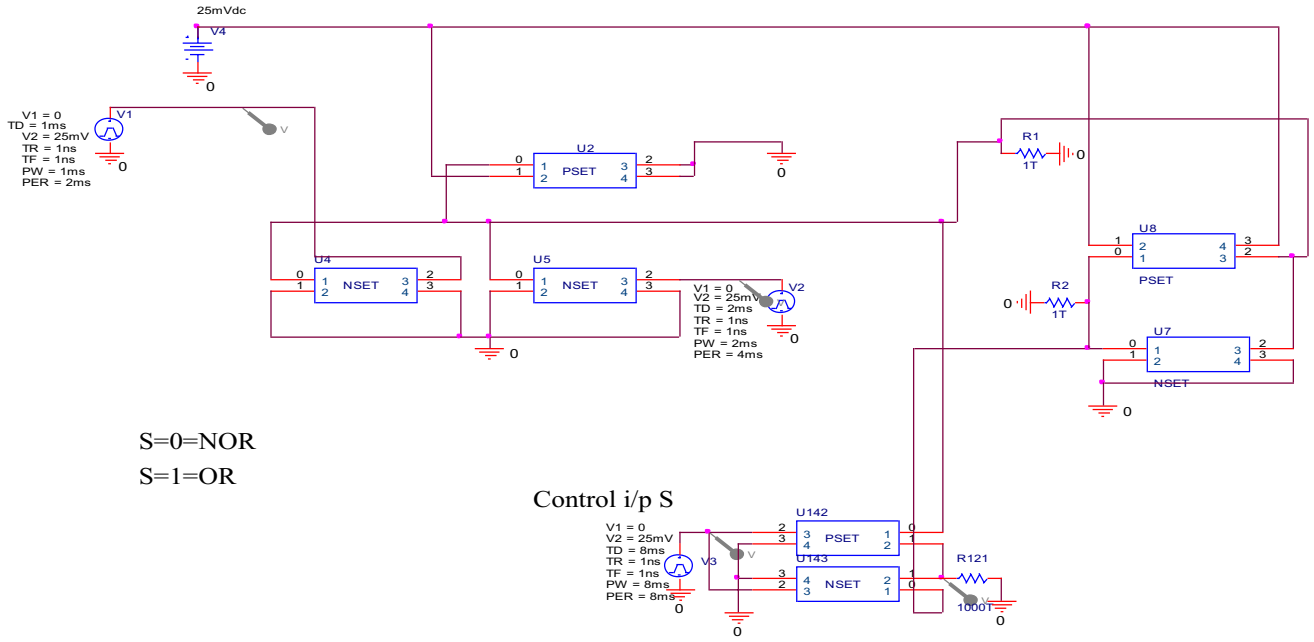

Fig. 13 NOR/OR gate using SET

3 Single electron transistor

A single electron transistor (SET) is considered as an essential feature of current research in the field of Nano technology. The single-electron charging energy of a nm scale island and consequent tunneling events to the island was analyzed by C.J. Gorter in 1950s. Gorter (1951) noticed that the granular thin film structure and the suppression of low voltage due to the charging of grains with single electron. The film is actively granular in nature, with a range of grain sizes are only ~ 7–10 nm. This Nano scale size is strong enough for significant charging effects of single electron. A thin oxide layer is then sputtered on top of the granular metal film, and certainly a metal contact is deposited on top to develop a layer

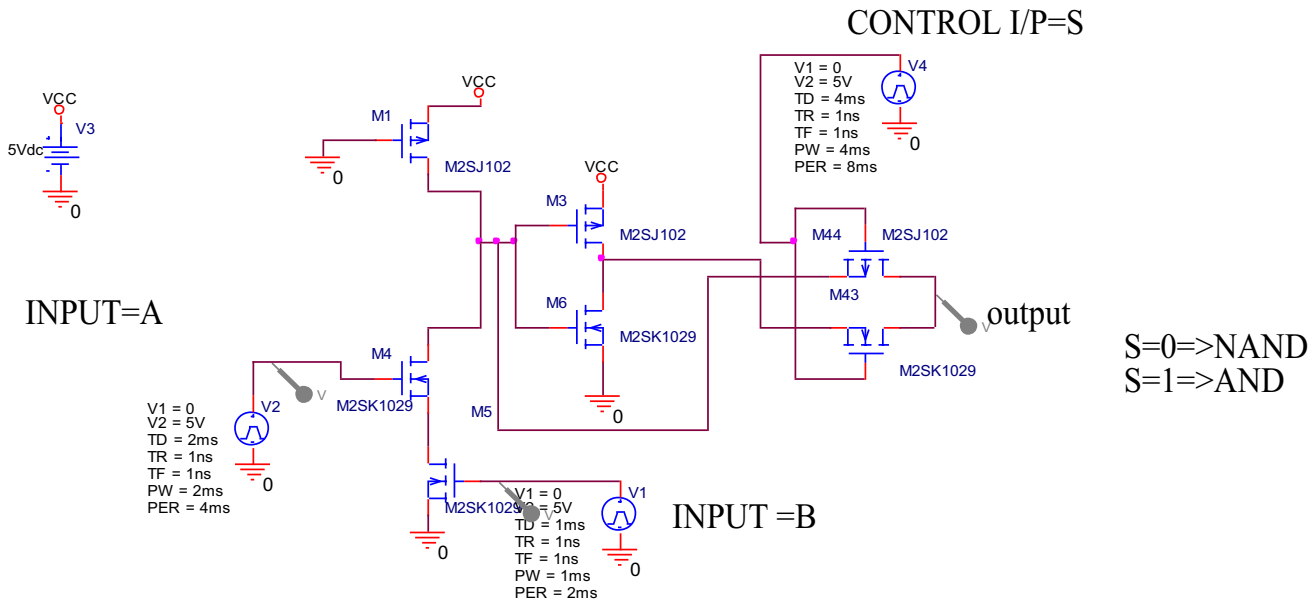

Fig. 14 NAND/AND gate using CMOS

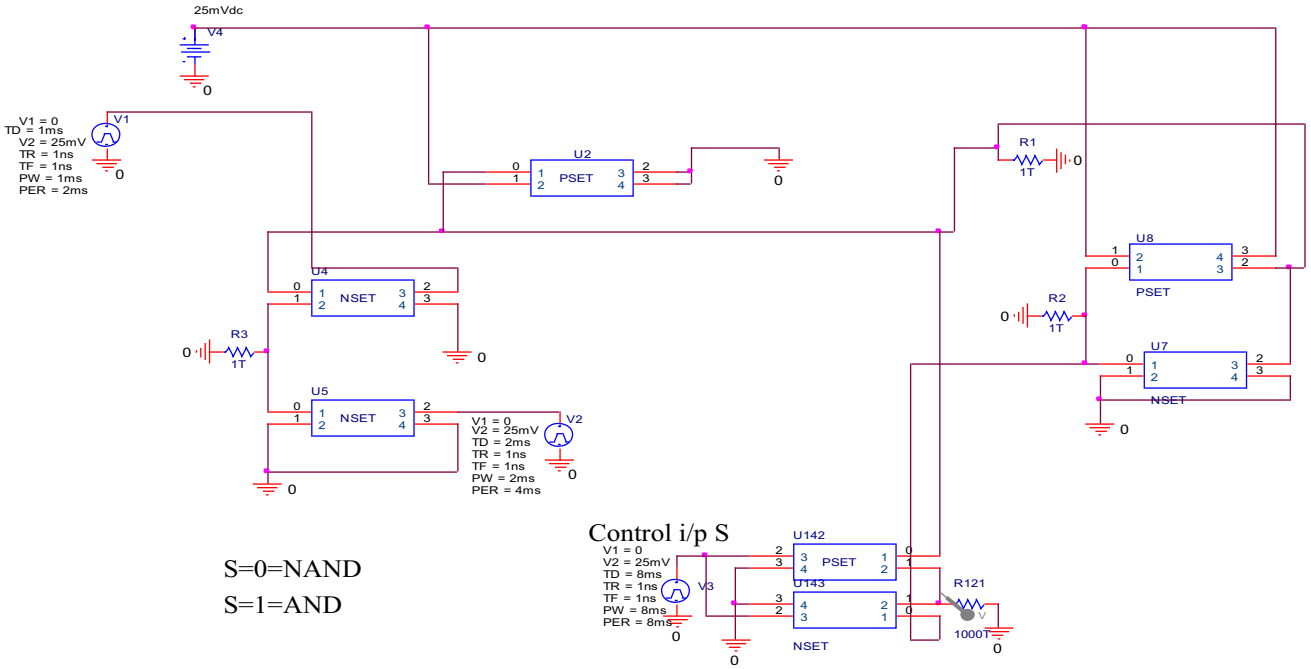

Fig. 15 NAND/AND gate using SET

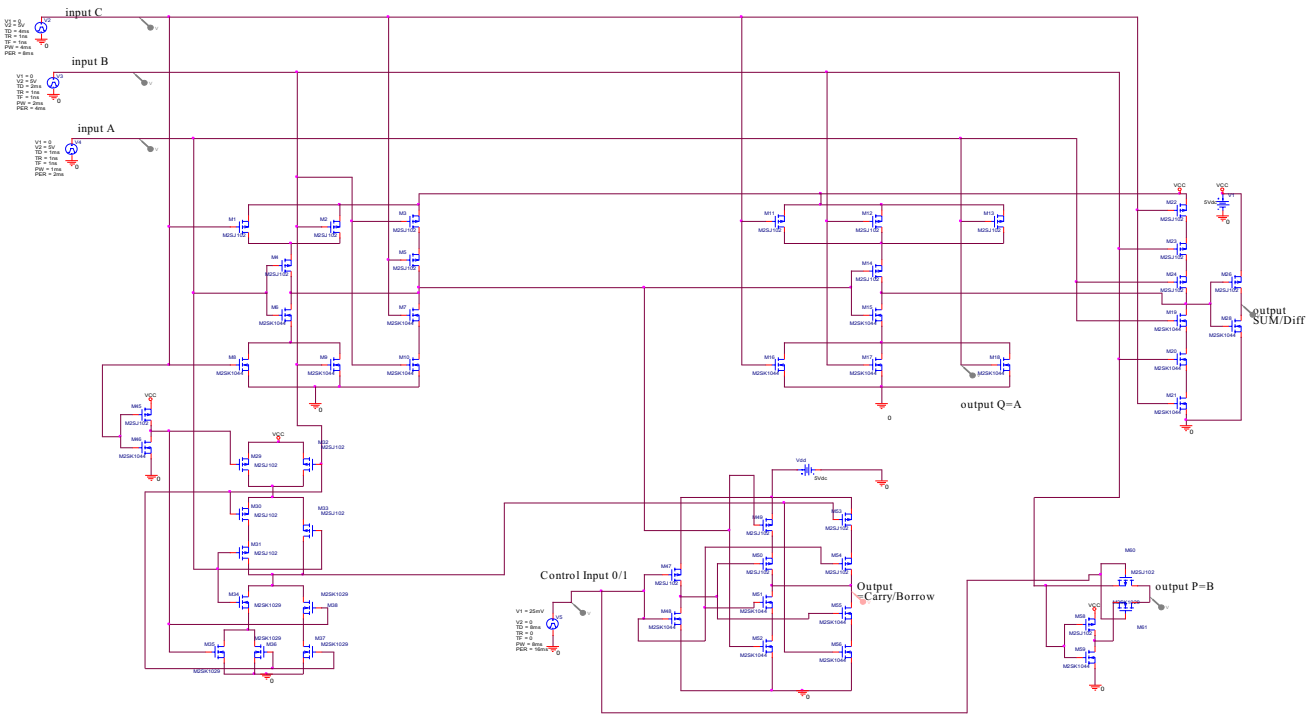

Fig. 16 1-bit full adder using CMOS

of metal nano particles. The thin oxide layers develop tunnel barriers for transfer of electrons. Addition of a third terminal called 'gate', the island of the two tunnel junctions forms SET by Fulton and Dolan (1987). SETs are devices in which the charge transport occurs discrete in nature unlike MOS devices.

It comprises of two electrodes namely, the drain and the source, connected through tunnel junctions to one common electrode with a low self-capacitance, known as the island. The third electrode called gate, is capacitively coupled to the island shown in Fig. 2. This gate electrode can tune the electrical potential of the island.

The single electron tunneling concept can be detailed by considering a tiny metallic sphere. In Fig. 3, consider a small sphere which is electro-neutral. Also seeing that an electron is located near to the sphere and it gets attracted and linked with a sphere which in turn leaving a negative charge on the sphere. Due to that charge, a strong electric field is produced around the sphere. If any other electron comes near to this sphere, it will feel a strong repulsive force exerted by the electric field created around the sphere. This coulomb blockade energy is the repelling energy of preceding electron remain in the island to the next electron coming towards the island.

This coulomb charging energy is the key reason for the suppression of electron transfer across the junction simultaneously. This occurrence is known as "Coulomb blockade" as shown in Fig. 4. In order entering and leaving of electrons from one to another junction is commonly called as "correlated tunneling of electrons". Since it has the ability to control the tunneling of single electrons across its junction, it performs at high speed. Since power consumption is proportional to number of transferred electrons across the junction, it consumes less power. Since electron tunneling

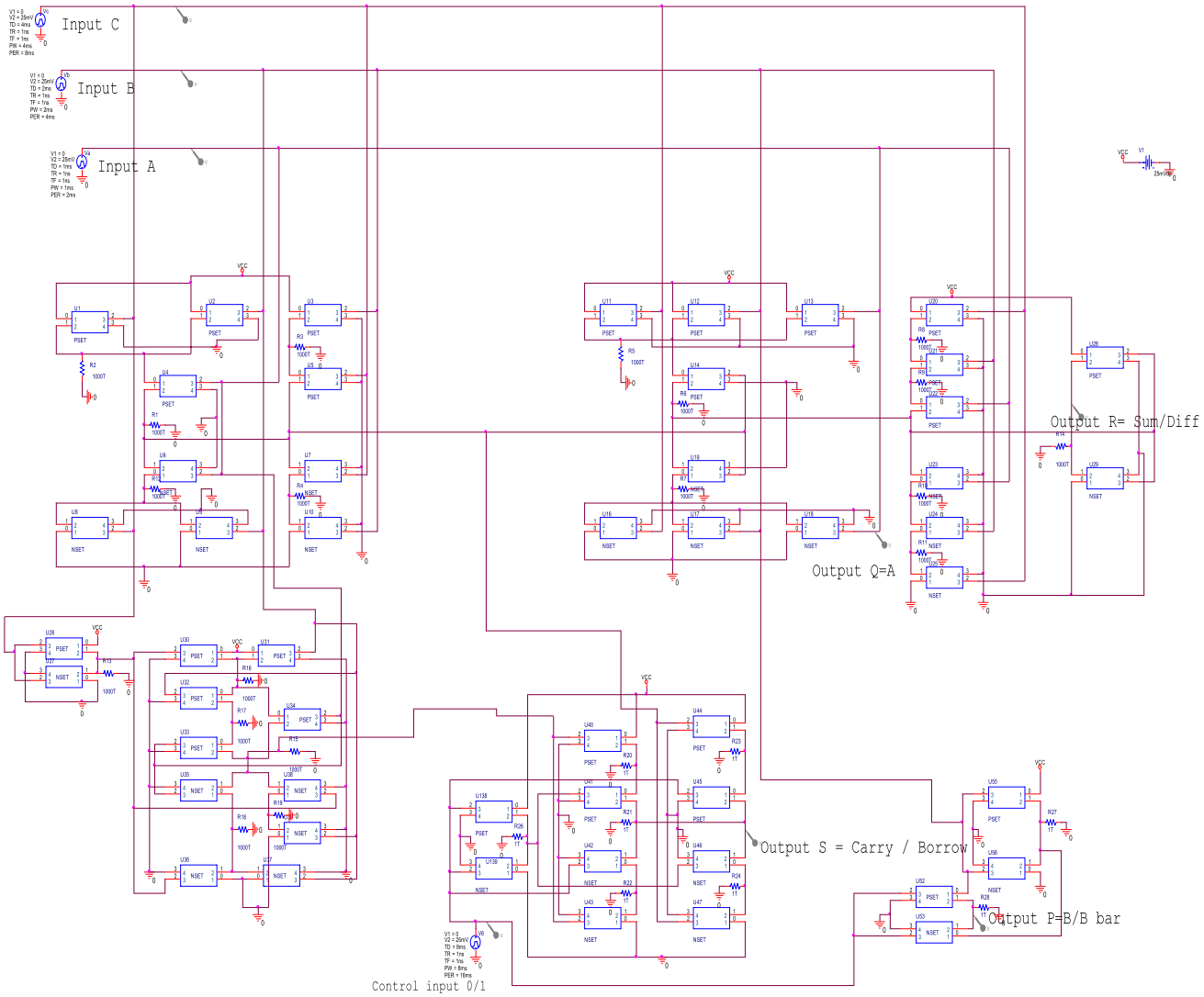

Fig. 17 1-bit full adder using SET

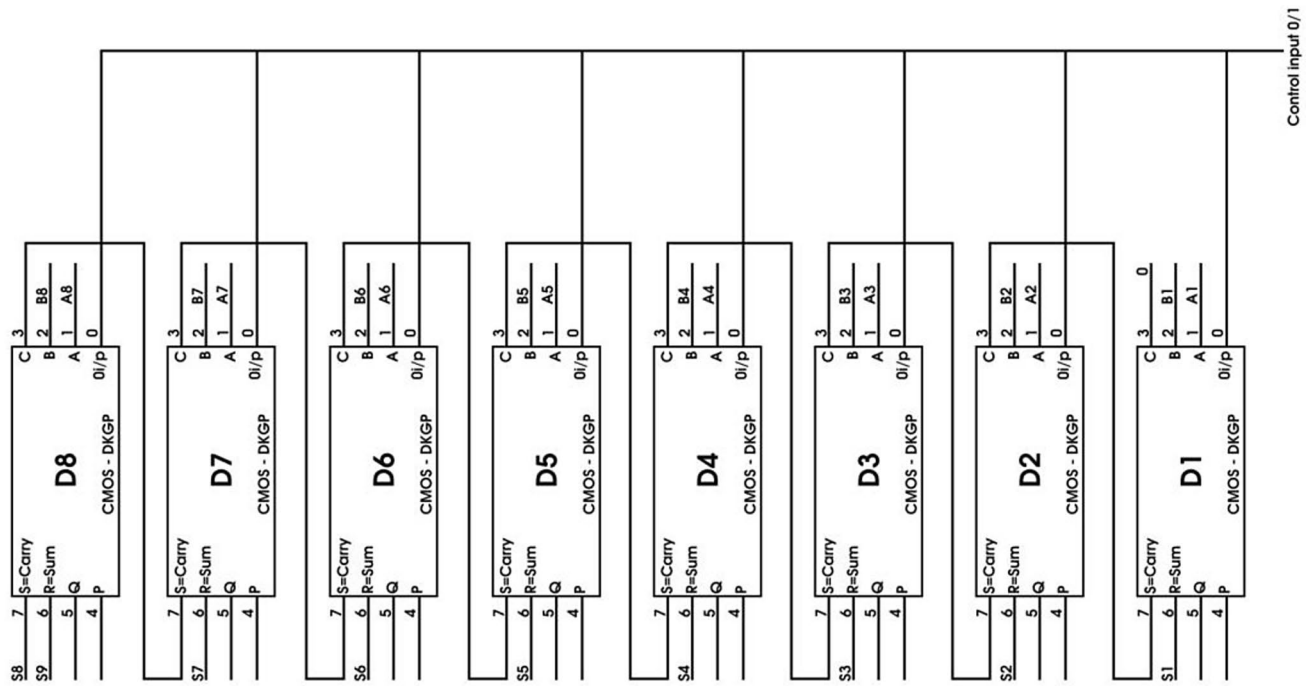

Fig. 18 Block diagram for 8-bit adder/subtractor using CMOS

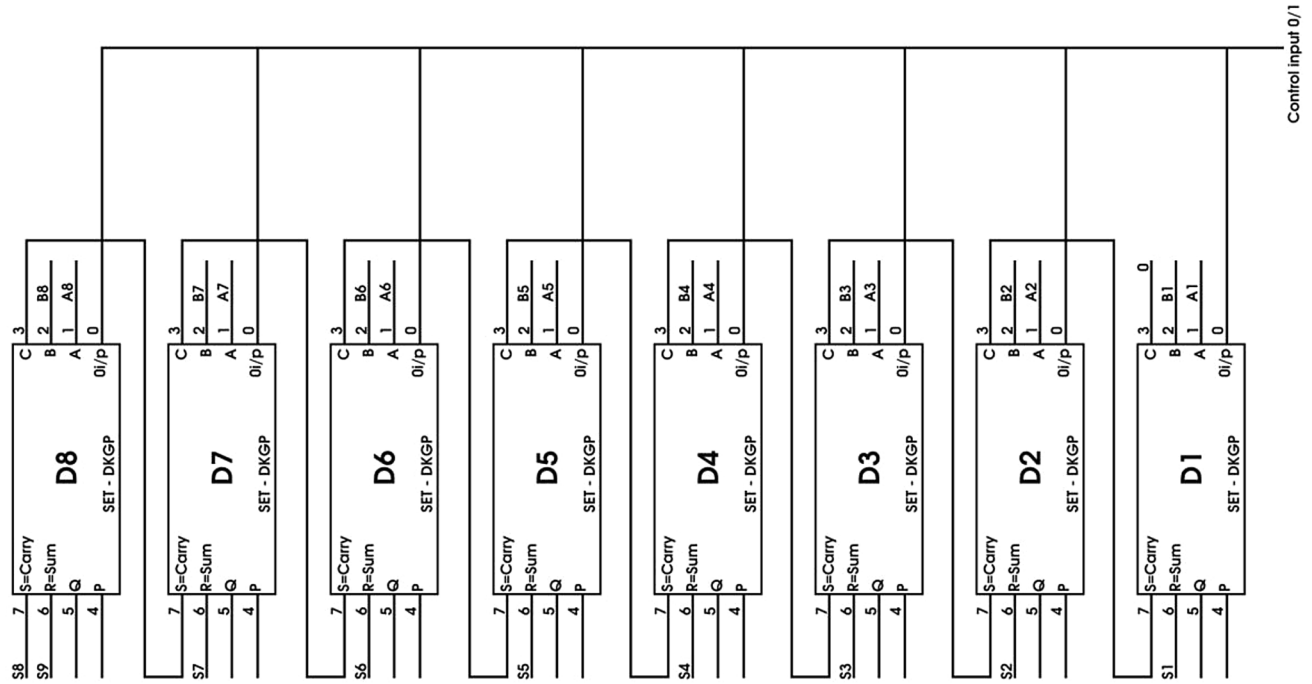

Fig. 19 Block diagram for 8-bit Adder/Subtractor using SET

Table 2 Number of gates used for complementing adder block

S.no	Existing works and Proposed	No.of reversible gates	No. of garbage outputs
1	Existing (Bommi 2016)	16FG + 16FTFA = 32	80
2	Existing (Sahu et al. 2017)	16peres + 6toffoli + 2fredkin gates = 24	24
3	Existing (Gouthami and Sathyanarayana 2016)	16 peres gate = 16	16
4	Existing (Sarada and Muralidhar 2016)	16 RACSG = 16	32
5	Adder in this work	8 DKGP = 8	16

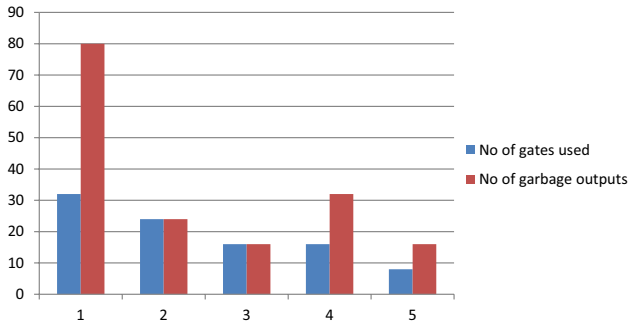

Fig. 20 Comparison of adders with number of gates

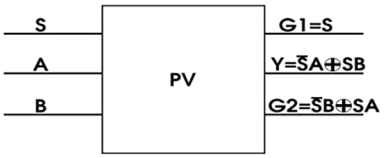

Fig. 21 PV gate

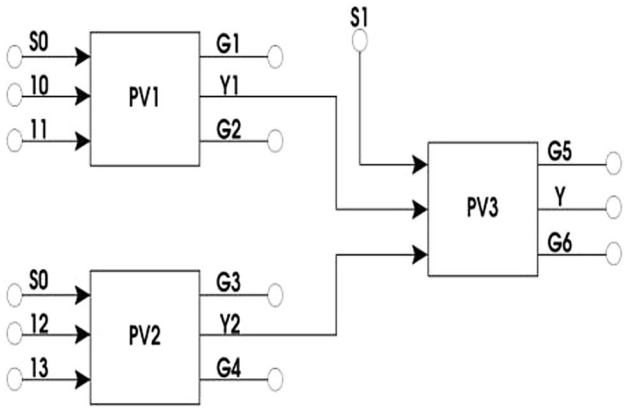

Fig. 22 4:1 Mux using PV gate

is a discrete process, the electric charge flows through the tunnel junction in multiples of e. Now if the bias voltage V is kept below the Coulomb gap voltage and if the gate voltage is increased, the energy of the initial system (with no electrons on the island) gradually increases, while energy of the system with one excess electron on the island gradually decreases. The periodic oscillation in the Coulomb gap is observed in the IDS-VDS characteristics by changing the gate voltage as shown in Figs. 5 and 6. The SET behaves as a easy switch, because it is influenced by the gate voltage. The SET will turn 'on' when Coulomb blockade does not exist and the SET will turn 'off' when a Coulomb blockade exists. Since SET is a Nano-scaled switching device, it can hang on to its scalability even on an atomic scale. Single electron device is commonly depend on an intrinsically quantum phenomenon known as the Tunnel effect (Singh et al. 2012).The molecular single-electron transistor (SET) with (10-Boranylanthracene-9-yl) borane molecule as an island has been analyzed in an attempt to model a better acene series SET. The analysis proved that the doped anthracene-based SET has high switching speed and power efficiency related with the other organic molecular SETs reported of the kind.(Boddepalli SanthiBhushan et al. 2016). SET is a promising candidate for attaining higher detection sensitivity due to its coulomb oscillations and thus it can be possibly used as one of the sensors among many in the ultra-sensitive detection of ions and biomolecules in the field of healthcare and life sciences (Malasinghe et al. 2017). SET can also be significantly employed in the detection of infrared images in object recognition especially in infrared animal recognition in the forest (Mangai et al. 2018).

4 DKGP reversible gate

A 4* 4 reversible DKGP gate is one among many of the reversible gates available and it can function as both reversible full adder and full subtractor. It is shown in Fig. 7. It can be verified with the input pattern corresponding to a

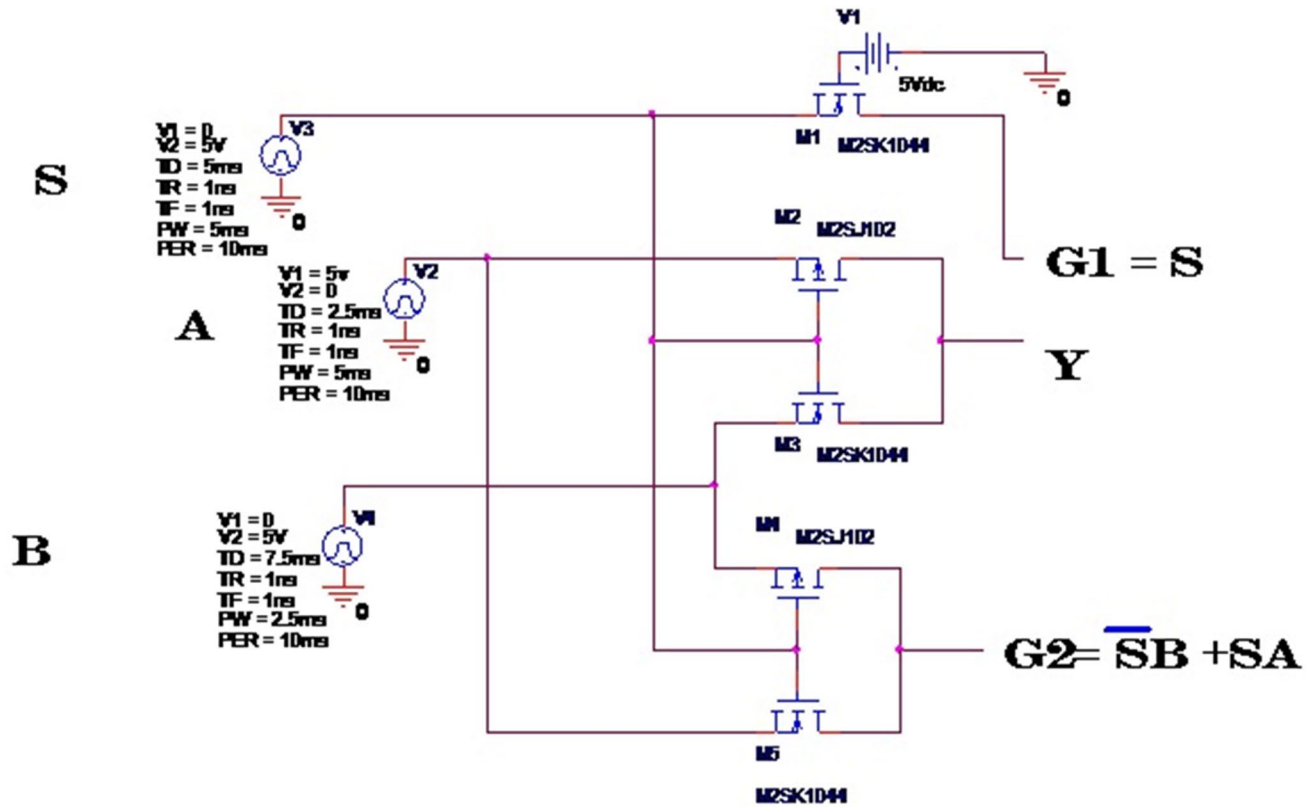

Fig. 23 2:1 Mux using CMOS

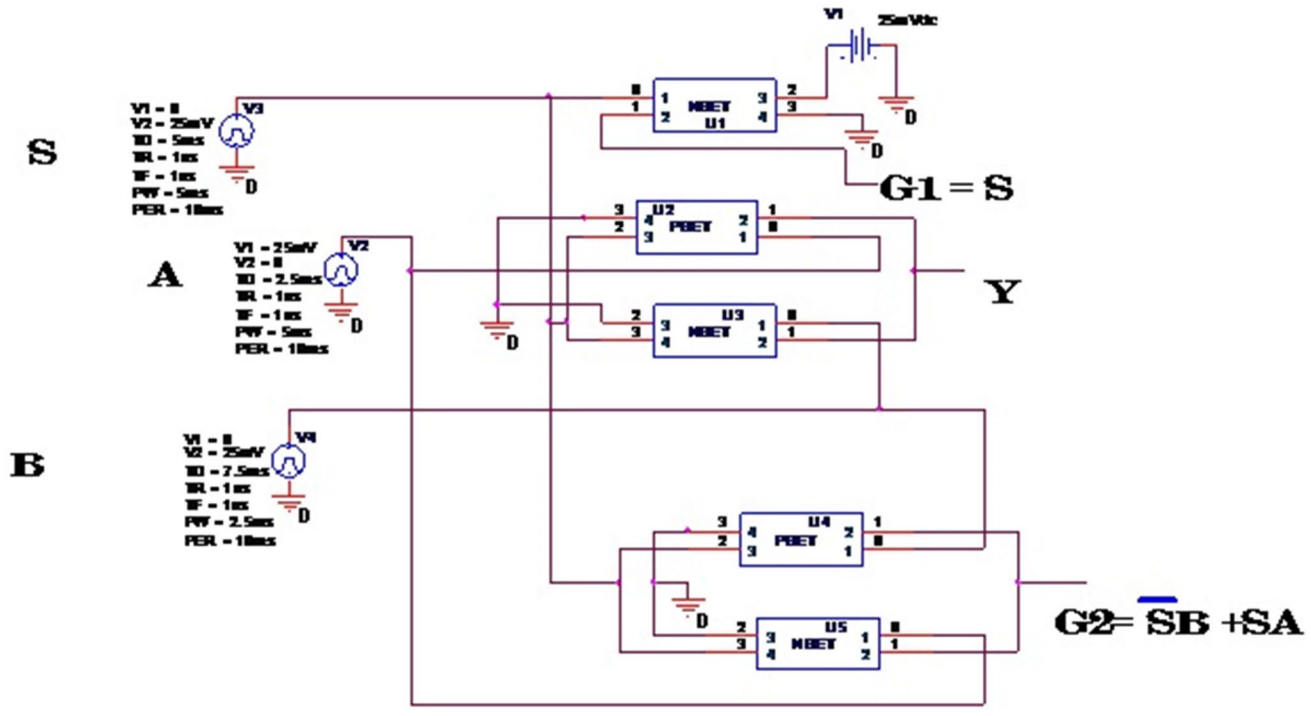

Fig. 24 2:1 Mux using SET

Table 3 Truth table for 4:1 mux

Selected inputs		Output
S1	S0	Y
0	0	I0
0	1	I1
0	0	I2
1	1	I3

respective output pattern which can be uniquely determined. The logical implementation of both full adder and full subtractor from DKGP gate is shown in Figs. 8 and 9 respectively. If the input P = 0, the gate behaves as a reversible Full adder and if the input P = 1, the gate behaves as a reversible full Subtractor (Krishnaveni.D et al. 2012).

The 4:2 and 6:2 compressors can be constructed from DKGP full adder and it is shown below in the Figs. 10 and 11 (see Table 1).

Using this reversible gate, all the components of the ALU are developed initially and then it is implemented using CMOS and SET.

5 Reversible 8-bit ALU using single electron transistor

The 8-bit ALU is constructed from NOR/OR gate and NAND/AND gate for logical operations and complementing adder and multiplier for arithmetic operations. All the blocks are implemented using CMOS and SET.

5.1 NOR/OR gate

The gate acts as NOR gate if the control input is zero and acts as OR gate if the control input is one. The transistor implementation of NOR/OR gate using CMOS and SET is shown in the Figs. 12 and 13.

5.2 NAND/AND Gate

The gate acts as NAND gate if the control input is zero and acts as AND gate if the control input is one. The transistor implementation of NAND/AND gate using CMOS and SET is shown in the Figs. 14 and 15.

5.3 DKGP gate as a 1-bit full adder

The one bit full adder using DKGP gate has been developed by giving the first input of DKGP gate is zero. The transistor implementation of one bit full adder using CMOS and SET is shown in the Figs. 16 and 17.

5.4 8-bit Reversible Adder/Subtractor

The complementing adder block acts as both 8-bit adder and 8-bit subtractor depending on the control input. If the control input is 0, this block acts as 8 bit adder and if it is 1 then it acts as 8 bit subtractor. This complementing adder is constructed from series of DKGP full adders which is shown in Figs. 18 and 19.

The number of gates has been minimized to develop 8 bit complementing adder block using DKGP gate. The comparison for existing and proposed 8 bit adder with number of gates and garbage outputs is shown in Table 2 and a comparison graph is shown in Fig. 20.

5.5 4:1 Multiplexer

The reversible multiplexer is designed using reversible PV gate is shown in the Figs. 21 and 22. It can work as 2:1 multiplexer. The 4:1 multipl exer can be obtained from three PV gates. The 4:1 mux can be developed by calling the 2:1 mux in program coding(using syntax .subckt). Thus the transistor implementation of 2:1 mux using CMOS and SET is shown below in the Figs. 23 and 24 (see Table 3).

5.6 8 × 8 Reversible multiplier

The 8-bit multiplier is constructed from 4:2 and 6:2 compressors in order to reduce the partial product addition. There are 22 full adders, eight 4:2 compressors and five 6:2 compressors are employed to develop reversible multiplier. The serial and parallel combination of these compressors are involved in generating the multiplication output. The block diagram for 8-bit Wallace tree multiplier using compressors are shown in Figs. 25 and 26.

The number of gates has been minimized to develop reversible multiplier using DKGP gate. The comparison for existing and proposed 8 bit multiplier with number of gates and garbage outputs is shown in Table 4 and a comparison graph is shown in Fig. 27.

6 Results and disscussions

The reversible 8-bit ALU is designed with minimum number of gates and implemented with both CMOS and SET technology. The design is simulated using ORCAD tool. The outputs are verified for CMOS-ALU with the operating voltage of 5V. The output glitches are obtained with the operating voltage of less than 2 V. The same output responses with no glitches are obtained for SET-ALU with the operating voltage of 25 mV. The SET technology gives exact output and dissipates ultra low power. The functions

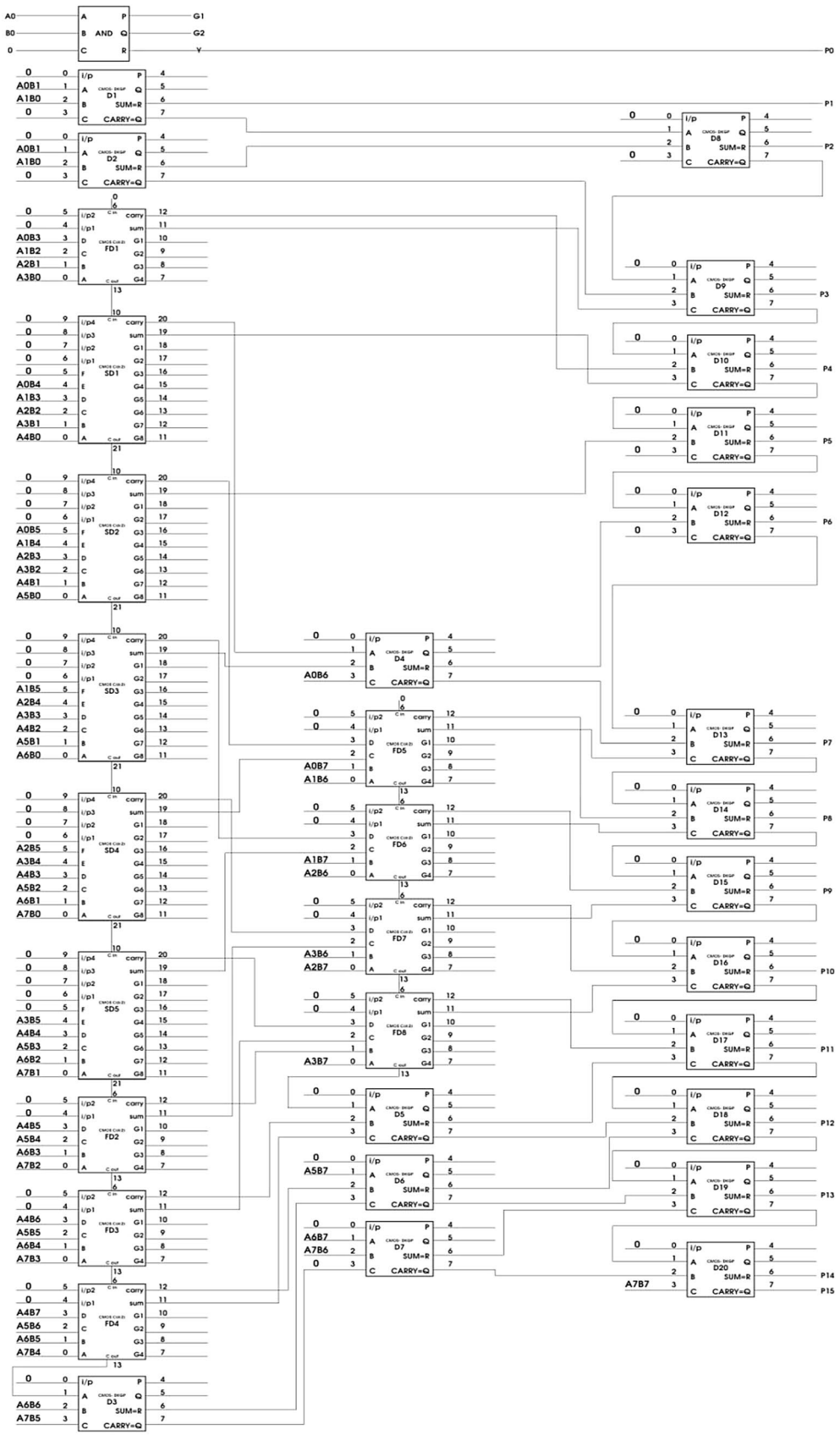

Fig. 25 8×8 reversible multiplier using CMOS

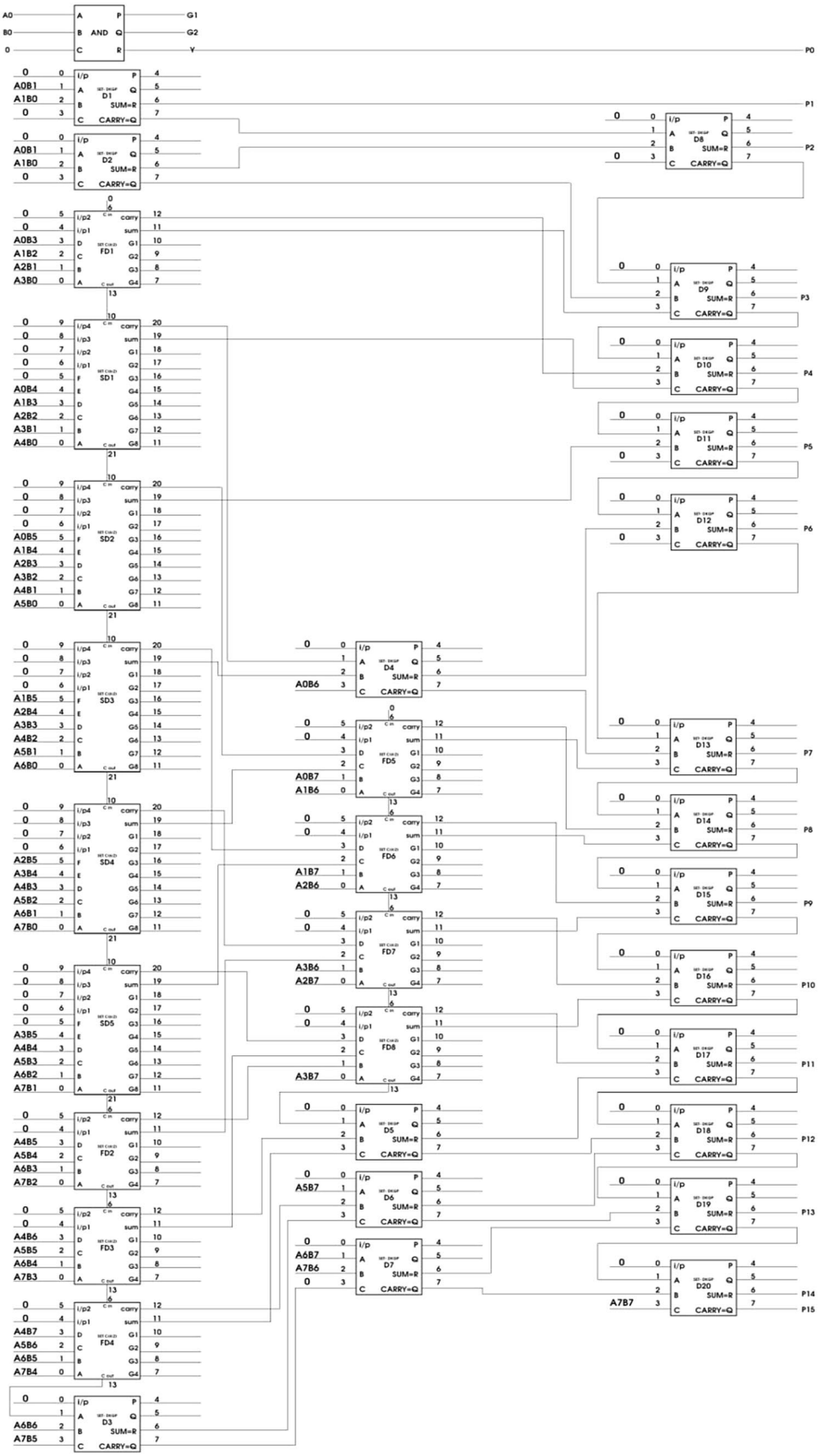

Fig. 26 8×8 reversible multiplier using SET

Table 4 Number of gates used for reversible multiplier

S.No	Existing and proposed work	No.of reversible gates	No. of garbage outputs
1	Existing (Gowthami and Satyanarayana 2018)	97	102
2	Existing (AnanthaLakshmi and Sudha 2013)	69	159
3	Existing (Thapliyal and Srinivas 2006)	61	122
4	Existing (Nekkanti Gowthami and Srilakshmi 2017)	59	114
5	Proposed	57	112

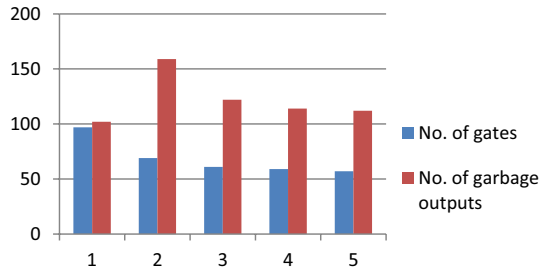

Fig. 27 Comparison of multiplier with number of gates and garbage outputs

of ALU to the control inputs are given in the Table 5. The model parameters of CMOS and SET is given in Table 6. The simulation results of reversible ALU using SET is shown below in the Figs. 28, 29, 30 and 31.

The power dissipation of various components involved in ALU using CMOS and SET is shown in the Tables 7 and 8.

Table 5 Functions of ALU

Control inputs			Input		Output	Function
S1	S2	S0	A0–A7	B0–B7	O0–O7	
0	0	0	11101101	00001110	00010000	NOR
0	0	1	10100100	00010101	11111011	NAND
1	0	0	01101010	01110001	00100111	ADDITION
1	0	1	10010100	11000000	11011110	MULTIPLICATION
0	1	0	01100110	10010101	11110111	OR
0	1	1	00110011	10110011	00110011	AND
1	1	0	00011101	00011100	00000001	SUBTRACTION

Table 6 Values of Parameters used for the simulation

Device	Parameters	Voltage level
NSET	RTD = RTS = 100K, CTD = CTS = 1aF, CG = 1aF, Qo = 0.25(offset charge in units of e)	Logic0 = 0V, Logic1 = 25 mV VDD = 25 mV
PSET	RTD = RTS = 100K, CTD = CTS = 1aF, CG = 1aF, Qo = − 0.25(offset charge in units of e)	Logic0 = 0V, Logic1 = 25 mV VDD = 25 mV
NMOS	VTH = 3.2V, W/L = 3.8 µm/2 µm, Tox = 2 µm, Rs = 20 mΩ, Rds = 800 KΩ, Rd = 1413 Ω,Cgdo = 25.34 pf, Cgso = 336.9 pf	Logic0 = 0V, Logic1 = 5V VDD = 5V
PMOS	VTH = -0.846V, W/L = 0.55 µm/2 µm, Tox = 2 µm, Rs = 20 mΩ, Rds = 50 KΩ, Rd = 0,Cgdo = 684 pf, Cgso = 266 pf	Logic0 = 0V, Logic1 = 5V VDD = 5 V

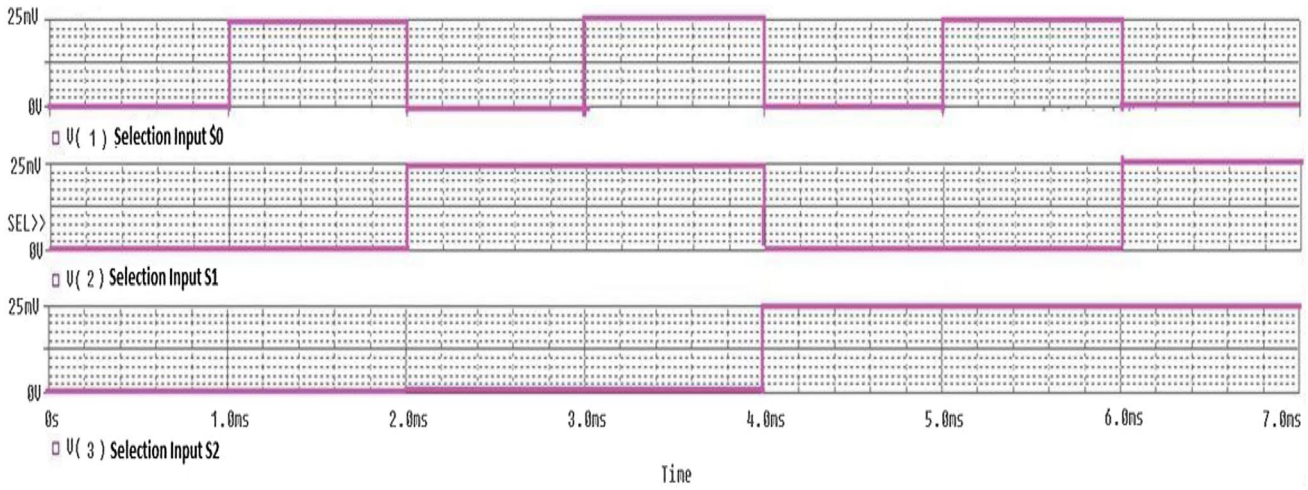

Fig. 28 Control inputs (S2 S1 S0)

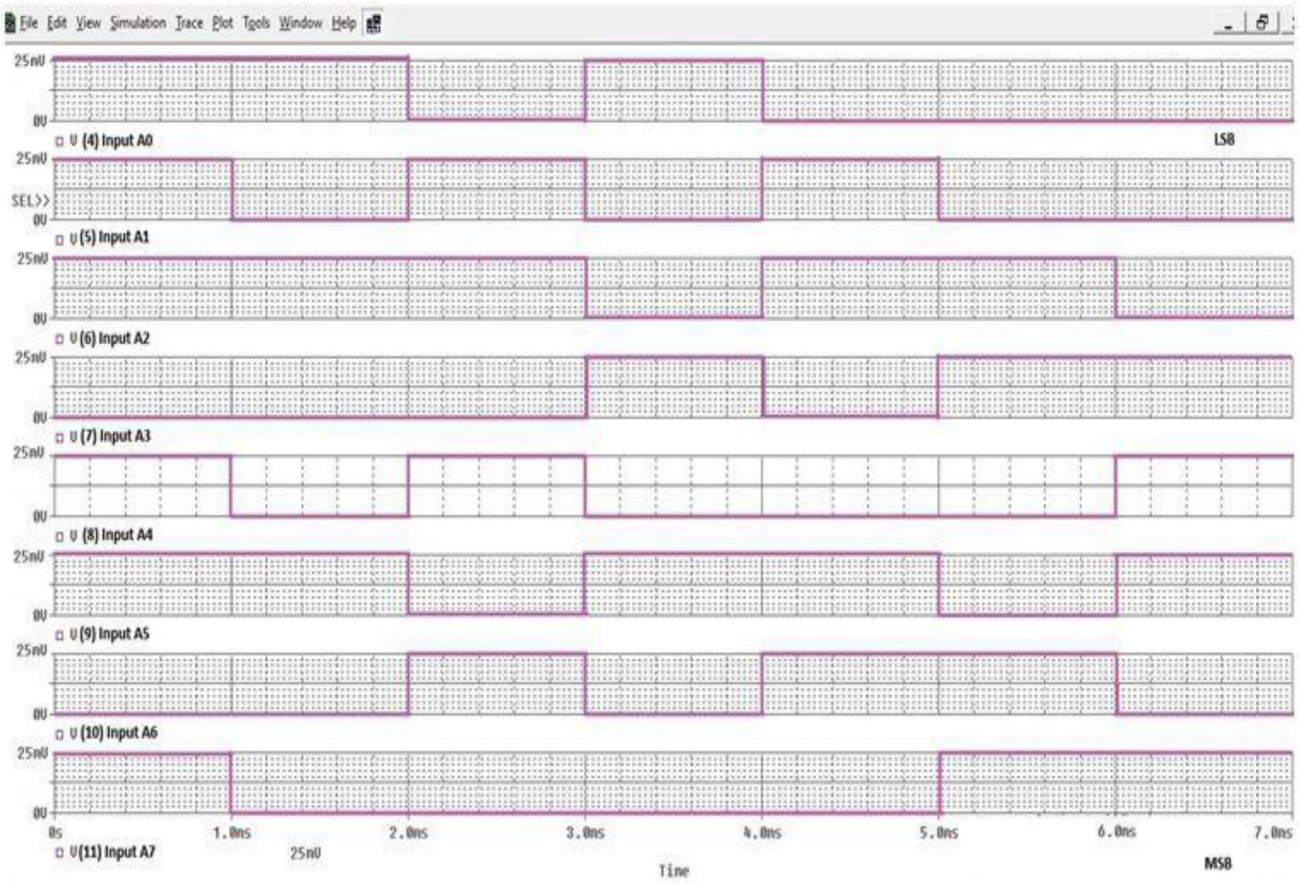

Fig. 29 Input A0–A7

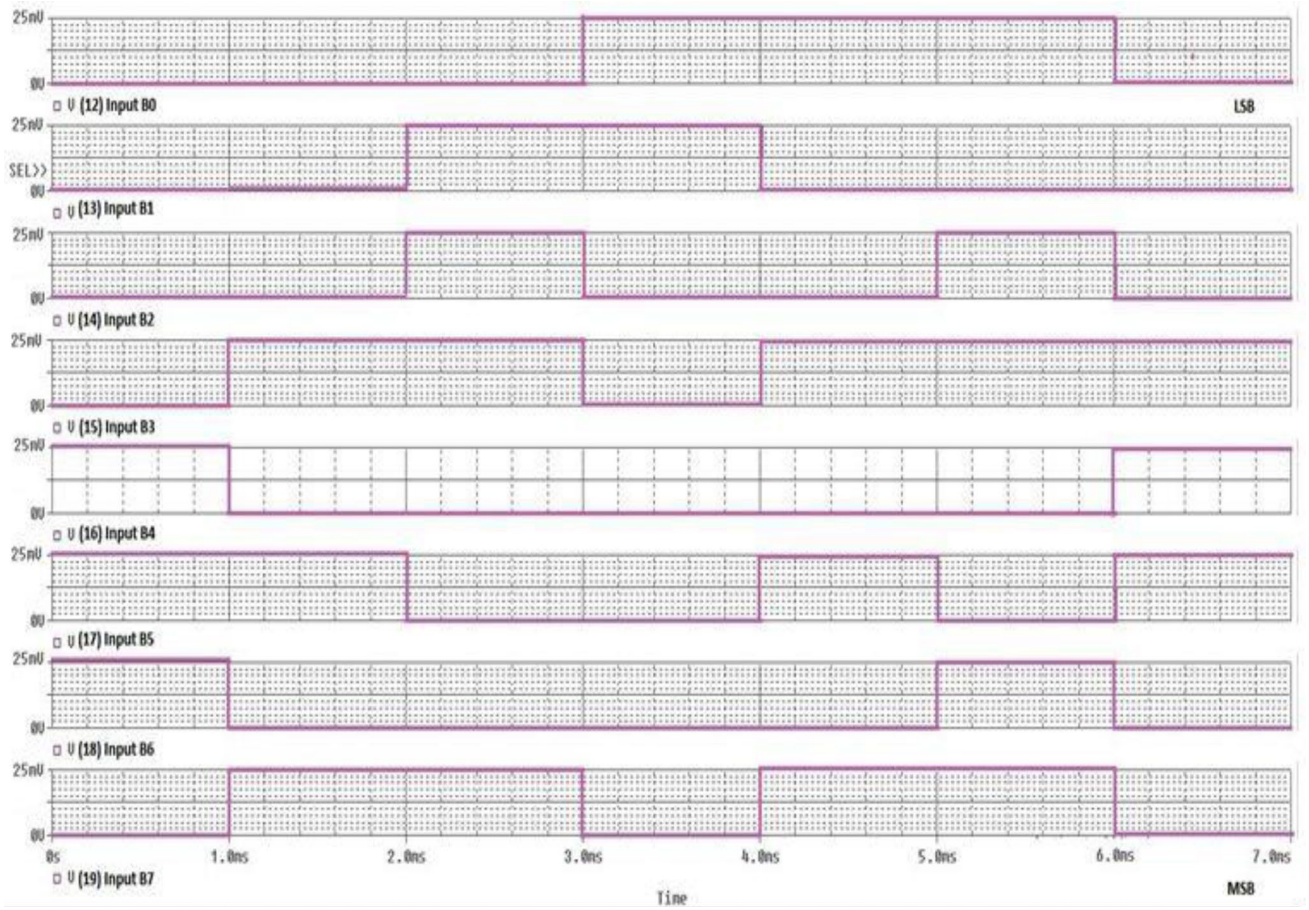

Fig. 30 Input B0–B7

7 Conclusion

The reversible 8-bit ALU is designed using CMOS and SET. The SET technology provides the same output response for the same input signal timing as in CMOS with very low operating voltage. Thus power consumption of SET technology varies drastically with CMOS. This work witnessed that the SET technology provides an alternative approach to conventional CMOS in low power digital applications. Therefore ALU using SET could be a potential towards the development of faster Nano processor with smaller size and low power consumption.. The practical implementation of SET can be done with adequate lithographic techniques and parameter dispersion considerations.

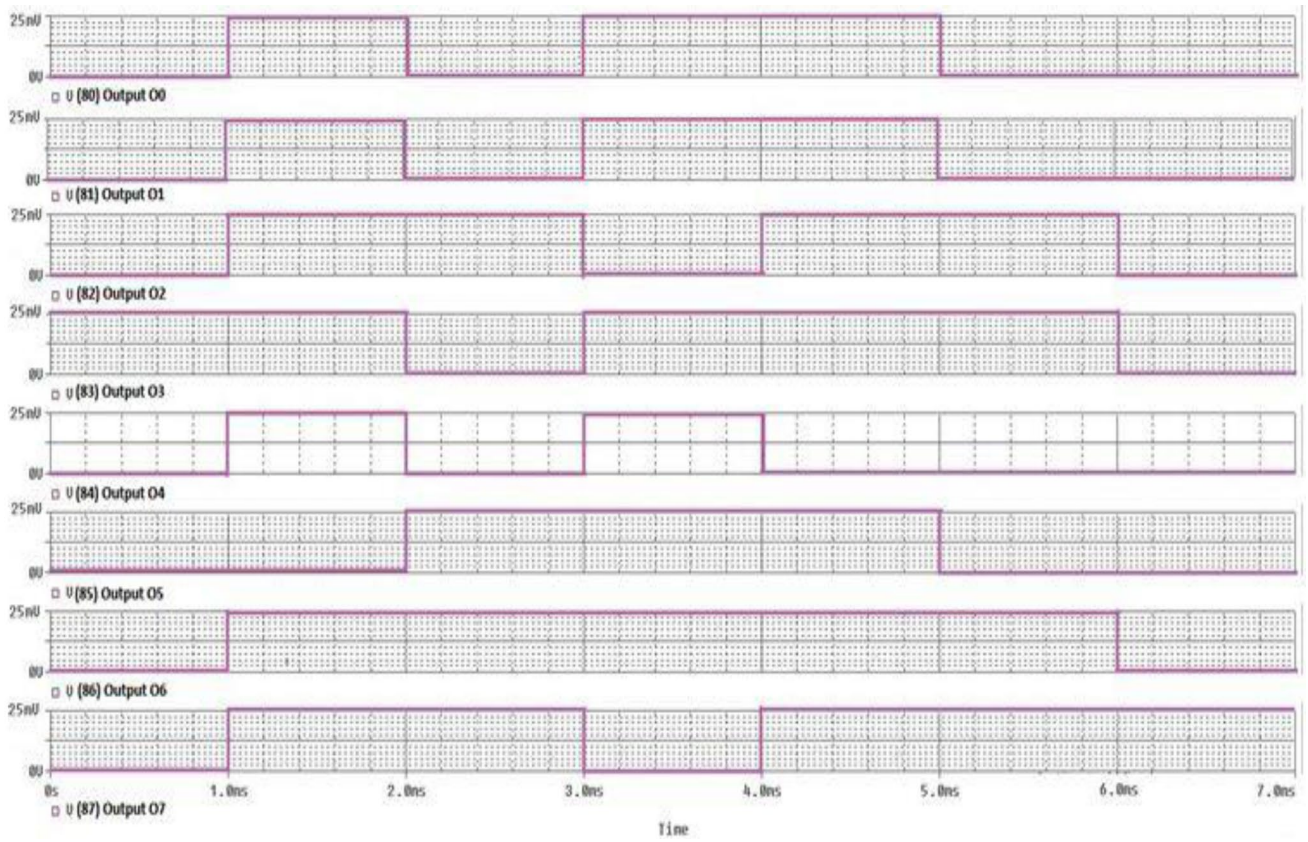

Fig. 31 Output(O0–-O7)

Table 7 Power dissipation, delay and PDF of components using CMOS

Component	Power dissipation for CMOS (mW)	Delay (ns)	PDP (10^{-12} J)
OR/NOR gate	0.65	2.45	1.5925
AND/NAND gate	0.575	2.16	1.242
1-bit full adder	1.431	5.39	7.7077
4:1 multiplexer	1.51	5.69	8.591
8-bit Add/Sub	8.03	30.3	243.305
8-bit multiplier	18.04	68.14	1229.245
Reversible 8-bit ALU	28.02	105.9	2967.318

Table 8 Power dissipation, delay and PDP of components using SET

Component	Power dissipation for SET (pW)	Delay (ps)	PDP (10^{-27} J)
OR/NOR Gate	0.00381	0.0165	0.6286
AND/NAND Gate	0.00258	0.0108	0.0278
1-bit full adder	0.00894	0.0442	0.395
4:1 multiplexer	0.0138	0.0802	1.106
8-bit Add/Sub	0.0826	0.0834	6.88
8-bit multiplier	0.61	0.315	192.15
Reversible 8-bit ALU	0.786	0.341	268.02

References

AnanthaLakshmi AV, Sudha GF (2013) An efficient implementation of a reversible single precision floating point multiplier using 4:3 compressor. In: Elsevier, Proc. of Int. Conf. on advances in information technology and mobile communication, pp 229–238

Bennett CH (1973) Logical reversibility of computation. IBM J Res Devel 17(6):525–532

Bommi RM (2016) Circuit design and CNTFET implementation of ultra adder. Austral J Basic Appl Sci 10(1):214–218

Deng G, Chen C (2013) Binary multiplication using hybrid MOS and multi-gate single-electron transistors. IEEE Trans Very Large Scale Integr (VLSI) Syst 21(9):1573–1582

Dhulipalla L, Deepak A (2011) Design and implementation Of 4-bit ALU using FINFETS for nano scaletechnology. In: IEEE international conference on nanoscience, engineering and technology, pp 190–195; https://doi.org/10.1109/ICONSET.2011.6167951

Dubuc C, Beaumont A, Beauvais J, Drouin D (2009) Current conduction models in the high temperature single-electron transistor. Solid-State Electron 53(5):478–482

Fulton TA, Dolan G (1987) Observation of single-electron charging effects in small tunnel junctions. Phys Rev Lett 59(1):109–112

Gangadhar Reddy and Ramireddy (2014) A novel power-aware and high performance full adder cell for ultra low power design. IEEE Int Conf Circuit Power aComput Technol. https://doi.org/10.1109/ICCPCT.2014.7055037

Gorter CJ (1951) A possible explanation of the increase of the electric resistance of thin metal films at low temperatures and small field strengths. Physics 17(8):777–780

Gouthami P, Sathyanarayana RVS (2016) Design of digital adder using Reversible logic. Int J Eng Res Appl 6(2):53–57

Gouthami P, Sathyanarayana RVS (2018) Performance evaluation of reversible vedic multiplier. ARPN J Eng Appl Sci 13(2):1002–1008

Gowthami N, Srilakshmi K (2017) Design and Implementation of Reversible Multiplier using optimum TG Full Adder. IOSR J Electron Commun Eng (IOSR-JECE) 12(3):81–89

Inokawa H, Takahashi Y (2003) A compact analytical model for asymmetric single-electron tunneling tran-sistors. IEEE Trans Electron Devices 50(2):455–461. https://doi.org/10.1109/TED.2002.808554

Jain A, Sarkar SK (2012) Design and Reliability Analysis of a 4:1 Mux Using Single Electron Tunneling Technology Based Threshold Logic Gate. J Electron Devices 15(1):1241–1248

Jana B, Jana A, Basak S, Sing JK, Sarkar SK (2013a) A comparative performance study of hybrid SET-CMOS based logic circuits for the estimation of robustness. J Nano Electron Phys 5(3):54–57

Jana A, Sing NB, Sing JK, Sarkar SK (2013b) Design and simulation of hybrid CMOS SET circuits. Microelectron Reliab 53(4):592–599

Jana B, Jana A, Basak S, Sing JK, Sarkar SK (2014) Design and performance analysis of reversible logic based ALU using hybrid single electron transistor. In: IEEE 2014 recent advances in engineering and computational sciences (RAECS) UIET, pp 1–5; https://doi.org/10.1109/RAECS.2014.6799652

Krishnaveni D, GeethaPriya M, Baskaran K (2012) Design of an efficient reversible 8 × 8 wallace tree multiplier. World Appl Sci J 20(8):1159–1165

Landauer R (1961) Irreversibility and Heat generation in the computing process. IBM J Res Devel 5(3):183–191

Li C-H, Shiau Y-H (2018) A time division multiplexing algorithm based on FPGA buffer shift to realize high speed image processing. J Ambient Intell Humaniz Comput. https://doi.org/10.1007/s12652-018-0991-0

Mahapatra S, Vaish V, Wasshuber C, Banerjee K, Ionescu AM (2004) Analytical modeling of single electron transistor for Hybrid CMOS-SET analog IC Design. IEEE Trans Electron Devices 51(11):1772–1782. https://doi.org/10.1109/TED.2004.837369

Mahima U, Chaitra A, Manasa R, Navya Holla K (2017) Implementation of full adder using single electron transistor, SET: the next generation nano device. Int J Sci Technol Eng 3(12):152–157

Malasinghe LP, Ramzan N, Dahal K (2017) Remote patient monitoring: a comprehensive study. J Ambient Intell Humaniz Comput. https://doi.org/10.1007/s12652-017-0598-x

Mangai NMS, Karthigaikumar P, Vinod ST, Chandy DA (2018) FPGA implementation of elephant recognition in infrared images to reduce the computational time. J Ambient Intell Humaniz Comput. https://doi.org/10.1007/s12652-018-0984-z

Parihar R, Tiwari N, Mandloi A, Kumar B (2014) An implementation of 1-bit low power full adder based on multiplexer and pass transistor logic. IEEE Int Conf Inf Commun Embedded Syst. pp. 101–103; https://doi.org/10.1109/ICICES.2014.7034071

Rani TE, Rani MA, Rao R (2011) Area optimized low power arithmetic and logic unit. IEEE Int Conf Electron Comput Technol. https://doi.org/10.1109/ICECTECH.2011.5941742

Ravindra JVR, Ramireddy GR, Kamatham H (2013) Design of ultra low power full adder using modified branch based logic style. In: IEEE European modelling symposium, pp 691–696. https://doi.org/10.1109/EMS.2013.116

Sahu I, Joshi PK, Narkhede NP, Admane SV (2017) Design of power efficient reversible carry skip adder. Int J Appl Eng Res 12(22):12772–12782

SanthiBhushan B, Khan MS, Khan MS, Srivastava A (2016)) First principle analysis of (10-Boranylanthracene-9-yl)borane-based molecular single-electron transistor for high-speed low-power electronics. IEEE Trans Electron Devices 63(3):1232–1238

Sarada M, Muralidhar M (2016) A novel design and implementation of reversible adder cum subtractor. Int J Innov Eng Technol 16:48–54 (**special issue on ETICE**)

Sharma A, Tiwari R (2016) Low Power 8-bit ALU design using full adder and multiplexer. IEEE WiSPNET, 2160–2164; https://doi.org/10.1109/WiSPNET.2016.7566525

Singh VP, Agrawal A, Singh SB (2012) Analytical discussion of single electron transistor(SET). Int J Soft Comput Eng (IJSCE) 2(3):502–507

Srivastava A, Srinivasan C (2002) ALU design using reconfigurable CMOS Logic. In: IEEE 45th midwest symposium on circuit and system, pp 663–666. https://doi.org/10.1109/MWSCAS.2002.1186949

Thapliyal H, Srinivas MB (2006) Novel reversible TSG gate and its application for designing components of primitive reversible quantum ALU. Int Conf Inf Commun Signal Process. https://doi.org/10.1109/ICICS.2005.1689293

Tiwari R, Deshmukh K (2014) Design and analysis of low power 11-transistor full adder. IJAREEIE 3(6):10301–10307

Touati A, Chatbouri A, Sghaier N, Kalboussi A (2012) New model for drain and gate current of single-electron transistor at high temperature. WJNSE l(2):171–175

Uchida K, Matsuzawa K, Koga J, Ohba R, Takagi S, Toriumi A (2000) Analytical single-electron transistor (SET) model for design and analysis of realistic SET circuits. Jpn J Appl Phys 39(4B):2321–2324. https://doi.org/10.1143/JJAP.39.2321

Vaishnav P, Moyal V (2012) Performance analysis Of 8-bit ALU for power in 32 N m Scale. IJERT 1(8):1–3

Willy F, Darma Y (2016) Modeling and simulation of single electron transistor with master equation approach. J Phys Conf Ser 739:1–7. https://doi.org/10.1088/1742-6596/739/1/012048