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RESEARCH

Effect of Amorphous Si-Zn-Sn-O Passivation Layer on Si-In-Zn-O Thin Film Transistors

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Abstract
Bi-layer thin film transistors (TFTs) have been fabricated with improved field effect mobility and stability. These TFTs feature a unique channel structure comprising a dielectric layer, an amorphous-Si-In-Zn-O (a-SIZO) layer, and an amorphous-Si-Zn-Sn-O (a-SZTO) layer. Total resistance of the channel and contact resistance between the electrode and channel were determined using transmission line method (TLM). Precisely deposited thin films via RF sputtering at room temperature, our TFTs, equipped with a bottom gate top contact and processed at 500 °C, exhibited outstanding characteristics. They showcased high mobilities exceeding 30 $cm^2V^{-1}s^{-1}$, a current on/off ratio of approximately 10^9, and a subthreshold swing (SS) value below 0.45 V $decade^{-1}$. Furthermore, these bi-layer TFTs demonstrated stability under negative and positive bias stress, indicating their potential for reliable performance across a range of applications and promising advancements in TFT technology.

Keywords Amorphous oxide semiconductor · Field effect mobility · Negative and positive bias stress · Thin film transistor · Bi-layer-TFT

1 Introduction

Amorphous oxide semiconductors (AOSs) represent a class of materials extensively investigated for their potential as channel materials in thin-film transistors (TFTs) due to their exceptional properties, including high mobility, uniformity over large areas, cost-effectiveness, and stability [1, 2]. AOSs find primary application in next-generation flat panel displays such as liquid-crystal displays (LCDs) and organic light-emitting diode (OLED) displays. However, challenges persist in AOSs concerning bias-induced stability and mobility [3–6].

To address these challenges, numerous studies have been conducted to enhance AOS TFT mobility and stability through methods such as oxygen plasma treatment, annealing, high-pressure plasma annealing, bilayer fabrication, and channel passivation [7–14]. Among the various proposed methods, the bilayer structure has been extensively investigated for its ability to achieve both high mobility and bias stability. This approach involves integrating two distinct amorphous semiconducting thin film channel layers. To safeguard the unstable active under-layer, a chemically durable material can be employed as the active top layer. In addition to the bilayer approach, multiple reports have emerged on multilayer structure TFTs demonstrating significantly improved performance and stability [15–19]. However, it's important to note that most AOS TFTs still exhibit low mobility and significant instability under bias stress. Ensuring stability under both negative and positive bias is crucial for their integration into active-matrix liquid crystal displays (AMLCDs) and active-matrix organic light-emitting diode (AMOLED) devices.

In this paper, we have studied the improvement of device performance and stability in 1SIZO TFT with the incorporation of SZTO as an active top layer. We have varied the Si concentration from 0 to 2 wt% in the top passivation layer a-SZTO and studied its effect on the overall performance of the TFT. Additionally, we employ the transmission line method

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(TLM) to demonstrate that Ti/Al forms an ohmic contact with the bilayer channel. Furthermore, we examine the effects of positive and negative bias stress on bilayer TFTs.

2 Experimental

Bottom gate bilayer TFTs were fabricated using RF magnetron sputtering at ambient temperature. The device configuration is illustrated in Fig. 1. The bilayer architecture was composed of 0, 1, and 2 wt % Si-Zn-Sn-O (SZTO) and 1 wt % Si-In-Zn-O (1SIZO). Depositions were performed on 100 nm SiO_2/p^{++}-Si substrates, with SiO_2 acting as the gate insulator. Prior to deposition, the SiO_2/p^{++}-Si substrates underwent a series of cleaning steps including ultrasonication in acetone, methanol, and DI water for 10 minutes each, followed by drying with N_2 gas.

The base pressure of the deposition chamber prior to each deposition cycle was approximately $(5 \pm 1) \times 10^{-6}$ T. For the top SZTO channel,deposition parameters including power, pressure, and Ar flow rate were held constant at 50 W, 6 mT, and 40 sccm, respectively. Conversely, for the 1SIZO channel, these parameters were adjusted to 60 W, 12 mT, and 40 sccm, respectively. The thickness of the SZTO and 1SIZO layers remained consistent at (7.5 ± 0.5) nm and (4.5 ± 0.5) nm, respectively.

After deposition of ZTO/1SIZO, 1SZTO/1SIZO, and 2SZTO/1SIZO, the bilayer thin films were subject to wet etching process to form channel with width and length of 250 μm and 50 μm, respectively. Subsequently, channels were annealed in air at 500 °C for 2 hours. The source and drain electrodes (S/D) were deposited using e-beam evaporation (10 nm Ti) and thermal evaporation (40 nm Al), followed by a lift-off process. The fabrication procedure for TLM devices closely resembled that of TFT devices. TLM devices were fabricated with a constant width (W) of 250 μm and various lengths (L) ranging from 10 μm to 300 μm.

The electrical properties and stability analysis were conducted within a black box utilizing a semiconductor parameter analyzer (HP 4156C, 33220s, Agilent) and a vacuum probe station (Hewlett-Packard Co. HP 4145B, Keysight), respectively.

3 Results and Discussion

Figure 2 depicts the transfer curve of an a-SIZO TFT with Ti/Al electrodes. The figure illustrates a substantial gate leakage current in the 1SIZO TFT, accompanied by a significant shift in threshold voltage towards extremely negative values. This deviation in threshold voltage can be attributed to the high carrier concentration of the a-SIZO semiconductor. The instability observed in SIZO devices may be associated with the absorption of oxygen from the atmosphere. The absorbed oxygen molecules form In-O bonds, leading to the creation of traps within the semiconductor material. These traps ultimately degrade the overall performance of 1SIZO TFTs [20–22]. Consequently, there is a need to fabricate 1SIZO TFTs with a passivation layer to mitigate these issues and improve device stability and performance.

To fabricate a bilayer TFT using 1SIZO and SZTO, it is imperative to establish a reliable ohmic contact with low contact resistance. The selected ohmic contact should adhere well to the channel, possess a smooth surface, and exhibit lower metal sheet resistance. Various methods exist for measuring ohmic contacts in metal/semiconductor interfaces, but the TLM is the most commonly employed technique. We utilized TLM to measure the contact resistance and sheet resistance of the channel. The total resistance can be calculated using the slope of the linear region of the output

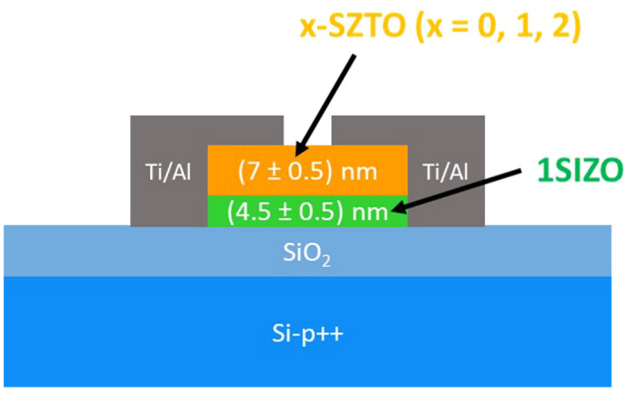

Fig. 1 Cross-sectional schematic of the bi-layer structure of the TFT devices showing the bottom SIZO layer with a thickness of (4.5 ± 0.5) nm and the top SZTO layer maintained at a constant thickness of (7.5 ± 0.5) nm. The total thickness of the bilayer TFT devices is (12 ± 1) nm

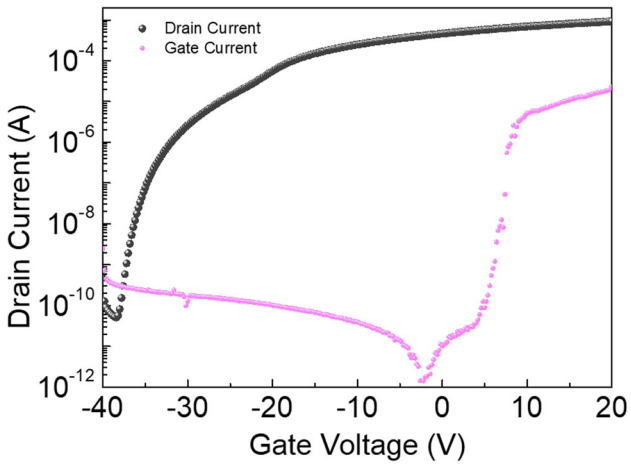

Fig. 2 Transfer characteristics of 1SIZO TFTs with Ti/Al as source and drain. Width and length of TFT was 250 and 50 μm respectively

characteristic with the following equation [23, 24]:

$$R_{\text{tot}} = 2R_c + \frac{R_{\text{sh}}}{W} \cdot L_{\text{ch}} \tag{1}$$

Here, L_{ch} represents the electrode separation, and W denotes the fixed channel width of 250 μm. R_c represents the contact resistance, while R_{sh} signifies the sheet resistance of the semiconducting layer.

Figure 3(a) and (b) illustrate the total resistance of ZTO/1SIZO and 1SZTO/1SIZO bilayer channels, respectively, with varying channel lengths. Ti/Al of 10/40 nm have been used as electrode on channel for TLM measurement. The gate voltage has been adjusted to obtain the total resistance at different gate voltages. As the channel length increases, the total resistance exhibits a linear increase, indicating ohmic behavior. Moreover, increasing the gate voltage results in a reduction of the total resistance. Figure 3(c) and (d) indicate that the sheet resistance and contact resistance reduces with increasing gate voltage.

Figure 4(a) displays the combined transfer curve of three bilayer devices: ZTO/1SIZO, 1SZTO/1SIZO, and 2SZTO/1SIZO. These devices exhibit very low gate leakage current, indicating the formation of a highly stable interface. The field-effect mobility (μ_{FE}) in these bilayer devices was determined at $V_{DS} = 5.1$ V using the equation [25]:

$$\mu_{FE} = \frac{Lg_m}{WV_{ds}C_{ox}} \tag{2}$$

Here, g_m represents transconductance, C_{ox} is the capacitance of the oxide gate electrode, and L and W are the channel length and width, respectively.

Both ZTO/1SIZO and 1SZTO/1SIZO devices exhibit excellent transfer curves with a subthreshold swing (SS) value of less than 0.45 V-decade^{-1}, an on/off current ratio (I_{ON}/I_{OFF}) of 10^9, and a field-effect mobility exceeding 30 cm^{2}V^{-1}s^{-1}. However, the device with 2 wt% Si TFT displays a poor transfer curve, resulting in degraded on/off ratio and SS value. Table 1 presents a overview of all extracted device parameters. Our previous research has revealed that the Fermi level of 1SIZO lies significantly closer to the conduction band minimum (CBM) compared to SZTO, as illustrated in Fig. 4 [26, 27]. The band alignment of 1SIZO and SZTO under positive gate bias delineates the direction of charge flow in the bilayer TFT. Specifically, under positive gate voltage, carriers readily traverse from the conduction band of SZTO to 1SIZO due to the downward bending of the CBM, facilitated by the higher carrier concentration in 1SIZO compared to SZTO. Furthermore, besides aiding in carrier transport, SZTO also serves as a passivation/capping layer for 1SIZO.

In all TFT parameters, the SS value is a primary indicator of the total trap density (N_t), which consists of bulk trap density (N_{bulk}) and interface trap density (D_{it}). The total trap density (N_t) was calculated using the equation [25]:

$$N_t = \left[\frac{SS \cdot \log(e)}{kT/q} - 1\right]\frac{C_{ox}}{q} \tag{3}$$

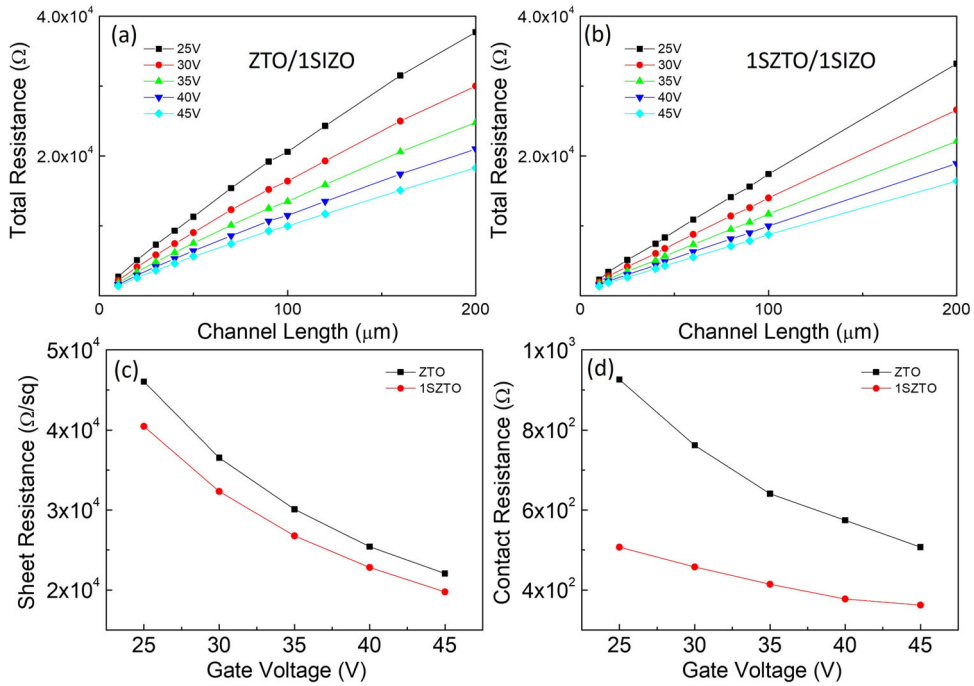

Fig. 3 Total resistance from TLM with varying channel thickness and gate voltage of (a) ZTO/1SIZO bilayer, and (b) 1SZTO/1SIZO bilayer. Extracted (c) sheet resistance and (d) contact resistance

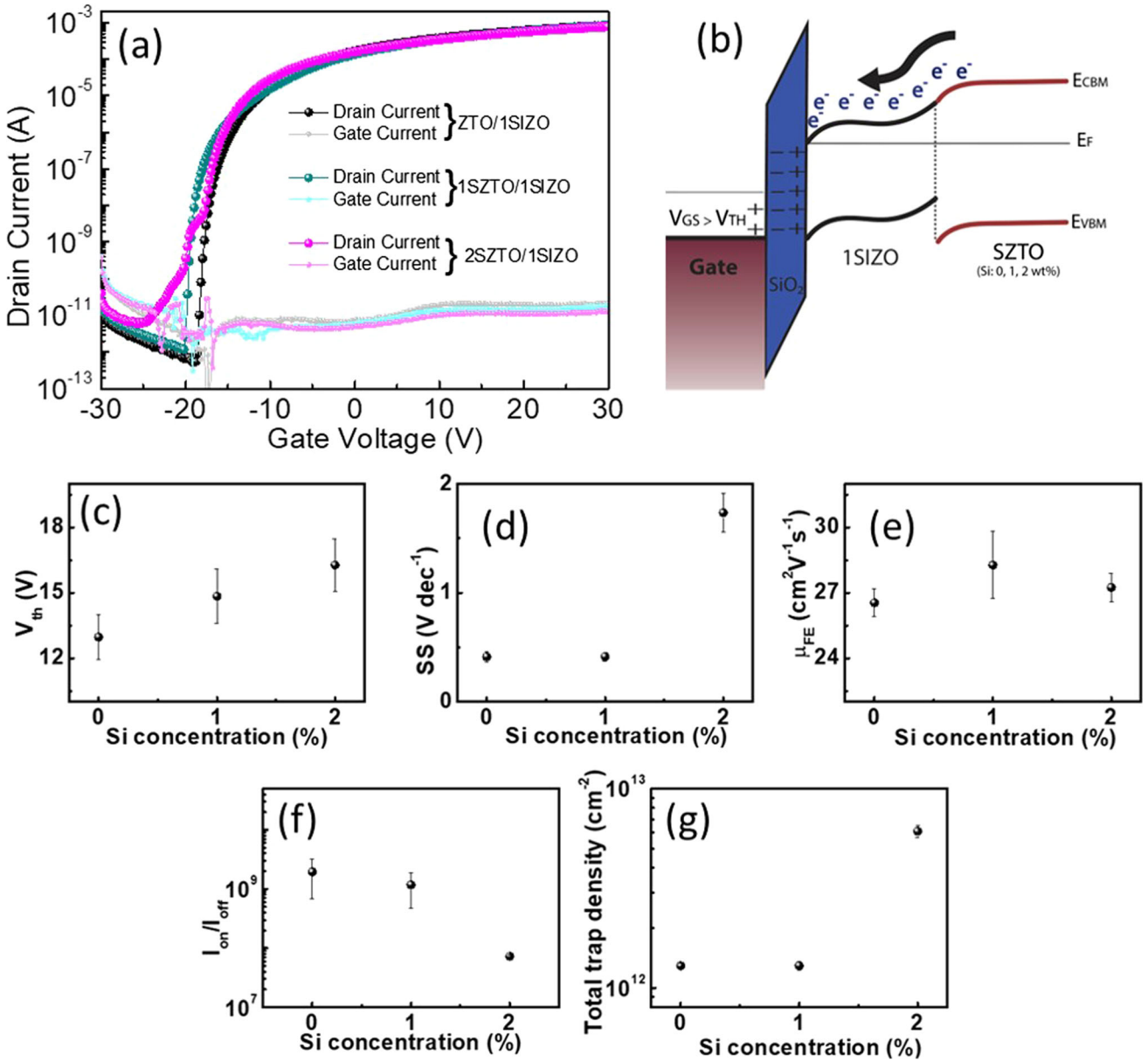

Fig. 4 a) Transfer characteristics of ZTO/1SIZO, 1SZTO/1SIZO, and 2SZTO/1SIZO bi-layer TFTs. (b). SIZO-SZTO band structure schematic. Extracted parameters of bilayer TFTs with respect to change in Si concentration of top layer (SZTO) (c). threshold voltage, (d). SS value, (e). field effect mobility, (f). on/off ratio, and (g). total trap density

Table 1 Extracted device parameters of bi-layered amorphous Si-Zn-Sn-O/Si-In-Zn-O thin film transistors TFTs

Si conc. (wt%) in SZTO	μ_{FE} ($cm^2V^{-1}s^{-1}$)	V_{th}(V)	I_{ON}/I_{OFF}	SS (V decade^{-1})	N_t ($\times 10^{12}$ cm^{-2})
0	26.55 ± 0.65	-12.97 ± 1.02	$\approx 10^9$	0.41 ± 0.05	1.29 ± 0.04
1	28.50 ± 1.55	-14.84 ± 1.25	$\approx 10^9$	0.41 ± 0.04	1.29 ± 0.03
2	27.25 ± 0.65	-16.27 ± 1.20	$\approx 10^7$	1.73 ± 0.18	6.11 ± 0.43

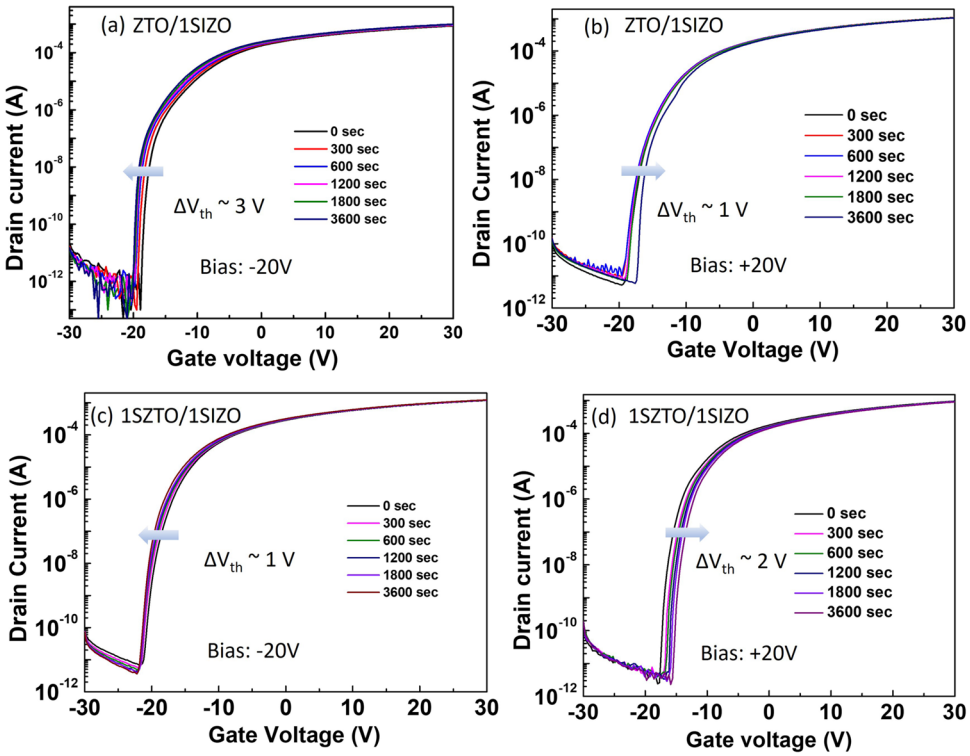

Fig. 5 Stability test of bilayer TFTs: (a) negative bias stress test of ZTO/1SIZO, (b) positive bias stress test of ZTO/1SIZO, (c) negative bias stress test of 1SZTO/1SIZO, and (d) positive bias stress test of 1SZTO/1SIZO

Here, SS represents the subthreshold swing, kT is the thermal energy, q is the electronic charge, and C_{ox} is the dielectric capacitance of the oxide gate electrode.

The calculated total trap density for ZTO/1SIZO and 1SZTO/1SIZO TFTs is approximately 1.29×10^{12} cm^{-2}, whereas for the device with 2 wt% Si TFT, it increases to as high as 6.11×10^{12} cm^{-2}. Moreover, previous studies on amorphous oxide semiconductor TFTs have identified instability in these devices as potentially arising from charge injection into the gate insulator, the generation of defect states in the bulk or at the interface, and/or the absorption of O_2 from the ambient environment into the channel surface [28, 29]. The incorporation of SZTO contributes to the formation of an exceptional interface and minimizes the absorption of ambient oxygen into the surface, thereby resulting in enhanced performance of bilayer TFTs.

To gain further insights into the gate bias stability of these bilayer devices, positive and negative gate bias stresses were applied to the 1SZTO/1SIZO and ZTO/1SIZO devices. Figure 5(a) and (c) depict the plots of log $I_{DS} - V_{GS}$ under negative gate bias stress at V_{GS} of -20 V, and Fig. 5(b) and (d) show the plots under positive gate bias stress at +20 V for the ZTO/1SIZO and 1SZTO/1SIZO devices, respectively.

In both bilayer devices, under positive bias stress, the I_{DS}–V_{GS} curve shifts positively by $\approx$ 1 to 2 V, while under negative bias stress, it shifts negatively $\approx$ 1 to 3 V, with no definite change in the SS value. The absence of SS variation may indicate carrier trapping in the bulk region and/or in deep traps of the channel and/or in the channel insulator interface, with almost no creation of defect states [30]. During positive bias, the change in threshold voltage towards the positive direction can be explained by the trapping of carriers in the defect states. These trapped carriers screen the applied gate-to-source voltage, resulting in a decreased V_{GS} [31, 32].

4 Conclusions

In summary, we have developed a high-quality bilayer structure using RF sputtering, incorporating amorphous SZTO and SIZO materials. The a-SZTO layer serves as the top layer in the channel and acts as a passivation layer. The concentration of Si in the SZTO layer has been varied from 0 to 2 wt%. The bilayer with 1 wt% Si exhibits improved mobility of approximately 30 cm^{2}V^{-1}s^{-1} with an SS value below 0.45 V-decade^{-1}. However, further increases in Si concentration in the top layer severely degrade device performance, with an SS value exceeding 1.7 V-decade^{-1}, indicating the formation of a poor interface between 1SIZO and 2SZTO, leading to the formation of numerous trap states at the interface. Positive and negative bias stress tests revealed that the devices are quite stable, with no formation of additional trap sites at the

interface. The TLM showed that Ti/Al forms an ohmic contact with the channel. Our study suggests that further research is needed to understand the bias stress mechanism in these bilayer devices before their application in AM-display panels.

Author Contributions S.K.M. and S.Y.L. designed the study. S.K.M. performed the experiments, analysed the data, and wrote the main manuscript text. All authors reviewed the manuscript. All authors read and approved the final manuscript.

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Data Availability No datasets were generated or analysed during the current study.

Declarations

Conflicts of Interest There is no conflict of interest among the authors while submitting the manuscript.

Competing of Interest The authors declare no competing interests.

Consent for Publication Yes.

Informed Consent All authors have been informed before submitting the manuscript.

Authorship All authors have read the Nature Portfolio journal policies on author responsibilities and submit this manuscript in accordance with those policies.

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