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RESEARCH

Investigation of Analog/RF behaviour of Asymmetrical Gate Tunnel FET at Cryogenic temperatures

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Abstract
This paper extensively sheds light on the performance of an Asymmetrical-gate Tunnel FET (A-TFET) under cryogenic temperatures (< 78 K) in terms of DC, Analog, and RF metrics. SILVACO ATLAS TCAD is implemented to invoke the device physics and subsequently characterize the lattice temperature parameters for facilitating the carrier transport in terms of device transfer characteristics, I_{ON}/I_{OFF} ratio, subthreshold swing (SS). Steep profiles for I_{ON}/I_{OFF} ratio and SS are observed at cryogenic temperatures representing superior device performance. Furthermore, the transconductance (g_m) and transconductance generation factor (TGF) profiles are thoroughly investigated as a part of analog analysis while RF metrics like the transistor parasitic capacitances and cut-off frequency are investigated as well. The real-time fabrication complexity in terms of presence of interface traps for a damaged device has been compared with a fresh device with absence of interface traps in terms of transfer characteristics and g_m at cryogenic and ambient temperatures thereby ensuring the CMOS compatibility of the A-TFET for quantum computing.

Keywords Asymmetrical · Tunnel FET · Cryogenic · CMOS quantum computing

1 Introduction

Downscaling of Metal–Oxide–Semiconductor Field Effect Transistors (MOSFETs) is often faced by obstacles such as short-channel effects (SCEs) leading to increased Off-state/leakage current (I_{OFF}), static-power dissipation, degrading sub-threshold swing (SS) etc. Higher power consumption is a biproduct of these limitations, which in turn restrict the possibility of further supply voltage reduction and device scaling. Thus, in comparison to conventional MOSFETs, when it comes to low power applications, Tunnel FETs (TFET) acts as a much attractive choice due to its sub-60 mV/dec subthreshold swing and minimized power dissipation. For low power applications, it is reported that the performance of TFET is approximately eight times better than that of a MOSFET [1]. Applications that require precision and optimal reliance, such as the field of sensing, TFET has been proven to give much superior results when compared to conventional FETs [2]. Despite being advantageous over traditional MOSFET, TFETs still encounters various issues such as low On-state current (I_{ON}) and ambipolarity [3–5]. Low I_{ON} in TFETs can be overcome using line-TFET as reported by Agopian et al. due to its higher gain voltage than Fin-Field Effect Transistors (FinFET) and gate-all-around FET (GAA FET) [6]. It was proposed that an z-configured TFET not only improve the On-state current (I_{ON}) but it also significantly reduces the ambipolar conduction. The I_{ON} and the sub-threshold swing (SS) was further enhanced by introducing horizontal pocket doping in source of the Z-TFET [7]. A $GaAs_{0.5}Sb_{0.5}/In_{0.53}Ga_{0.47}As$ heterojunction Z-TFET combined with hetero-gate-dielectric (HGD-HZ-TFET) was designed to improve I_{ON} current and

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analog/RF performance while concurrently reduce the ambipolar conductions [8].

Cryogenic temperature refers to extremely low temperatures where many materials exhibit unique properties, and certain phenomena, particularly quantum effects, become more pronounced. Cryogenic temperature offers advantages for certain electronic devices especially concerning improved performance and reduced power consumption over their ambient temperature counterparts. JFETs at cryogenic temperatures (CT) can act as meticulous measuring device due to a boost in sensitivity and they can also convert electric signals at extremely low current levels making it a perfect candidate for studies that deals with low power applications [9]. The increase in need of faster computing speed has called for the intensive research on the working of Complementary Metal Oxide Semiconductor (CMOS) circuits at sub-10 K i.e., cryogenic temperature [10–13]. Analysis for low noise applications of JLDG MOSFET with high-k gate stack was done at cryogenic temperature and its applicability in the domain of quantum computing was confirmed [14]. A study on junction-less SOI Fin-FET in cryogenic environment was performed to observe its impact on quantum information processing to affirm its usage in the field of quantum technology [15].

In this paper, an Asymmetrical-gate TFET (A-TFET) has been designed to amplify ON-state current (I_{ON}), cut back on ambipolarity and to investigate the transistor electrostatic at cryogenic temperature ranging from 50 to 400 K. Performance metrices such as like SS, I_{ON}/I_{OFF} ratio, transconductance(g_m), parasitic capacitances, transconductance generation factor (g_m/I_{ON}) and cut-off frequency were used for the analysis. For analysis of transistor reliability, the impact of interface trap charge densities has been investigated for transistor electrostatics.

2 Device Structure and Simulation Methodology

The 3-D schematic of the structure is shown in Fig. 1. The A-TFET has source and drain lengths (L_s / L_D) of 30 nm each while the channel length (Lch) is 25 nm. Thus, the total length of the device is 85 nm. The thickness of the silicon body of the device is 10 nm and the gate thickness is 1 nm. Here, SiO_2 and HfO_2 of 2 nm thickness are considered as the gate oxide for the front and back gate, respectively to facilitate the ON state current (I_{ON}). For the generation of vertical tunnelling component, the front gate is placed over the entire $P++$source with a doping concentration of $1\times10^{20}/cm^3$. The intrinsic channel has a doping concentration of $1\times10^{15}/cm^3$ and has the back gate placed over it. The device incorporates the front and back gate consisting of palladium metal with work function ($\phi_m = 4.7$ eV). The $N+$type drain has a

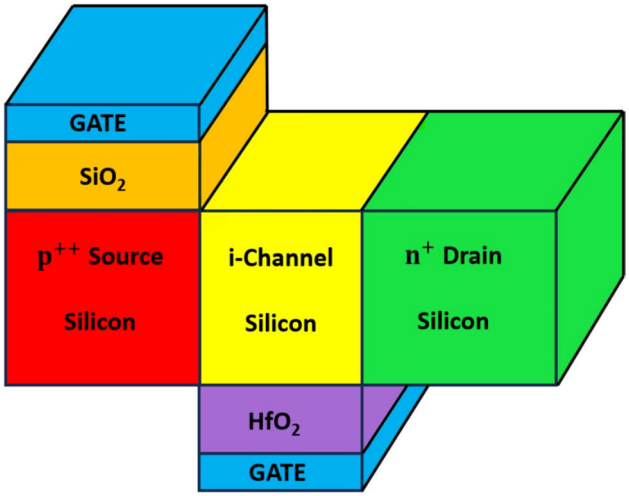

Fig. 1 3-D schematic of the Asymmetrical-gate TFET

doping concentration of $1\times10^{18}/cm^3$. The commercial simulator used for analysis of the A-TFET is SILVACO ATLAS TCAD version 5.0.10.R [16]. The Drift–Diffusion Transport model and the Shockley–Read–Hall (SRH) model were engaged to emulate drifting of carriers within the channel lattice thickness of 10 nm and carrier recombination within the channel lattice/oxide interface respectively. The Bandgap Narrowing (BGN) model was utilized to mirror the reduction of bandgap with the increase in the doping density. The parallel electric field is characterized by activating the FLDMOB model. GIGA, an autonomous-lattice-heating model is activated to implement the temperature variations. LAT. TEMP model is added with a temperature boundary of 4 K to 400 K to foster lattice heating and thermos-contact commands are enabled to solve equations related to it. For heat-induced activation at the source and drain HEAT.FULL was utilized. ANALYTIC model was leveraged to evaluate the effect of temperature on mobility. The band-to-band (BTBT) tunnelling of the TFET device based on WKB approximation is incorporated by the bbt.nonlocal model at the source channel interface. Therefore, a quantum mesh setup has been considered at the source channel interface to facilitate BTBT. Overall, the device meshing is dense at the source channel interface. The Fermi–Dirac statistics is activated by the Fermi model. The drain to source voltage (Vds) is kept constant at 1 V and the gate voltage (V_{gs}) is varied from 0 V to 1.5 V. The possible fabrication steps of the A-TFET are highlighted in Fig. 2 with 3-D schematics in support of [17]. Furthermore, the validity of the A-TFET simulation data has been verified with the experimental results [18] in Fig. 3.

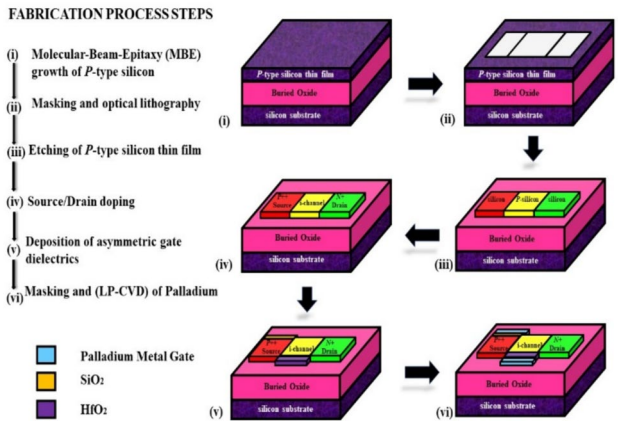

Fig. 2 Potential Fabrication process flow of A-TFET

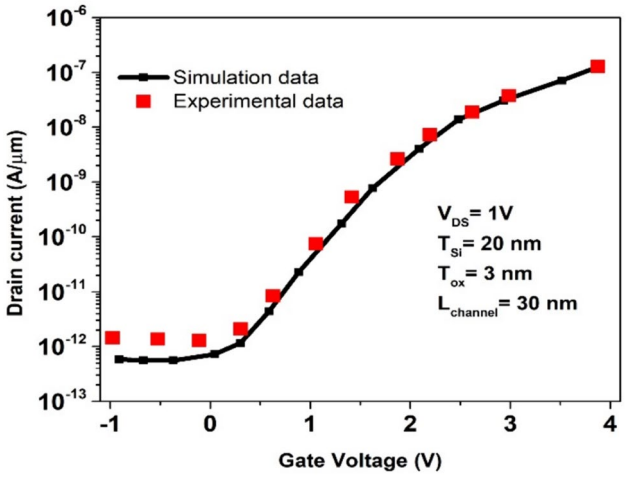

Fig. 3 Calibration results of transfer characteristics for the simulation model against the experimental data [18]

3 Results and Discussion

3.1 Evaluation of Dc Elements Under Cryogenic Environment

The investigation of electrostatic performance of A-TFET is done under cryogenic temperatures (below 78 K, liquid nitrogen temperature). A wide range of temperatures (from 50 to 400 K) has been taken into consideration to make a concise.

overview of the performance variation of the so-called A-TFET. Figure 4 represents the transfer characteristic of A-TFET in the log-y / linear-x scale at $V_{ds} = 1$ V. From the profile, it is observed that when temperature decreases, the threshold voltage (V_{th}) has a positive shift which leads to decrease in the On-state current (I_{ON}). On the other hand,

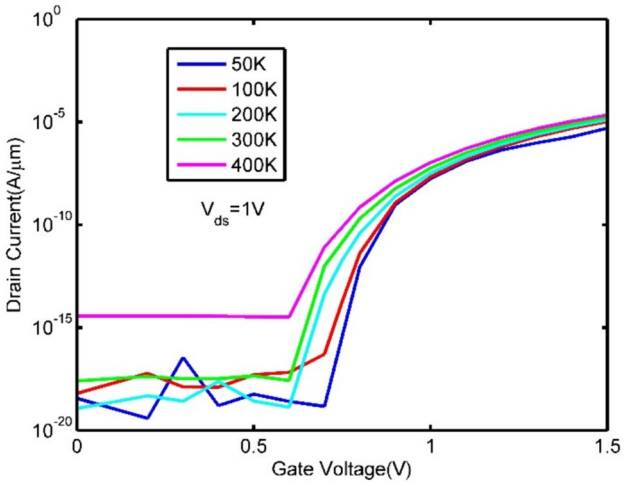

Fig. 4 Transfer characteristic under cryogenic environment at $V_{ds} = 1$ V

when temperature decreases the carrier mobility increases which in turn increases the I_{ON}. One interesting phenomenon to notice is that the carrier mobilities is a function of phonon scattering until 100 K.

Therefore theoretically, due to less phonon scattering the carrier mobilities tends to increase at low temperatures. However, considering cryogenic temperatures, the carrier mobilities is dominated by coulombic as well as surface scattering events that leads to reduction in the mobility [19]. The phenomenon of positive shift in threshold voltage mitigating the I_{ON} and theoretically known effect of lower temperatures amplifying I_{ON} makes the I_{ON} independent of temperature effects at a specific temperature known as temperature-compensation limit. Figure 4. shows that temperature-compensation limit is invalid in this case as I_{ON} remains almost same there is a certain improvement in the in OFF-state current, I_{OFF} (~ five orders) at cryogenic temperature which ultimately boosts transistor performance.

The I_{ON}/I_{OFF} ratio profile as a function of temperatures is investigated in Fig. 5. A steep OFF to ON switching ratio of ~ 10^{15} is observed at 50 K cryogenic temperature however, comparatively poor OFF to ON switching ratio of ~ 10^{10} is observed at 400 K temperature. Therefore, decrease in temperature leads to almost five orders of change in I_{ON}/I_{OFF} ratio. This proves that cryogenic temperature aids in the precise control of the I_{ON}/I_{OFF} ratio of the A-TFET and is suitable for low power and high-performance applications. According to Eq. (1) the sub-threshold slope of a device is governed by the temperature variation [20]. Figure 6. depicts the sub-threshold profile of the A-TFET. It is evident from the figure that there is improvement of the sub-threshold swing by approximately 70% when the temperature reduces from 400 to 50 K (8 mV/dec at 50 K) thereby further solidifying the compatibility for low power applications.

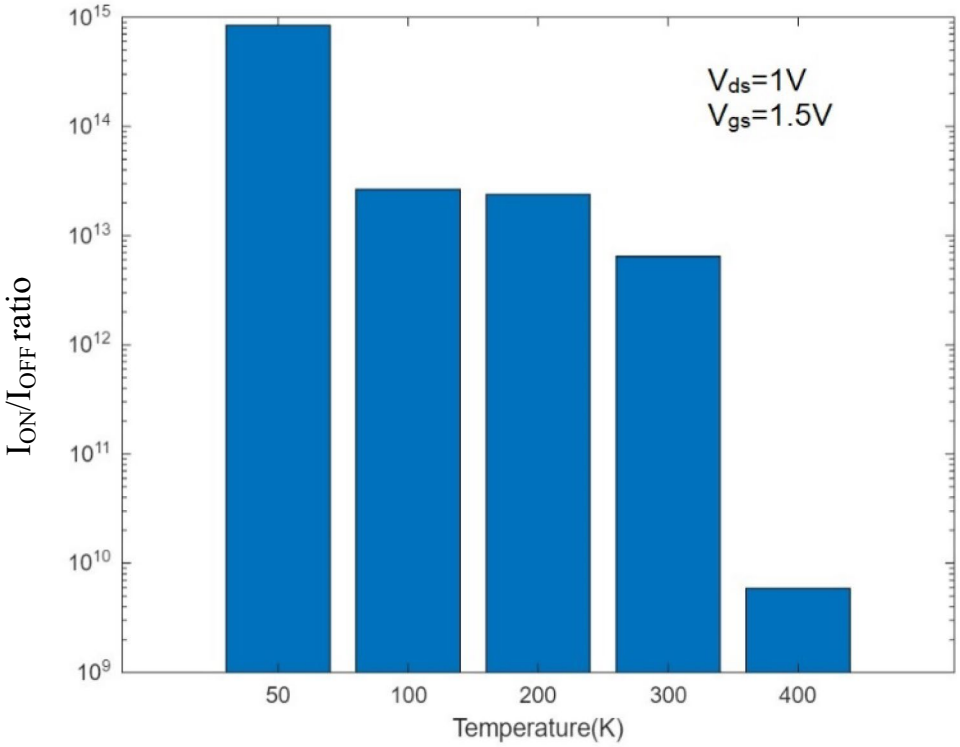

Fig. 5 I_{ON}/I_{OFF} ratio profile under cryogenic environment at Vds = 1 V

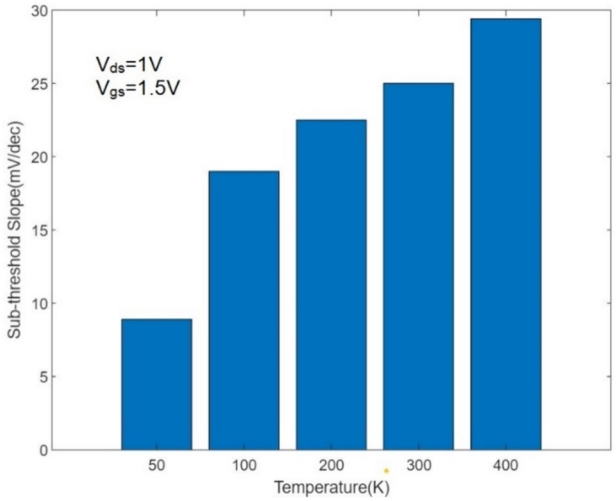

Fig. 6 Sub-threshold slope profile under cryogenic environment at Vds = 1 V

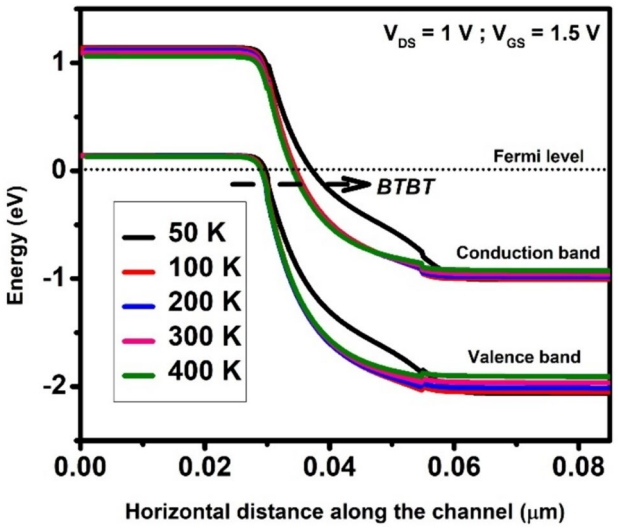

Fig. 7 Energy band diagram of A-TFET along the channel distance as a function under cryogenic environment at Vds = 1 V

$$SS = q^{-1}\gamma K_B T 1n(10) \quad (1)$$

In the above equation q,γ,K_B and T represents charge of an electron, SS factor, Boltzmann constant and temperature respectively. The energy band diagram profile of the A-TFET is shown in Fig. 7 depicting the band-to-band tunnelling (BTBT) phenomenon. As observed, the tunnelling width between the conduction band of the channel and the valence band of the source narrows down for higher temperatures thereby allowing enhanced BTBT rate of carriers from the source to channel [21].

Figure 8 depicts the electric field profile of the A-TFET at cryogenic temperatures. The maximum electric field for 400 K is attributed by its increased I_{ON} from the transfer characteristics (Id-Vg). The reduced threshold voltage from the device transfer characteristics at 400 K results

Table 1 Evaluated performance metrics of A-TFET down to cryogenic temperatures

Temperature (K)	400	300	200	100	50
I_{OFF} (A)	3.69×10^{-15}	2.5×10^{-18}	1.1×10^{-19}	6.3×10^{-19}	3.8×10^{-20}
I_{ON} (A)	2.17×10^{-5}	1.6×10^{-5}	1.3×10^{-5}	1.1×10^{-5}	3.3×10^{-7}
I_{ON}/I_{OFF}	5×10^{9}	8×10^{12}	3×10^{13}	4.5×10^{13}	9×10^{15}
SS (mV/dec)	28	24.8	22.5	18	8
Peak g_m (S)	11×10^{-5}	8×10^{-5}	6.8×10^{-5}	5×10^{-5}	2.3×10^{-5}
Peak g_m/I_{ON} (V^{-1})	1×10^{4}	1.1×10^{6}	1.4×10^{6}	5×10^{3}	5×10^{7}
Peak F_t (Hz)	1.2×10^{10}	2×10^{10}	2.5×10^{10}	3.3×10^{10}	4.4×10^{10}

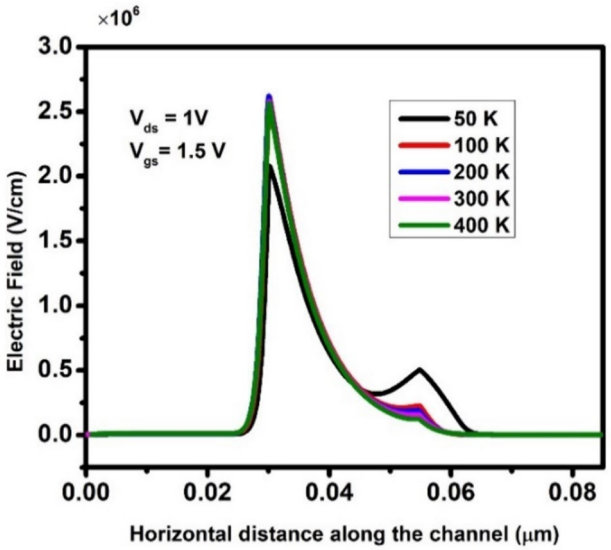

Fig. 8 Electric field profile of A-TFET at cryogenic temperatures

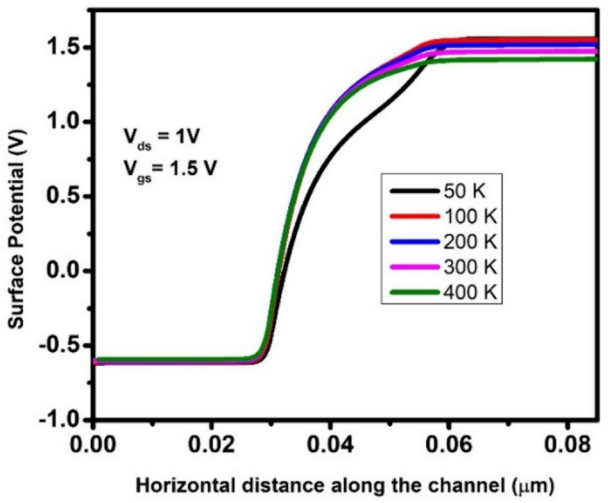

Fig. 9 Surface Potential profile of A-TFET at cryogenic temperatures

in the increased surface potential profile represented in Fig. 9.

3.2 Evaluation of Analog Elements Under Cryogenic Environment

This section takes an in-depth look at the A-TFET performance under the influence of cryogenic temperatures in terms of analog behaviour. Transconductance (g_m) of a device is an essential performance sensing metric given by the first order derivative of the drain current as a function of gate voltage change in (2).

$$g_m = \frac{\partial I_{ON}}{\partial V_{gs}} \tag{2}$$

Transconductance profile is a function of the slope of the transfer characteristics that helps determining the ON to OFF switching speed of the device [22–24]. Figure 10. portray the change in transconductance(g_m) value in accordance with

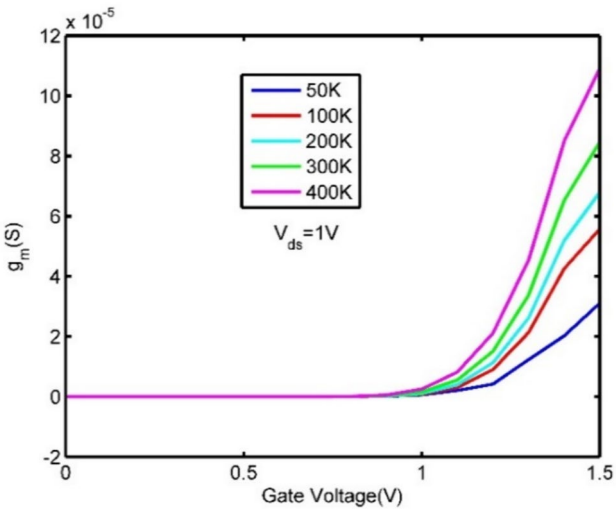

Fig. 10 Transconductance profile under cryogenic environment at Vds = 1 V

the gate voltage for different sub-ambient temperatures while the value of the drain to source voltage (V_{ds}) is kept constant at 1 V. With increase in the gate bias, with the increase of inversion region, the carrier mobility boosts which results in increase in I_{ON} thereby boosting the transconductance profile. However, at maximum gate bias, the profile starts to decrease due to the increased carrier scattering leading to reduced I_{ON} and simultaneously transconductance profile. Thus, as the g_m lowers at cryogenic temperatures, we observe a reduction of approximately 72.73% relative to 400 K.

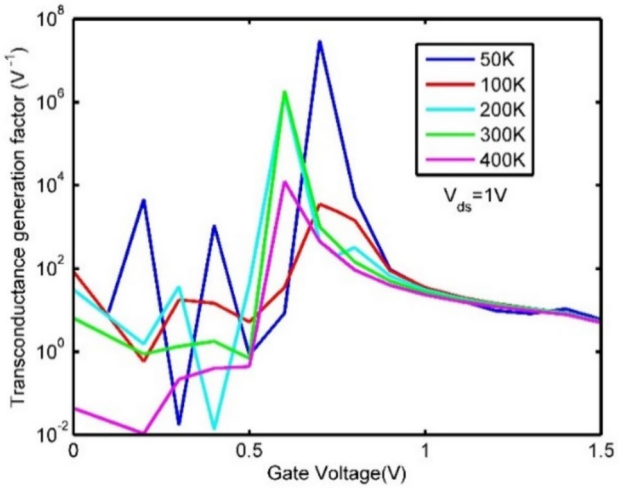

Fig. 11 Transconductance generation factor profile under cryogenic temperatures at Vds = 1 V

Transconductance generation factor is represented by the formula g_m/I_{ON} and it is inversely proportional to subthreshold slope provides a deeper insight to the device sensitivity specifically when it comes to tunnel FETs due to its steeper SS. The values of transconductance generation factors (TGF) are plotted against corresponding gate voltage in Fig. 11. At cryogenic temperatures, maximum TGF values ($\sim 10^7\ V^{-1}$ at 50 K for 0.7 V gate bias) are reported implying minimization in power dissipation [25]. Therefore, we imply a change of almost three orders of magnitude in the peak TGF values at cryogenic temperatures relative to 400 K.

3.3 Evaluation of RF Elements Under Cryogenic Environment

The parasitic capacitances such as gate-to-source capacitance (Cgs), gate-to-drain capacitance (Cgd) and total gate capacitance (Cgg) are depicted through Fig. 12(a), 12(b) and 12(c) respectively depicting small signal analysis of the A-TFET at ultra-low temperature. The value of the total gate capacitance at a particular gate voltage is equivalent to the summation of the gate to source capacitance and gate to drain capacitance corresponding to the same gate

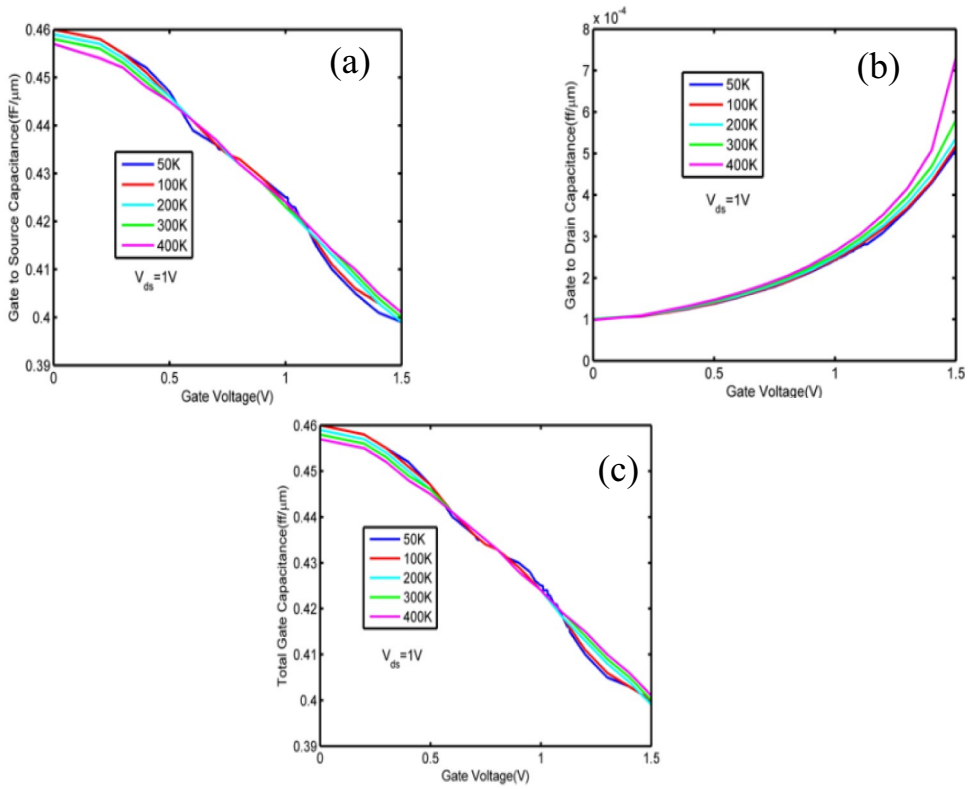

Fig. 12 Profiles of (**a**) C_{gs}, (**b**) C_{gd} and (c) C_{gg} as a function of gate bias under cryogenic environment at Vds = 1 V

voltage ($C_{gg} = C_{gs} + C_{gd}$) [26]. Figure 12(a) and Fig. 12b. reveals that the gate to drain capacitance at a certain gate voltage is very less when compared to that of the gate to source capacitance. As a result, the gate to source capacitance dominates the gate to drain capacitance during the calculation of the total gate capacitance. Thus Fig. 12c, which displays the change of total gate capacitance with respect to the variation in voltage applied at the gate, follows the same patterns as that of Fig. 12(a). i.e., the gate to source capacitance versus gate voltage plot.

Cut-off frequency (F_t) is an important radio frequency (RF) parameter and is determined by Eq. (3) [27–31]. The change in the Cut-off frequency as a function of cryogenic temperatures with varied gate to source bias (V_{gs}) is depicted in Fig. 13. Since Cut-off frequency is directly proportional to transconductance and inversely proportional to total gate capacitance, thus the value will be more for high transconductance and low total gate capacitance [20]. Figure 12 (c). illustrates the fact that the total gate capacitance is very small (order of 10^{-16}), hence the transconductance value dictates the transition or the Cut-off frequency value. This is the reason behind the behaviour of A-TFET at cryogenic temperature follows the pattern as displayed by Fig. 10. Table 1 briefly tabulates the metrics determining the critical implications in the low-power and high-performance applications.

$$F_t = \frac{g_m}{2\pi C_{gg}} \tag{3}$$

In the above equation g_m and C_{gg} represents transconductance and total gate capacitance respectively.

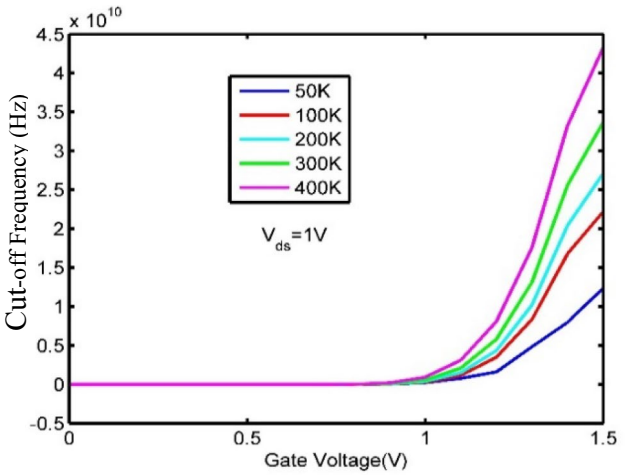

Fig. 13 Cut-off frequency profile as a function of gate bias under cryogenic environment at Vds = 1 V

3.4 Evaluation of Interface Trap Charges Under Cryogenic Condition

The existence of discrete energy levels or trap states at the conjunction of the semiconductor and the dielectric is dictated by the Shockley–Read–Hall recombination theory [32]. The interface trap charge density per unit area is formulated as [15]:

$$Q_{itc} = \int_{Ei}^{+\infty} \eta_{itc}(E) f(E) dE \tag{4}$$

Thus, η_{itc} signifying the total distribution of interface states across the energy. Considering cryogenic temperatures, there's hardly any considerable increase in the dangling bonds concentration at the semiconductor/oxide interface. The dependence of η_{itc} on cryogenic temperatures is due to the sweeping of the fermi level across a significant section of the bandgap [33]. Therefore, η_{itc} play a huge role in terms of understanding the stability of the device under test since it directly affects the threshold voltage of the transfer characteristics. These interface trap states arise from fabrication complexities and thus found in damaged devices. Therefore, devices without traps can be termed as fresh devices. When the η_{itc} is positively charged, donation of electrons commences due to the donor states below conduction band. Similarly, trapping of electrons occurs due to the acceptor state just above the valence band when η_{itc} is negatively charged [23]. This charge polarities affect the surface potential (ψ_s) thereby affecting the flatband voltage [34].

Figure 14(a). and 14(b). shows that the transfer characteristics due to positive trap charge density is slightly higher than the case without any trap charge and negative trap charge density. This is due to the seizing of holes by the by the donor state which ultimately boosts the current. With negative trap charge density, the ON state current drops due to the electron seizing by the acceptors.

Figure 15(a). and Fig. 15(b). illustrates the increase and decrease in transconductance when trap charge density is positive and negative respectively in comparison to the situation where trap charge is absent. Since transconductance is directly proportional to the current, thus increase in current with positive trap charge density increases the transconductance and decrease in current with negative trap charge density reduces the transconductance.

From the above set of Fig. 14(a), (b) and Fig. 15 (a), (b) an observation can be made regarding the fact that the departure of current or transconductance values due to the introduction of trap charges is significantly small across huge range of temperature i.e., 50 K-300 K. Since the change in values of current and transconductance due to introduction of trap

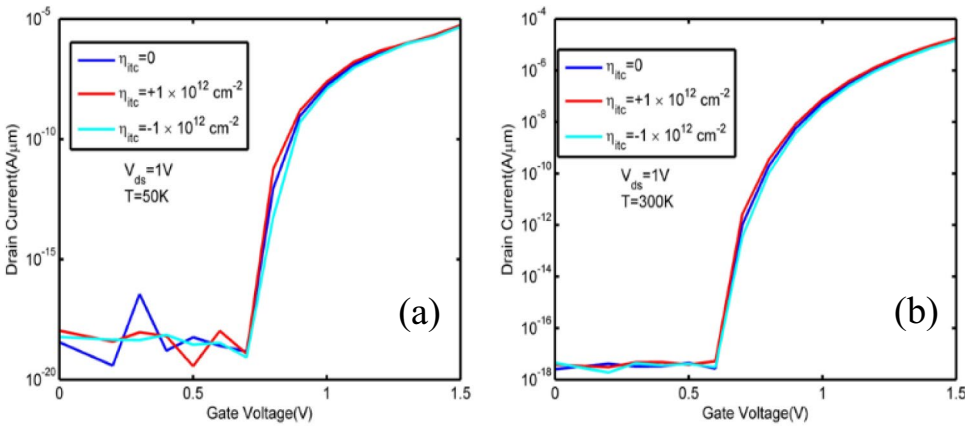

Fig. 14 Transfer profile with and without interface traps charge densities at (**a**) T = 50 K and (**b**) T = 300 K respectively at Vds = 1 V

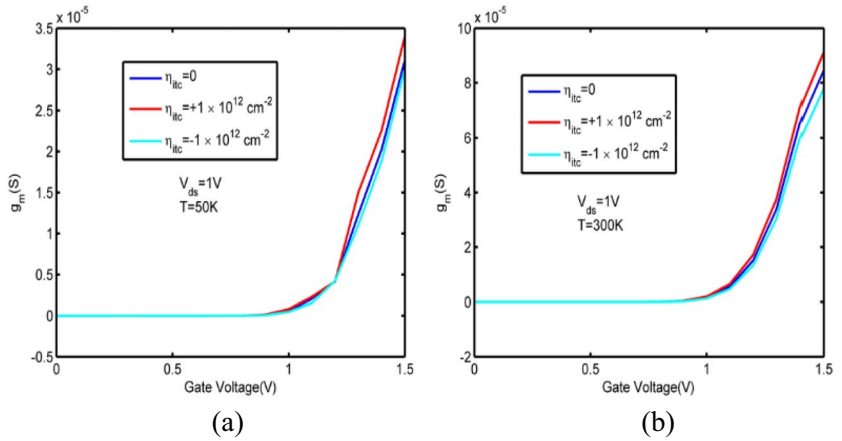

Fig. 15 Transconductance profile with and without interface traps charge densities at (**a**) T = 50 K and (**b**) T = 300 K and Vds = 1 V

Table 2 Performance comparison of A-TFET at cryogenic temperatures

	[35]	[36]	[37]	**This work**
Lch (nm)	30	15–23	28	25
V_{DS} (V)	0.8	0.75	0.9	1.0
I_{ON}/I_{OFF}	-	-	10^6	$\sim 10^{15}$
SS (mV/dec)	30	25	25	8
Peak g_m(S)	19% change	24% change	27% change	72.73% change

charges is almost negligible thus the A-TFET is extremely reliable in ultra-low temperature regime. Table 2 depicts a brief performance comparison with the existing results from different cryogenic temperature-based analysis highlighting the market compatibility of A-TFET.

4 Conclusions

In this paper, analysis of A-TFET has been done under cryogenic environment to study its applicability in the domain of quantum computation and information processing. Investigation of the device under subzero realm led to improvement of device electrostatics which were reflected in the DC, analog and RF elements. Significant improvements were observed in the current, I_{ON}/I_{OFF} ratio, subthreshold swing, transconductance, parasitic capacitances and transition frequency when the device was frozen at subfreezing regime. For reliability assessment inspection was done by introducing intrinsic trap charges at the dielectric-semiconductor conjunction which culminated into showing that the device presents negligible change under the influence of trap charges within temperature range of 50 K-300 K, making the device extremely reliable for applications with calls for precise current outputs. The result from this study shows that due to improved electrostatic parameters and high reliability A-TFET will allow its incorporation with CMOS technology. The A-TFET will be fast, energy-efficient, and unerring at ultra-low

temperature and can play a significant role in the domain of quantum information science.

Author Contributions Sinjini Misra: Formal analysis, methodology, software, validation. Chandreyee Bose: Methodology, software, validation. Rittik Ghosh: Conceptualization, formal analysis, interpretation of results and writing the original draft. Priyanka Saha: Conceptualization, interpretation of results, review, editing, and supervision. All authors reviewed the results and approved the final version of the manuscript.

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Data Availability No datasets were generated or analysed during the current study.

Declarations

Competing Interests The authors declare no competing interests.

Ethics Approval The authors of this paper announce that they have no known competing financial interests or personal associations that may have influenced the work presented in this document. The authors also confirm that this manuscript has not been published elsewhere and is not under consideration by another journal. All the authors have approved the manuscript and agree with its submission to Silicon journal.

Consent to Participate The authors of this paper voluntarily agree to contribute in this work.

Consent for Publication Not applicable.

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