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RESEARCH

A Theoretical Performance and Reliability Investigation of a Vertical Hetero Oxide Based JL-TFET under Ideal Conditions

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Abstract

The fabrication complexity, leakage current, low-power operation, and cost of nano-scale devices are major concerns. To address these challenges, we propose a dual oxide-based approach to enhance the performance of the dual oxide electrically doped junction-less tunnel field-effect transistor (DO-ED-JL-TFET). For this purpose, the oxide layer (T_{ox}) is vertically segmented into two sections. The lower section comprises SiO_2 (low-K dielectric), while the upper section incorporates HfO_2 (high-K dielectric). This segmentation enhances the capacitive coupling between the gate and channel area, resulting in a reduced tunneling width near the source-channel region. Moreover, a polarity gate bias (electrically doped) of PG = -1.2 V is applied to create a P^+ source region over the thin silicon body. The proposed device addresses challenges such as random dopant fluctuation, thermal budget, and fabrication complexity issues compared to conventional TFETs. The performance of the proposed device has been assessed in terms of variations in carrier concentrations, electric field, energy band diagram, transfer (I_{ds} - V_{gs}) characteristics, subthreshold swing (SS), and switching ratio (I_{on}/I_{off}). Moreover, analog/RF performance parameters such as transconductance (g_m), cutoff frequency (f_T), and gain bandwidth product (GBP) are also analyzed and compared with conventional ED-JL-TFET. Furthermore, the impact of trap charges at the oxide-semiconductor interface on device performance is investigated for reliability. Simulated results demonstrate that DO-ED-JL-TFET exhibits greater immunity to various types of ITCs compared to conventional ED-JL-TFET, making it a more reliable choice for applications in radioactive environments.

Keywords Dual-Oxide (DO) · Electrically Doped (ED) · Junctionless (JL) · Polarity Gate (PG)

1 Introduction

As the device dimensions of the conventional metal-oxide-semiconductor field-effect transistor (MOSFET) are scaled down, it gives rise to certain constraints. These include drain-induced barrier lowering (DIBL), reduced switching ratio (I_{on}/I_{off}), increased power dissipation due to leakage, and a subthreshold swing (SS) limitation of 60 mV/decade. To address these challenges, various device structures have been explored, like multi-gate MOSFETs [1–4], impact ionization MOS (IMOS) [5], and junctionless transistors [6]. The use of multi-gate MOSFETs offers the SS of approximately 60 mV/decade and addresses the issues of short-channel effects (SCEs) up to a limited extent. Meanwhile, IMOS exhibits SS of $<$ 60 mV/decade, a very high I_{on}/I_{off}, and a high breakdown voltage requirement, increased fabrication complexity. Junction-less transistors exhibit electrical characteristics (SS $>$ 60mV/decade) very similar to multi-gate FETs but with reduced fabrication complexity. As a result, improvements in achieving low SS and reducing leakage current are needed for low-power high-speed applications. In this regard, tunnel field-effect transistors (TFETs) have emerged as potential candidates for ultra-low power high-speed applications [7–10], owing to their low I_{off}, SS of $<$ 60 mV/decade and operation at low supply voltage. TFETs offer superior performance and provide a promising opportunity to address the challenges associated with downscaling conventional MOSFETs. However, significant challenges in TFETs include low ON-state current (I_{on}) and ambipolar current conduction. To enhance the I_{on} [10–16] and suppress the ambipolar current

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[17–19], various methods have been employed in the literature.Furthermore, the fabrication of doped source and drain regions for nano-scale devices necessitates a more extensive thermal budget. This is due to the use of ion implantation, expensive thermal annealing techniques, and the difficulties in achieving an abrupt junction. This is particularly evident in the case of physically doped P^+-i-N^+ TFETs, where carrier diffusion from source/drain regions to the channel region further complicates the attainment of an abrupt junction. Hence, conventional TFETs suffer from random dopant fluctuations (RDF) [21] and fabrication complexity resulting in the degradation of device performance. The earlier proposed approach is based on conventional doping which is highly doped and requires a higher thermal budget. Moreover, RDF happens due to a high concentration gradient in the conventional TFET. To overcome such challenges JLTFET has been proposed [22] but a thermal budget is still required for the formation of pin structure. To address such an issue, dopingless (charge plasma) TFET has recently been explored and demonstrated better control over the channel, with reduced thermal budget and process complexity [23]. The proposed device adopts the dopingless concept, employing electrostatic doping instead of charge plasma for carrier concentration beneath the source/drain region, allowing for dynamic configuration [24].

This device utilizes a vertical dual oxide (DO) layer to the conventional ED-JL-TFET, referred to as the DO-ED-JL-TFET (proposed device). In this technique, the vertical oxide layer is divided into two distinct layers. The region near the gate is primarily composed of HfO_2, while the region near the Si intrinsic layer is predominantly composed of SiO_2. By employing these dielectric materials, the proposed device exhibits improvements in I_{on}, SS, I_{on}/I_{off} ratio, and Analog/RF figures of merit (FOMs). This enhancement arises from the improved capacitive coupling between the channel-gate area, leading to increased band-to-band tunneling (enhanced electric field) at the source-channel region compared to conventional devices. Therefore, the proposed device (DO-ED-JL-TFET) is well-suited for applications requiring rapid switching and low power consumption.

The work presented in this paper is organized as follows: Section 2 describes the design parameters and simulation environment. In Section 3, the simulation results are analyzed in six parts. The first part covers the analysis of various oxide layers, the second part focuses on the optimization of dual oxide thickness, the third part presents DC performance, the fourth part discusses analog/RF performance, fifth part explores the effect of Interface Trap Charges (ITCs) on DC, analog/RF performance, and the linearity performance parameters in the sixth part. Finally, Section 4 concludes the work by summarizing its key findings.

2 Device Structure and Simulation Setup

Figure 1(a-b) illustrates the structural views of conventional ED-JL-TFET and the proposed DO-ED-JL-TFET. The proposed device incorporates a vertical hetero oxide layers consisting of a combination of silicon dioxide (SiO_2) and hafnium dioxide (HfO_2) as an intermediate layer between the channel and gate electrodes, with two isolated gates (CG and PG) having identical work functions. The N^+ substrate i.e. N^+-N^+-N^+ (drain, channel, source) is initially heavily doped ($1\times10^{19} cm^{-3}$), undergoes a conversion into the intrinsic layer below the control gate (CG) and polarity gate (PG) by applying work functions (4.72 eV) [25]. Further, the proposed structure employs a polarity gate bias voltage of -1.2 V and a work function of ϕ_{PG} = 4.72 eV to induce P^+ region and achieve the desired carrier concentration ($1\times10^{19} cm^{-3}$) in the source region [26]. Therefore, the structure operates as an N^+-i-P^+ gated structure similar to conventional TFET, where the control gate is employed to adjust the effective tunneling barrier width. Apart from these considerations, the source gap length ($L_{gap,s}$) spacer is kept constant at 5 nm between the control gate and

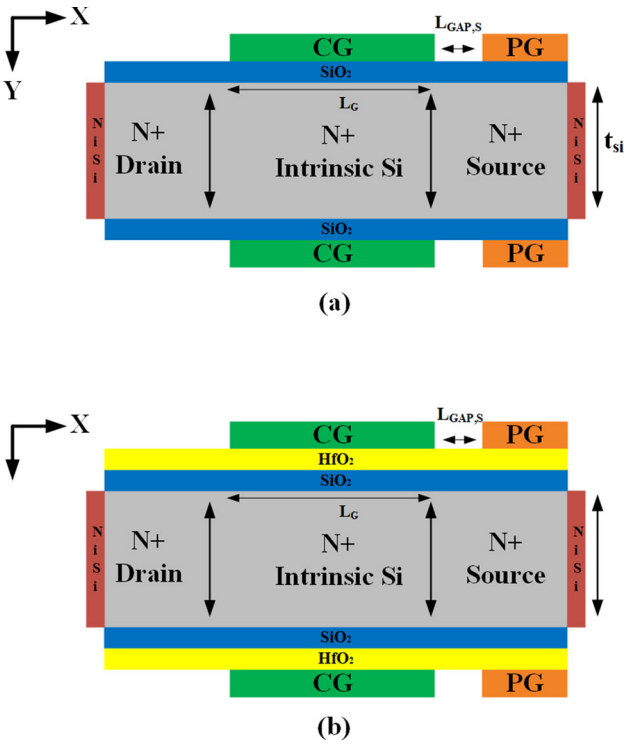

Fig. 1 Structure of (a) conventional ED-JL-TFET and (b) proposed DO-ED-JL-TFET

polarity gate. This ensures enhanced abruptness between the source and channel junction, reducing the tunneling barrier width and increasing tunneling current [24, 26]. An N^+-i-P^+ TFET structure is formed using electrical doping instead of physical doping. As a result, the structure exhibits lower variability, and short-channel effects (SCEs), and outperforms conventional TFETs. The use of nickel-silicide (NiSi) with a near-midgap metal work function and a barrier height of 0.45 eV has been proposed for source and drain contacts [26]. Based on the findings of the literature research and prevailing technological advancements, a gate length of 50 nm has been considered. Previous research has demonstrated the influence of gate length on the performance of TFET [27]. The channel length modulation primarily affects the OFF-state performance, with the ON-state performance remaining relatively unchanged. Specifically, the OFF-state current increases as the gate length decreases, attributed to the reduction in tunneling barrier width. In contrast, the ON-state current experiences minimal change due to quantum tunneling rather than the drift-diffusion mechanism. Consequently, when the gate length is less than 50 nm, the ON-state current remains relatively constant. Table 1 provides a detailed description of the design parameters used in the simulation.

The electrical characteristics of both the conventional and proposed devices are obtained using the Silvaco ATLAS 5.20.2 R device simulator [28]. For this, various models were incorporated into the simulation setup. Both the nonlocal and local BTBT models are utilized, as the operation of the proposed device depends on band-to-band tunneling (BTBT). These models effectively capture the tunneling process within the energy band. Nickel Silicide (NiSi) with a work function close to midgap and a barrier height of 0.45 eV serves as electrodes for both the source and drain regions. The Universal Schottky Tunneling (UST) model is also considered in this context. The trap-assisted tunneling model is additionally incorporated [26]. Furthermore, Shockley-Read-Hall and Auger recombination models are employed to address high impurity concentrations in the channel and account for minority recombination effects [29]. The Band Gap Narrowing (BGN) model is incorporated to accommodate the high doping concentration in the channel region. Additionally, other models such as the concentration-dependent mobility model (CONMOB), Fermi-Dirac model, and field-dependent mobility model (FLDMOB) are also utilized [29].

Table 1 Design parameters used for the device simulation

Parameter name	Symbol	Value	Unit
Silicon body thickness	T_{body}	10	nm
Silicon body length (X)	L_{body}	160	nm
Channel doping	N_{ch}	1×10^{19}	cm^{-3}
Source length	L_s	50	nm
Gate length	L_g	50	nm
Drain length	L_d	55	nm
Source gap length	$L_{gap,S}$	5	nm
Physical oxide thickness	T_{ox}	2	nm
HfO_2 oxide thickness	H_{ox}	1.6	nm
SiO_2 oxide thickness	S_{ox}	0.4	nm
Polarity gate workfunction	ϕ_{PG}	4.72	eV
Polarity gate voltage	ϕ_{PG}	-1.2	V
Control gate workfunction	ϕ_{CG}	4.72	eV
Trap charge density	N_f	$\pm1\times10^{12}$	cm^{-2}

The proposed DO-ED-TFET can be fabricated using non-planar technologies, where the major fabrication process steps are as follows: The channel can be formed using deep reactive ion etching or Bosch processes [30]. Following this, gate oxide can be deposited on the complete channel, followed by an HfO_2 layer deposition over the oxide layer using Atomic Layer Deposition (ALD) or chemical vapor deposition (CVD). The control gate (CG) deposition is carried out. Nickel silicide (NiSi) source/drain contacts can be epitaxially grown over the substrate. The polarity gate (PG) can be formed all around the channel using e-beam lithography [31]. Subsequently, spacer formation and contact deposition can be performed.

3 Results and Discussions

This section presents the performance analysis of the proposed DO-ED-JL TFET. In this context, the investigation explores the impact of different vertical hetero gate oxides on electrical characteristics, followed by the optimization of the oxide thickness for the proposed device. Subsequently, the DC performance of the proposed device is examined, considering variations in the carrier concentration profile, energy band diagram, electric field, transfer characteristics, and switching ratio (I_{on}/I_{off}). Moreover, analog/RF performance parameters, including parasitic capacitance, g_m, f_T, and GBP, are analyzed. To delve into device reliability, the impact of trap charges on DC, analog/RF, and linearity performance parameters is studied. This analysis takes into account the interface charge density of $N_f = \pm1\times10^{12}\ cm^{-2}$ at the oxide-semiconductor interface.

3.1 Investigation of Oxide Layers on Device Structure

In this subsection, to investigate the impact of the oxide layer on device performance, we have considered various configurations as illustrated in Fig. 2(a-d). These configurations are determined by the vertical hetero oxide region, with a fixed physical oxide thickness of 2 nm. The devices are labeled

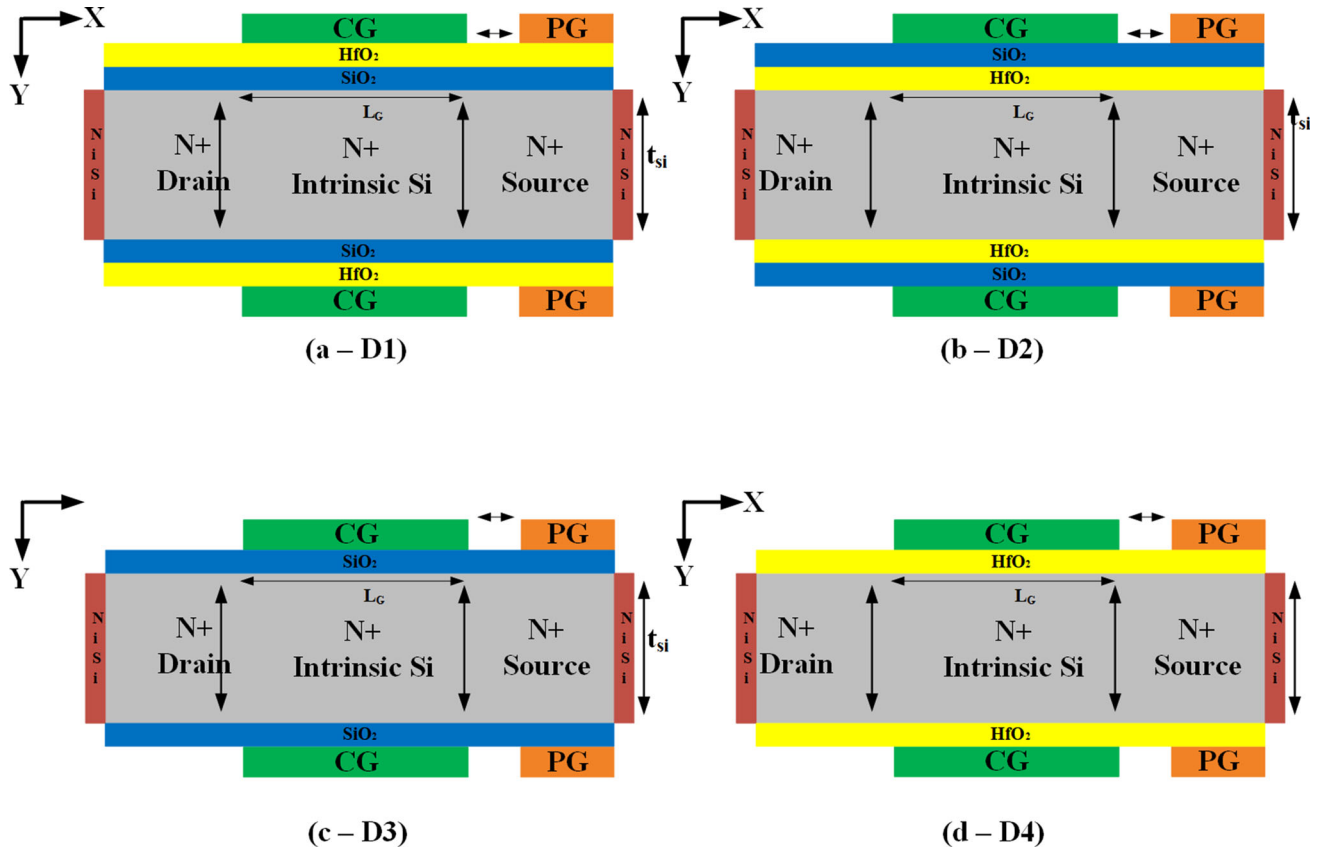

Fig. 2 Different device configurations (a) D1 (upper oxide layer HfO_2 and lower oxide layer SiO_2), (b) D2 (upper oxide layer SiO_2 and lower oxide layer HfO_2), (c) D3 (upper and lower oxide layer SiO_2), and (d) D4 (upper and lower oxide layer HfO_2)

as D1, D2, D3, and D4, and a complete alignment of these devices is provided in Table 2.

Figure 3(a) illustrates the energy band variation in the ON condition for all device configurations (D1, D2, D3, and D4). The band bending for D1 and D4 is greater than that of D2 and D3 due to a higher number of electrons generated in the presence of the high-K dielectric material (HfO_2), which has a greater thickness compared to the low-K dielectric material (SiO_2). Additionally, D1 and D4 exhibit a higher electric field owing to the enhanced coupling provided by HfO_2, as depicted in Fig. 3(b). Figure 3(c-d) presents the electrical characteristics and Point SS, along with the threshold voltage(V_{th}) at a gate voltage of 1.0 V. The increased electric field in D1 and D4, compared to D2 and D3, results in an improvement in the ON-state current, which is notably higher for D1 and D4 devices, followed by D2 and D3 devices. However, D4 devices experience a higher threshold voltage (V_{th}) and a higher point subthreshold swing (SS), which may not be favorable for high switching applications, potentially degrading device performance, as illustrated in Fig. 3(d). Considering the configurations of different devices, we have selected the proposed device as D1 due to its higher ON-current, lower point subthreshold swing (SS), and attainment of V_{th} at lower gate voltages. These parameters are crucial for enhancing the device and enabling its use in circuits, high-frequency, and fast-switching applications.

Table 2 Different configurations of device based on vertical oxides

Device names	Upper layer of oxide	Lower layer of oxide
D1	HfO_2	SiO_2
D2	SiO_2	HfO_2
D3	SiO_2	SiO_2
D4	HfO_2	HfO_2

3.2 Optimization of Oxide Thickness

In this subsection, we have explored various scenarios for the thickness of HfO_2 on the proposed device. The key principle to note is that an increase in the thickness of HfO_2 results in a reduction in the thickness of SiO_2; conversely, a decrease in the thickness of HfO_2 leads to an increase in the thickness of SiO_2. This approach is employed to maintain a consistent physical oxide thickness compared to a conventional

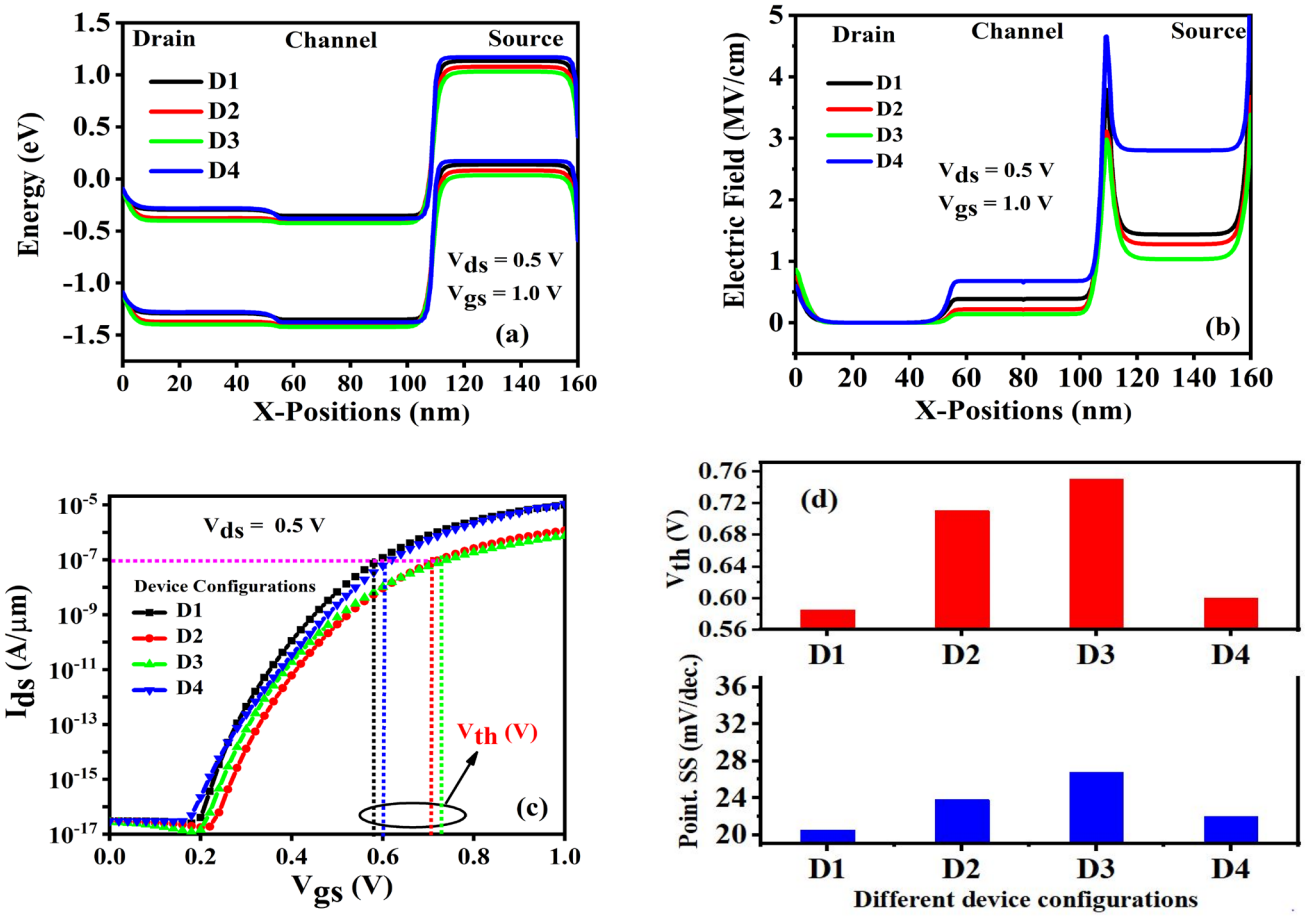

Fig. 3 Impact of vertical hetero oxide layers on (a) Energy Band Diagram (ON condition), (b) Electric Field, (c) $I_{ds} - V_{gs}$ characteristics, and (d) Point. SS along with V_{th} for D1, D2, D3 and D4 devices

device. Additionally, optimization has been conducted concerning carrier concentration, energy band profile, electrical characteristics, point subthreshold swing, I_{on}/I_{off} ratio, and transconductance (g_m). Figure 4(a-b) depicts plots of the carrier (electron and hole) concentration and energy band profile under thermal equilibrium conditions. From both figures, it is evident that no electrons are in motion in this state at the gate-to-channel interface, and minimal variation is observed. In Fig. 4(c), there is an increase in the generation of electrons as the thickness of HfO_2 increases in the ON condition. This is attributed to a reduction in tunneling width at the source-channel interface, leading to a higher capacitive coupling at the channel-to-gate interface. This increases the ON current (I_{on}), as confirmed by Fig. 4(d), and a lower threshold voltage (V_{th}) is observed at higher thicknesses of HfO_2. The thicknesses of SiO_2 and HfO_2 significantly impact both ON-state and OFF-state currents, as depicted in Fig. 4(d). It is observed from the figure that increasing the HfO_2 thickness and decreasing the SiO_2 thickness result in an increase in the ON-state current, attributed to the enhanced coupling between the gate and channel. Furthermore, this increase in ON-state current is governed by the reduction of the tunneling barrier width. Conversely, a decrease in HfO_2 thickness and an increase in SiO_2 thickness lead to a decrease in the ON-state current. Consequently, the I_{on}/I_{off} ratio ratio increases with the increment of HfO_2 thickness. In Fig. 5(a), the I_{on}/I_{off} ratio and point subthreshold slope (SS) are plotted by varying the thickness of HfO_2. It is evident that the I_{on}/I_{off} ratio increases and SS decreases with an increase in thickness. Notably, a higher ratio and lower point SS are observed at a thickness of HfO_2, making it more suitable for switching applications. Consequently, the optimal thickness is chosen at HfO_2 = 1.6 nm, SiO_2 = 0.4 nm, and a total oxide thickness (T_{ox}) of 2 nm. Furthermore, Fig. 5(b) displays the plot of transconductance (g_m) variation with V_{gs}. The proposed thickness offers higher g_m compared to other thicknesses of HfO_2 due to an increase in tunneling current. Hence, it can be concluded that for the selected thickness, the device exhibits a higher ON-state current, I_{on}/I_{off} ratio, and g_m, along with improved subthreshold slope (SS) and threshold voltage (V_{th}). These parameters are essential in designing for high-frequency and low-circuit applications.

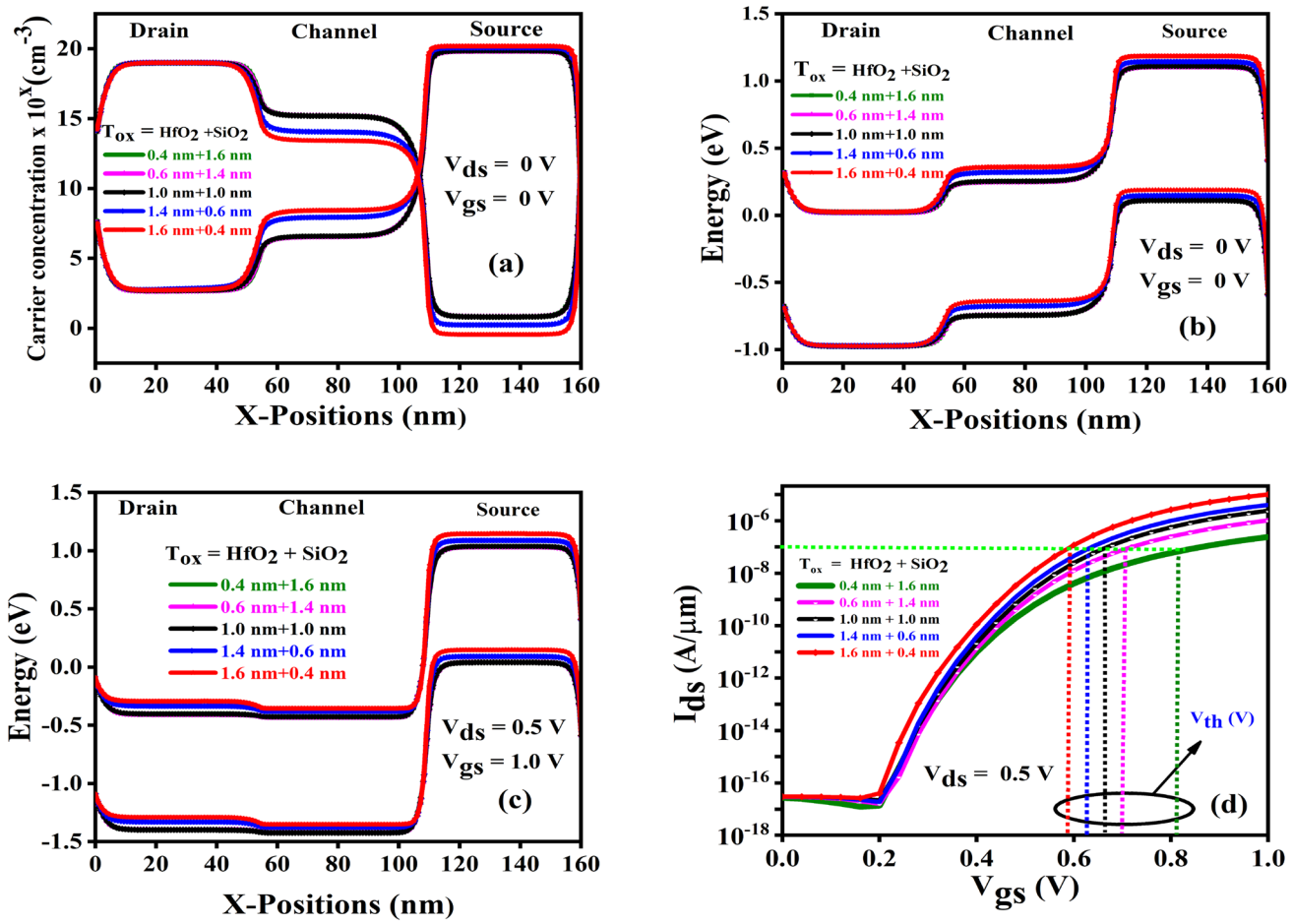

Fig. 4 Optimization of vertical hetero oxide thickness for DO-ED-JL-TFET (a) carrier concentration, (b-c) Energy band profile in thermal equilibrium and ON condition, (d) transfer Characteristics

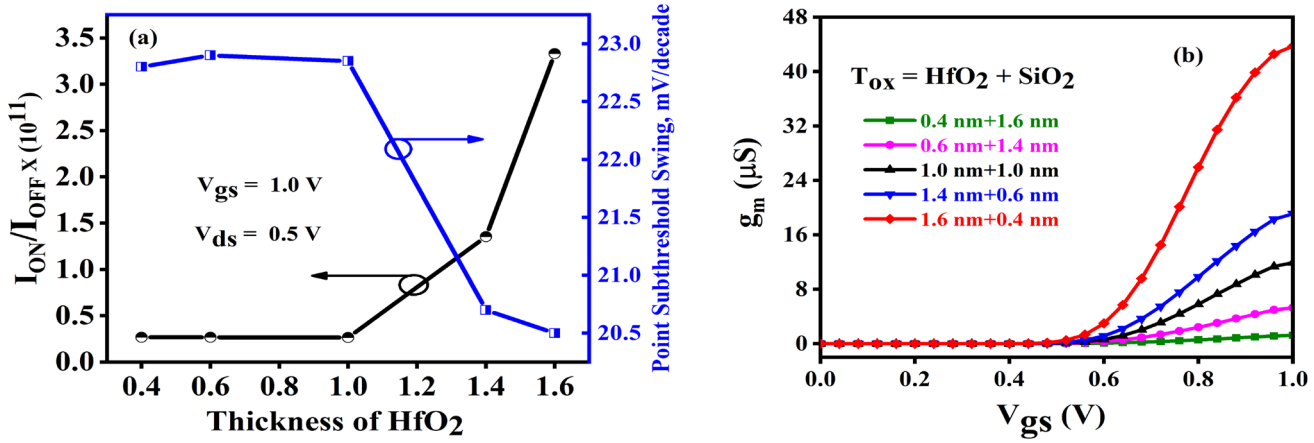

Fig. 5 Optimization of oxide thickness for DO-ED-JL-TFET (a) I_{on}/I_{off} ratio, Point. SS and (b) transconductance

3.3 DC Performance Parameters

Figure 6(a) illustrates the electron and hole concentrations in thermal equilibrium for conventional ED-JL-TFET and proposed DO-ED-JL-TFET. There is no significant increase in the electron concentration near the gate region. In Fig. 6(b-c), the energy band diagram is depicted under thermal equilibrium and ON state conditions. In the thermal equilibrium state, no tunneling occurs between the channel and source regions for electrons. However, in the ON state (Fig. 6(c)), increased tunneling is observed at the source-channel (S-C) region. This suggests a higher generation of electrons due to the reduction in the barrier width at the S-C region. Additionally, the use of dual oxide enhances the coupling between the gate-channel interfaces in the proposed device, leading to increased tunneling compared to conventional devices. Figure 6(d) illustrates the electric field in the ON-state condition of the DO-ED-JL-TFET. The tunneling rate (G_{BTBT}) depends on the electric field (ε), as expressed by the following equation [32]:

$$G_{BTBT} = A\varepsilon^{\sigma} \exp\left(-\frac{B}{\varepsilon}\right) \tag{1}$$

Where constant A primarily depends on the effective mass of an electron, B represents the tunneling probability constant, and σ represents the transition constant. Further, the probability of tunneling of the carrier at the tunneling barrier is analyzed by the approximation of Wentzel-Kramer-Brillouin (WKB) [32].

$$T_{WKB} \propto \exp\left[-\frac{4\lambda\sqrt{2m^*}\sqrt{E_g{}^3}}{3qh(E_g + \Delta\phi)}\right] \tag{2}$$

Here, m^* is the effective mass of an electron, q represents the electron charge, h represents Plank's constant, E_g is the effective bandgap, λ is the width of tunneling barrier, and $\Delta\phi$ represents the energy overlap where the tunneling occurs. This proposed device exhibits a larger electric field due to the presence of dual oxide materials, namely HfO_2 and SiO_2. Consequently, the proposed device yields a higher ON-state current, facilitated by significant energy band bending, allowing a greater number of electrons to traverse the tunneling width, as evident from the $I_{ds} - V_{gs}$ characteristics shown in Fig. 7(a).

Moreover, a lower V_{th} value is required for a device to operate at low-power applications. In this regard, from the

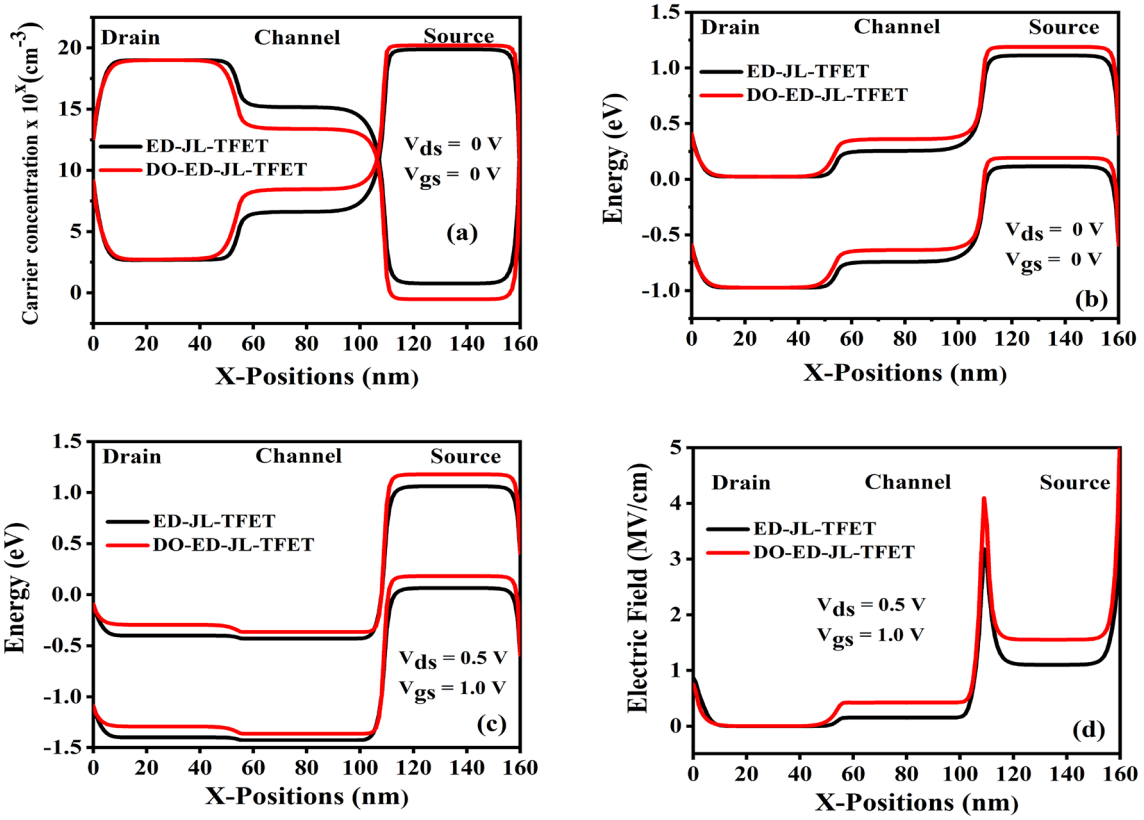

Fig. 6 Comparison between ED-JL-TFET and DO-ED-JL-TFET in terms of (a) Carrier concentration, (b-c) Energy band diagram under thermal equilibrium and ON condition, and (d) Electric field variation

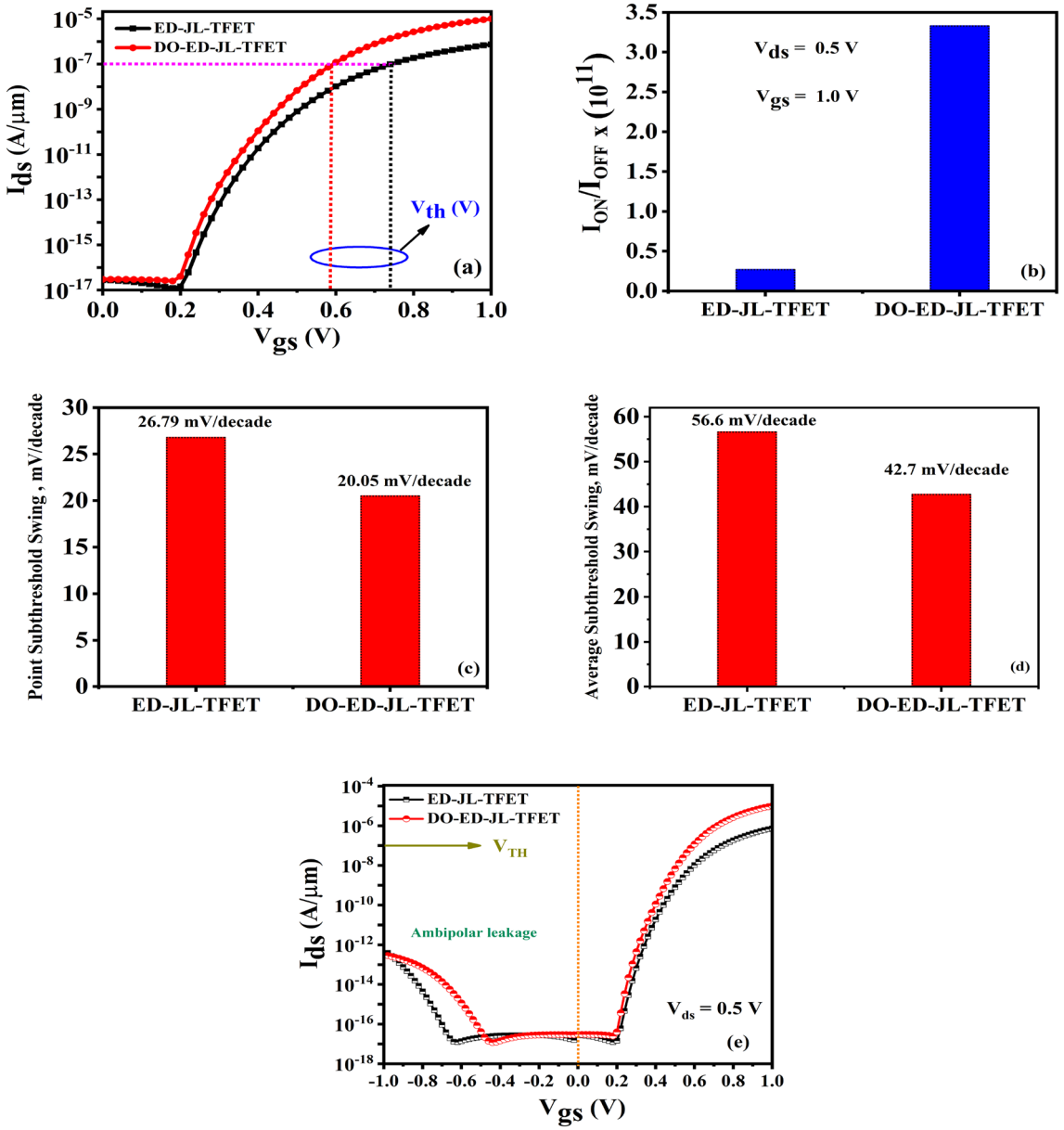

Fig. 7 Performance comparison of ED-JL-TFET and DO-ED-JL-TFET in terms of (a) $I_{ds} - V_{gs}$ characteristics, (b) I_{on}/I_{off} ratio, (c) Point SS, (d) Average SS, and (e) Ambipolar current conduction

$I_{ds} - V_{gs}$ characteristics V_{th} is calculated using constant current. From the Fig. 7(a), a V_{th} of 0.74V and 0.59 V are obtained for ED-JL-TFET and DO-ED-JL-TFET, respectively. Figure 7(b) illustrate the switching ratio (I_{on}/I_{off}) variations for both devices. The proposed device exhibits a better switching ratio (3.32×10^{11}) as compared to the conventional device (2.68×10^{10}). This indicates that the proposed device is suitable for low-power digital switching applications. To further explore the device's suitability for low-power applications, we investigated the subthreshold swing (SS) of both devices. A lower SS is preferable for enhanced energy efficiency, crucial in designing low-power circuits for various applications. Figure 7(c) and (d) illustrate the comparative point and average subthreshold swing of ED-JL-TFET and DO-ED-JL-TFET. The point and average SS are evaluated using the expression [33].

$$SS_{point} = \left(\frac{\delta V_{gs}}{\delta \log I_{ds}}\right) mV/decade \tag{3}$$

$$SS_{avg} = \frac{(V_{th} - V_{OFF})}{\log(I_{V_{th}}) - \log(I_{OFF})} \tag{4}$$

The proposed DO-ED-JL-TFET exhibits lower subthreshold swings (both point and average) due to the incorporation of dual oxide, indicating its suitability for low-power, energy-efficient circuit designs. From the above DC performance parameter results, it can be concluded that the proposed device demonstrates a significantly improved V_{th} of approximately 0.59 V, in contrast to the conventional device with a V_{th} of 0.74 V. Furthermore, the proposed device exhibits superior average SS (42.7 mV/decade) and point SS (20.05 mV/decade) and a higher switching ratio (3.32×10^{11}) as depicted in Fig. 7(b-d).

The ambipolar current conduction is one of the major limitations of TFET. Therefore, the ambipolar behavior of the proposed device is shown in Fig. 7(e). The ambipolar current occurs due to a negative gate bias at the gate terminal for the n-type TFET, as illustrated in the figure. Ambipolar conduction arises from the alignment of the conduction band of the channel and the conduction band of the drain, initiating tunneling at the drain junction. This parameter holds significant importance in TFET, where minimizing the ambipolar current is crucial for proper circuit operation. From the figure, it becomes evident that the proposed vertical hetero-oxide exhibits a higher ambipolar current compared to the conventional ED-JL-TFET. The ambipolar behavior in TFET is attributed to the symmetric N^+ and P^+ regions. Consequently, n-type tunneling occurs with a positive gate voltage, while p-type tunneling occurs with a negative gate voltage for n-TFET. The reverse holds for p-TFET. The similar transfer characteristics under positive and negative gate bias conditions lead to parasitic conduction during the OFF state. To address the ambipolar behavior, several methods have been employed in TFET, such as the utilization of a heterogeneous gate dielectric, Employing various doping profiles in the drain region, and Incorporating a large band gap material on the drain side to enhance tunneling width.

3.4 Radio Frequency Performance Analysis

This subsection presents the performance analysis of conventional ED-JL-TFET and proposed DO-ED-JL-TFET in terms of various analog/RF performance parameters such as parasitic capacitance (C_{gs}, C_{gd}), transconductance (g_m), cutoff frequency (f_T), and gain bandwidth product (GBP). All these parameters are obtained at 1 MHz frequency. The operation of the device at high frequencies (HF) is constrained by parasitic capacitances inherent in its structure, which degrade high-frequency behavior by influencing the switching speed, power consumption, and overall efficiency of the device. Figure 8(a) illustrates the total gate capacitance (C_{gg}) as a function of V_{gs}. The C_{gg} is the sum of the gate-to-source capacitance and the gate-to-drain capacitance (i.e., C_{gs} + C_{gd}). It is evident that the capacitance C_{gd} grows as the gate bias increases, mostly because the width of the potential barrier at the drain-channel region decreases. Similarly, the capacitance C_{gs} also increases with gate bias, but the variation is not as significant as that of C_{gd}. This is because C_{gs} is influenced by the barrier width at the source-channel region. Furthermore, at higher gate bias, C_{gd} is greater than C_{gs}. Therefore, the gate capacitance (C_{gg}) of the proposed device increases when the gate bias is increased. The gate-to-source capacitance (C_{gs}) and gate-to-drain capacitance (C_{gd}) are extracted from small signal analysis, and also expressed as per the following equations [34]:

$$C_{gs} = C_{gsi} + C_{fext} + C_{fint} \tag{5}$$

$$C_{gd} = C_{gdi} + C_{fext} + C_{fint} \tag{6}$$

Here, the external fringing capacitance is denoted as C_{fext}, while the internal fringing capacitance is represented by C_{fint}. The combined internal and external fringing electric field can influence analog/RF performance, particularly in the presence of external capacitances. The computation of these two fringing capacitances is executed using a substitute approach, as detailed in [34, 35]. The utilization of this method facilitates the determination of the total gate capacitance, as articulated below:

$$C_{gg} = C_{gs} + C_{gd} = \left| \frac{Im(Y_{11} + Y_{12})}{\omega} \right| \tag{7}$$

Here, $\omega = 2\pi f$ and f = applied frequency.

The transconductance (g_m) parameter of a device plays a crucial role in the analysis and design of circuits, especially in applications such as amplifiers and signal processing where attaining high gain is essential. In this regard, Fig. 8(b) illustrates the g_m variation of both devices with V_{gs}. It can be noted that the g_m increases as the V_{gs} increases. However, at higher V_{gs}, the g_m starts to decline due to the loss of mobility. Moreover, the DO-ED-JL-TFET (proposed device) exhibits a significant enhancement than the ED-JL-TFET (conventional device), attributed to the higher ON current (I_{on}) observed in the proposed device. The g_m is evaluated using the expression [18, 33].

$$g_m = \left(\frac{\delta I_{ds}}{\delta V_{gs}} \right) \tag{8}$$

The cutoff frequency (f_T) is another critical performance parameter to consider when examining the RF performance of a device. It is the frequency at which the current gain

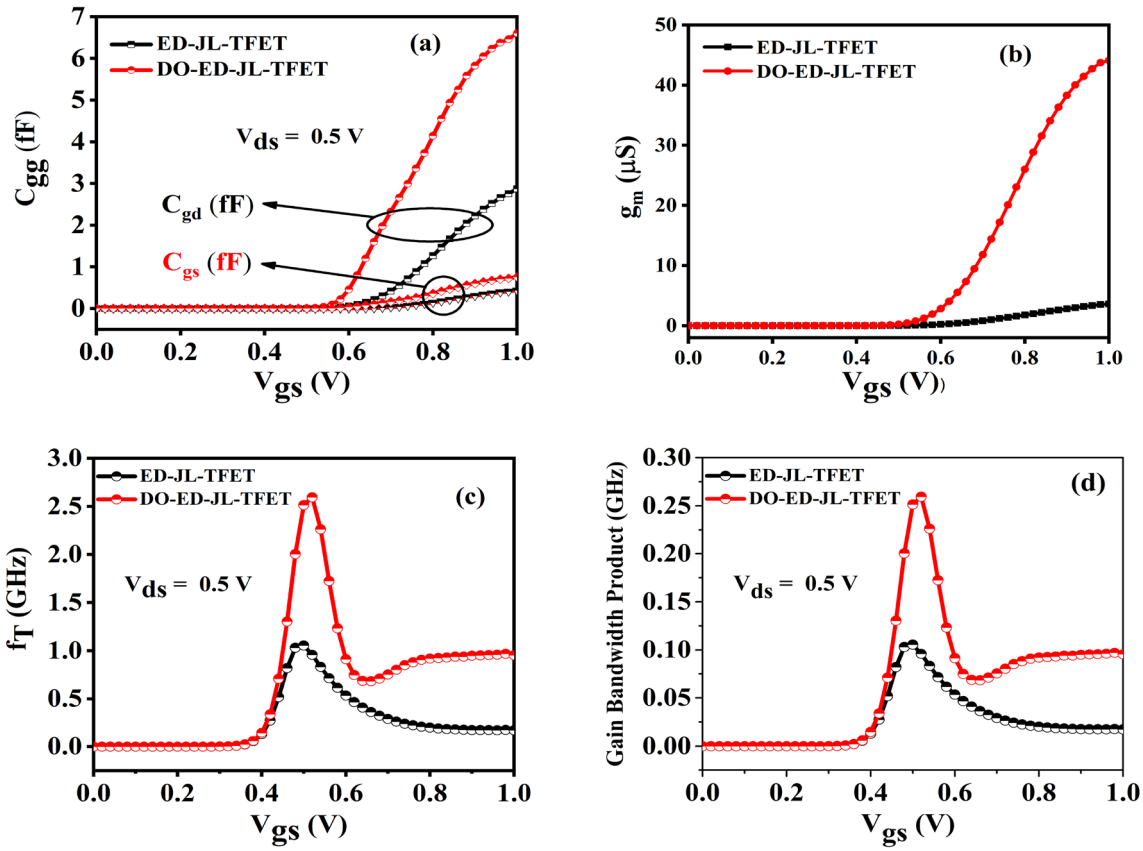

Fig. 8 Performance comparison of ED-JL-TFET and DO-ED-JL-TFET in terms of (a) C_{gg}, (b) g_m, (c) f_T and (d) GBP at gate bias 1.0 V

becomes unity and is expressed as follows [17]:

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})} \tag{9}$$

The variation of f_T with V_{gs} for both devices is illustrated in Fig. 8(c). It is evident that as V_{gs} increases f_T increases and then decreases at higher V_{gs} in both the devices due to the combined effect of the decrease in g_m due to mobility degradation and increase in parasitic capacitance (C_{gs} and C_{gd}) of the device. Moreover, the DO-ED-JL-TFET exhibits higher f_T as compared to the ED-JL-TFET, indicating the suitability of the device for RF applications. The GBP is another crucial performance metric RF performance assessment of a device. This parameter holds importance in applications demanding a balance between amplification and frequency response, including communication systems, and audio amplifiers. It is calculated by the expression [32, 33].

$$GBP = \frac{g_m}{20\pi C_{gd}} \tag{10}$$

The variation of GBP with V_{gs} for both devices is illustrated in Fig. 8(d). It is evident that as V_{gs} increases GBP increases and then decreases at higher V_{gs} in both the devices due to similar reasons as stated for f_T. Moreover, the DO-ED-JL-TFET exhibits higher GBP as compared to the ED-JL-TFET, indicating the suitability of the device for a wide frequency range.

3.5 Effect of Interface Traps Charges (ITCs)

Apart from the low ON-state current and ambipolar current issues, reliability issues arising due to the development of the ITCs at the oxide-semiconductor interface due to process variations, radiation, stress, and the impact of hot carriers are also significant issues [36–39]. Therefore, to investigate the reliability of the proposed device, the impact of donor (positive) and acceptor (negative) ITCs at the oxide semiconductor interface on the electrical performance of conventional ED-JL-TFET and the proposed and DO-ED-JL-TFET is discussed in this subsection. In the simulation setup, based on various literature, the charge density $N_f = \pm 1 \times 10^{12} cm^{-2}$ is considered for the analysis of electrical performance.

The impact of ITCs on $I_{ds} - V_{gs}$ characteristics of ED-JL-TFET and DO-ED-JL-TFET devices are shown in Fig. 9(a) and (b), respectively. It can be noted that positive (negative) ITCs increase (decrease) the I_{ds} because of the increase (decrease) in the band-to-band-tunneling rate. This

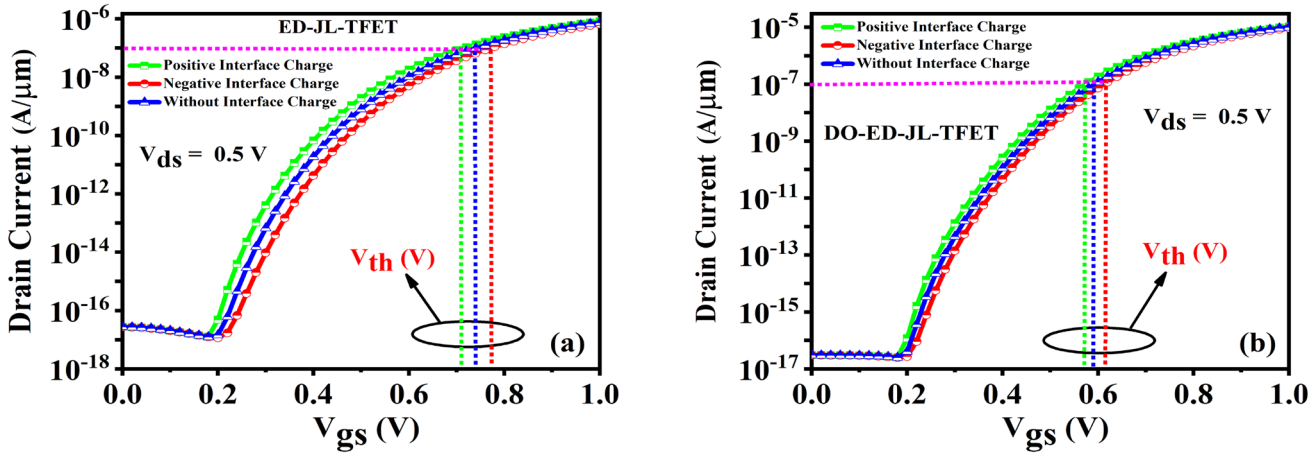

Fig. 9 Impact of ITCs on $I_{ds} - V_{gs}$ characteristics for (a) ED-JL-TFET and (b) DO-ED-JL-TFET

variation can be noted due to the dependence of V_{fb} on ITCs. The variation in V_{fb} with ITCs is given as [37]:

$$\Delta V_{fb} = \frac{qN_f}{C_{ox}} \tag{11}$$

The V_{fb} decreases for positive ITCs, due to increased effective gate bias (V_{eff}), where V_{eff} is given as: ($V_{eff} = V_{GS} - V_{fb}$). Increasing V_{eff} improves the band-to-band tunneling rate and thus increases I_{ds}, whereas negative ITCs increase the V_{fb} and decrease V_{eff}, lowering the band to band tunneling rate. As a result, the I_{ds} decreases. Moreover, increased positive (negative) ITCs significantly increase (decrease) the device performance. The increase (decrease) band-to-band tunneling rate, results in an increase (decrease) of I_{on} by 8.85% (11.8 %) and 5.94 % (6.73 %) for ED-JL-TFET and DO-ED-JL-TFET, respectively. Hence, the influence of ITCs is minimal for DO-ED-JL-TFET and is more reliable as compared to ED-JL-TFET. Figure 9(a) and (b) also illustrate the V_{th} variation with positive (negative) ITCs for ED-JL-TFET and DO-ED-JL-TFET, respectively. A lower V_{th} value is crucial for low-power applications. In this regard, the constant current method is employed to determine V_{th} from the $I_{ds} - V_{gs}$ characteristics. Moreover, due to donor (acceptor) ITCs, V_{th} experiences a decrease (increase) of 4.05% (4.32%) and 3.05% (3.73%), respectively, for DM-SGO-HTFET and DM-SGO-PD-HTFET devices. The impact of ITCs on the SS_{Avg} for the ED-JL-TFET and DO-ED-JL-TFET have been extracted from Fig.9(a) and (b). It can be noted that SS_{Avg} for both devices decreases (increases) for the positive (negative) ITCs due to a decrease (increase) in V_{th}. Moreover, due to positive (negative) ITCs, the SS_{Avg} decreases (increases) by 5.48% (2.35%), and 4.45% (3.75%), respectively, for ED-JL-TFET and DO-ED-JL-TFET.

Figure 10(a) and (b) illustrate the effect of ITCs on g_m for ED-JL-TFET and DO-ED-JL-TFET, respectively. The incorporation of dual oxide in the proposed device exhibits higher g_m as compared to a conventional device. Moreover, as compared to the ideal case (without ITC), pos-

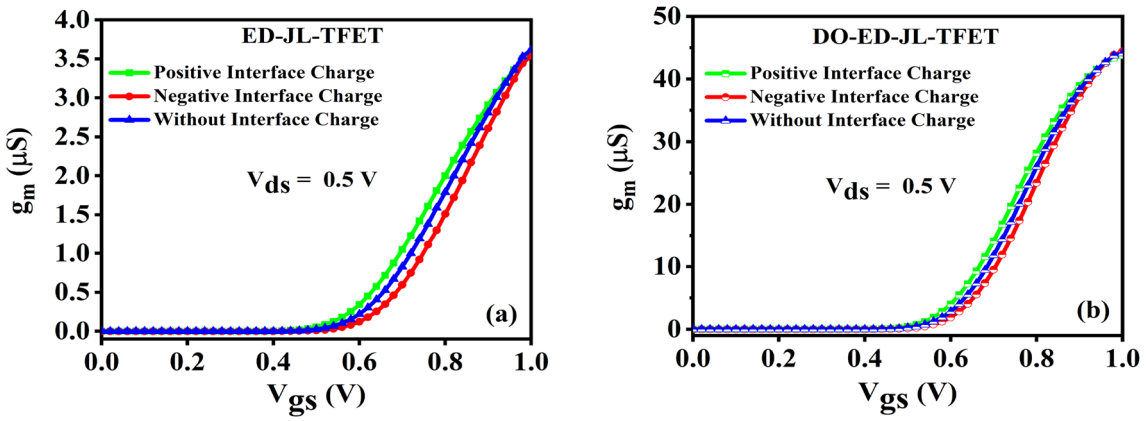

Fig. 10 Impact of interface trap charges on g_m for (a) ED-JL-TFET and (b) DO-ED-JL-TFET

itive (negative) ITCs increase (decreases) g_m by 2.14 % (6.68%) and 1.72% (2.93%) for ED-JL-TFET and DO-ED-JL-TFET, respectively. Hence, the influence of ITCs is less for DO-ED-JL-TFET and is more reliable as compared to ED-JL-TFET. The influence of parasitic capacitance (C_{gd} and C_{gs}) is generally observed in the switching speed and power consumption. C_{gs} and C_{gd} play crucial roles in evaluating the device's performance for analog/RF applications. Figure 11(a) and (b), respectively illustrate the variations in C_{gd} and C_{gs} for ED-JL-TFET and DO-ED-JL-TFET with positive (negative) ITCs at a fixed V_{ds}. Figure 11(a) illustrates the influence of ITCs on C_{gd} versus V_{gs} characteristics of ED-JL-TFET and DO-ED-JL-TFET. It is evident that as V_{gs} increases, C_{gd} increases due to a smaller potential barrier. From the Fig. 11(a), C_{gd} increases (decreases) by 1.57% (3.77%) and 0.12% (0.62%) with positive (negative) ITCs for ED-JL-TFET and DO-ED-JL-TFET, respectively. Consequently, a smaller variation in C_{gd} characteristics is observed for DO-ED-JL-TFET compared to ED-JL-TFET. Furthermore, C_{gs} Increases (decreases) by 4.09% (1.93%) and 1.09% (1.03%) with donor (acceptor) ITCs for ED-JL-TFET and DO-ED-JL-TFET, respectively. Consequently, DO-ED-JL-TFET exhibits a lesser variation in C_{gs} compared to ED-JL-TFET.

The impact of ITCs on f_T with V_{gs} for ED-JL-TFET and DO-ED-JL-TFET are shown in Fig. 11(c). It is evident that as V_{gs} increases f_T increases and then decreases at higher V_{gs} due to mobility degradation. This is due to the dependence of f_T on g_m, and the parasitic capacitance (C_{gs} and C_{gd}) of the device. Moreover, f_T increases (decreases) with positive (negative) ITCs for ED-JL-TFET and DO-ED-JL-TFET. In terms of % variation, at peak points, positive (negative) ITCs increase (decrease) f_T by 25.08% (46.33%) and 15.13% (25.02%) for ED-JL-TFET and DO-ED-JL-TFET, respectively. As a result of the incorporation of a dual oxide layer, the effect of ITCs is relatively less in the case of DO-ED-JL-TFET. Therefore, DO-ED-JL-TFET is more reliable than ED-JL-TFET. The impact of ITCs on GBP for ED-JL-TFET and DO-ED-JL-TFET is depicted in Fig. 11(d). It can be seen that positive (negative) ITCs increase (decrease) the GBP. Moreover, higher GBP has been noted for DO-ED-JL-TFET for positive ITCs up to V_{gs} =0.5V, and it starts to decrease because of g_m and C_{gd}. Also, at the peak point, GBP increased (decreased) by 25.28 % (57.09%) and 15.13% (34.88%) for the positive (negative) ITCs in ED-JL-TFET and DO-ED-JL-TFET, respectively. Therefore, the impact of ITCs is small for DO-ED-JL-TFET. Hence, DO-ED-JL-TFET is more reliable as compared to ED-JL-TFET.

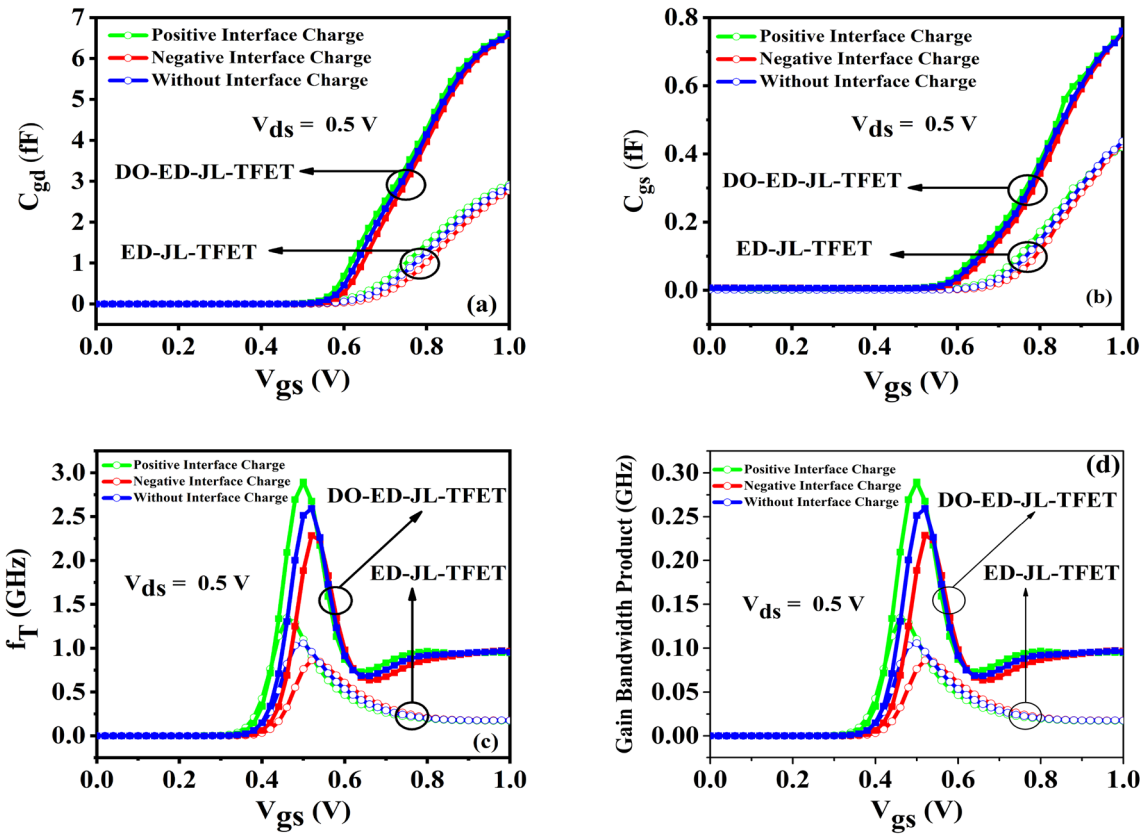

Fig. 11 Impact of ITCs on (a) C_{gd}, (b) C_{gs}, (c) f_T and (d) GBP for ED-JL-TFET and DO-ED-JL-TFET devices

3.6 Impact of ITCs on Linearity Performance

Modern communication systems require devices with low noise and high signal-to-noise ratios to achieve increased linearity while minimizing power dissipation. Non-linear devices can generate noise and distortion. ITCs have a significant impact on the linearity parameters of devices across various studies. Therefore, it is crucial to investigate the ITCs influence on the linearity parameters of devices. The small-signal model of drain current in terms of g_m and V_{gs} can be expressed as follows [40]:

$$I_{ds} = g_m V_{gs} + g_{m2} V_{gs}^2 + g_{m3} V_{gs}^3 + ... \quad (12)$$

The relationship between I_{ds} and V_{gs} of a device is expected to be linear; any deviation from linearity may introduce distortions in the output signal. To enhance linearity, g_m must remain constant over V_{gs}. However, as V_{gs} increases, I_{ds} enters a saturation region, indicating saturation in the mobility of charge carriers. Consequently, g_m decreases. To achieve a more linear device, it is necessary to reduce g_{m2} and g_{m3}, as indicated by the above equation. To address the nonlinearity problem, an examination of the linearity distortion parameters is carried out. These parameters include VIP2, VIP3, IIP3, and IMD3 which are investigated in this subsection.

Figure 12(a) and (b) show g_{m3} variation with V_{gs} and ITCs for ED-JL-TFET and DO-ED-JL-TFET, respectively. The amplitude of g_{m3} must be lower for better linearity. The peak of the g_{m3} is lower in DO-ED-JL-TFET than DO-ED-JL-TFET and also shifted towards lower V_{gs}. Furthermore, with ITCs, g_{m3} variation is minimal in DO-ED-JL-TFET, indicating better reliability than ED-JL-TFET.

The influence of ITCs on VIP2 for ED-JL-TFET and DO-ED-JL-TFET at V_{ds} = 0.5 V is shown in Fig. 12(c) and (d). To achieve better linearity, VIP2 needs to be high [34]. It is evident from the figure that VIP2 of DO-ED-JL-TFET is higher than ED-JL-TFET. Moreover, with positive (negative) ITCs, VIP2 increases (decreases). The VIP2 is obtained using the expression [41].

$$VIP2 = 4 \times \left(\frac{g_{m1}}{g_{m2}}\right) \quad (13)$$

Figure 12(e) and (f) depict the influence of the positive (negative) ITCs on VIP3 for ED-JL-TFET and DO-ED-JL-TFET, respectively. For better linearity, the amplitude of VIP3 should be large. It is evident from the figure that the amplitude of VIP3 is larger for DO-ED-JL-TFET than ED-JL-TFET. Moreover, VIP3 increases (decreases) with positive (negative) ITCs, as shown in the figure. In comparison to ED-JL-TFET, DO-ED-JL-TFET shows less variation in VIP3 (expressed as a percentage) showing better immunity to ITCs. The VIP3 is obtained using the expression [41].

$$VIP3 = \sqrt{24 \times \left(\frac{g_{m1}}{g_{m3}}\right)} \quad (14)$$

The next linearity FOM to consider is IIP3. For reliable communications systems, IIP3 peaks should be high. In this regard, Fig. 13(a) and (b) illustrates the IIP3 variation with V_{gs} for ED-JL-TFET and DO-ED-JL-TFET, respectively. The IIP3 is obtained using the expression [41].

$$IIP3 = \frac{2}{3} \times \left(\frac{g_{m1}}{g_{m3} \times R_S}\right) \quad (15)$$

IIP3 can be written in dBm as:

$$IIP3(dBm) = 10 \log_{10}(IIP3) + 10 \quad (16)$$

It can be seen that DO-ED-JL-TFET exhibits a higher IIP3, indicating the device has better linearity than the ED-JL-TFET. Moreover, the positive (negative) ITCs increase (decrease) the IIP3. Also, the impact of ITCs is lower in DM-SGO-PD-HTFET as compared to ED-JL-TFET. Thus, DO-ED-JL-TFET is more reliable as compared to ED-JL-TFET.

The IMD3 is the next linearity and distortion performance parameter to be investigated. It results from the non-linearity of $I_{ds} - V_{gs}$ characteristics. For distortion-free communication, the IMD3 parameter should be low. In this context, Fig. 13(c) and (d) show the influence of ITCs on IMD3 performance for ED-JL-TFET and DO-ED-JL-TFET, respectively. The IMD3 is obtained using the expression [41].

$$IMD3 = [\frac{9}{2} \times (VIP3)^2 \times (g_{m3})]^2 \times R_S \quad (17)$$

Here, R_S is taken as 50 Ω for most RF applications.

$$g_{m3} = \frac{\partial^3 I_{ds}}{\partial V_{gs}^3} \quad (18)$$

IMD3 can be written in dBm as:

$$IMD3(dBm) = 10 \log_{10}(IMD3) + 10 \quad (19)$$

It can be seen that in the superthreshold region, DO-ED-JL-TFET has the lowest IMD3, indicating distortionless performance. Moreover, at lower V_{gs}, IIP3 is higher than IMD3, indicating that DO-ED-JL-TFET has better linearity,

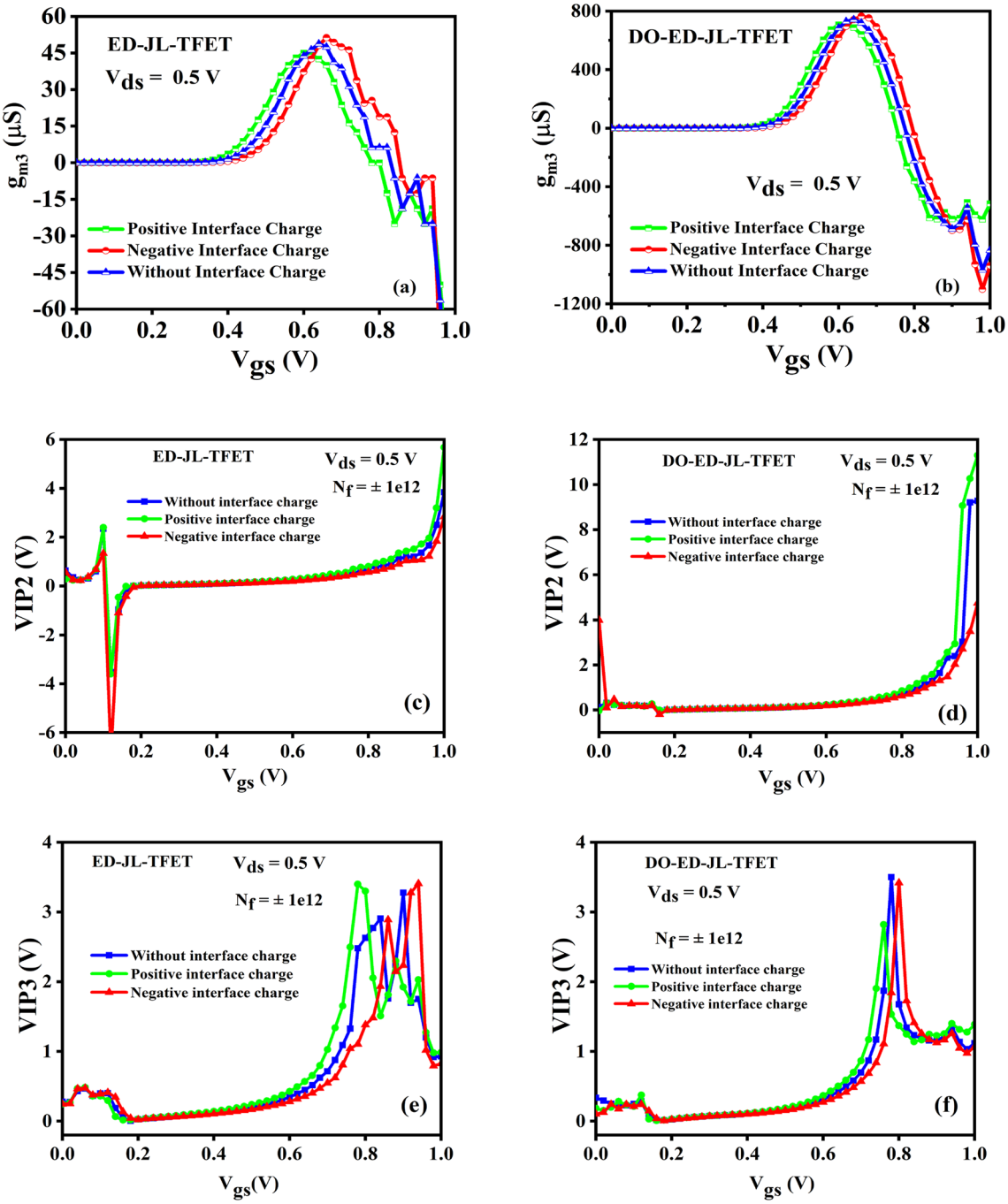

Fig. 12 Impact of ITCs on: (i) g_{m3} for (a) ED-JL-TFET and (b) DO-ED-JL-TFET, (ii) VIP2 for (c) ED-JL-TFET and (d) DO-ED-JL-TFET, (iii) VIP3 for (e) ED-JL-TFET and (f) DO-ED-JL-TFET

making the device suitable for reliable distortion-free communication systems. Furthermore, with positive (negative) ITCs, IMD3 increases (decreases) as shown in Fig. 13(c) and (d). Also, the influence of ITCs is minimal in DO-ED-JL-TFET as compared to ED-JL-TFET. Thus, DO-ED-JL-TFET is more reliable as compared to ED-JL-TFET.

4 Conclusion

The electrical performance of all actual device structures degrades as a consequence of the existence of interface trap charges. Therefore, in this manuscript, we investigate the impact of positive and negative interface trap charges (ITCs)

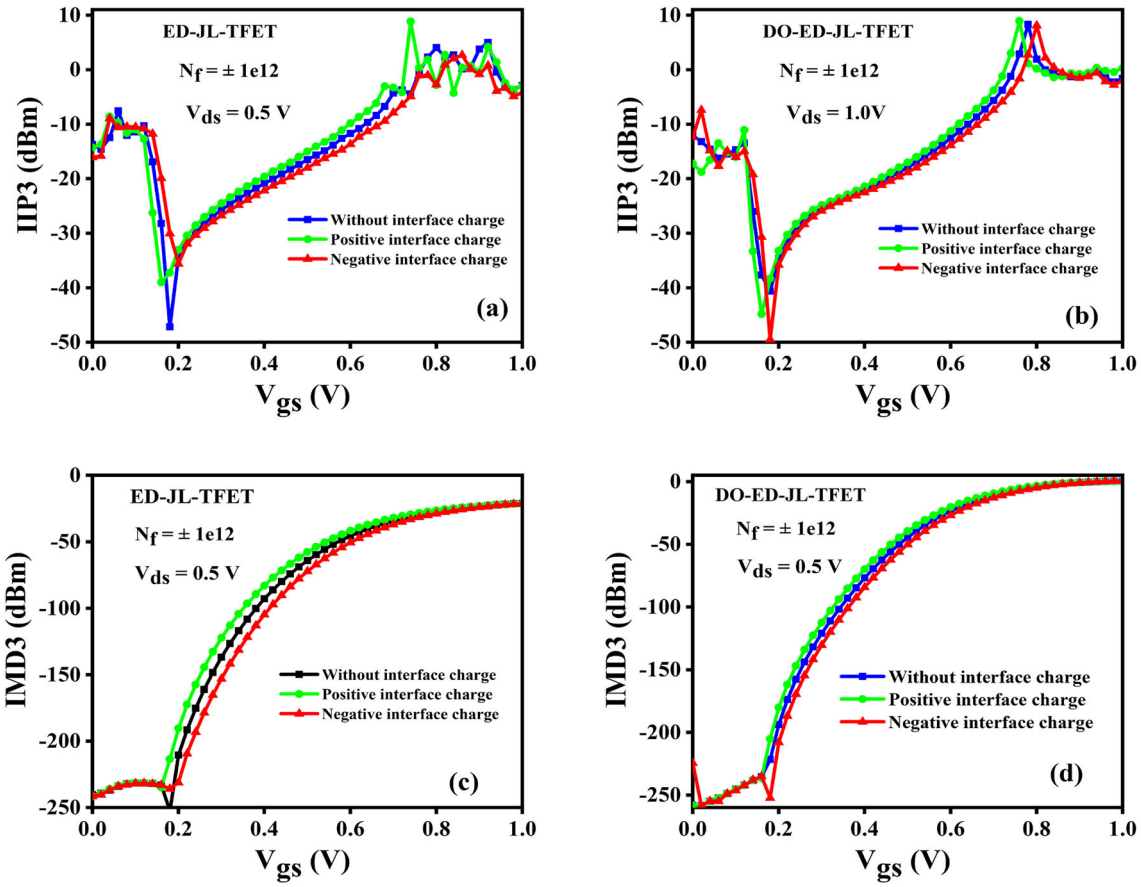

Fig. 13 Impact of ITCs on : (i) IIP3 for (a) ED-JL-TFET and (b) DO-ED-JL-TFET, (ii) IMD3 for (c) ED-JL-TFET and (d) DO-ED-JL-TFET

on the performance of the dual oxide-based electrically doped junction less TFET (DO-ED-JL-TFET) for reliability analysis, and the performance is compared with conventional ED-JL-TFET with SiO_2 gate oxide. In the proposed device, a dual oxide is employed to enhance the tunneling current and reduce the leakage current. The oxide thickness is determined using an optimization approach, where the physical oxide thickness (T_{ox}) is set at HfO_2 = 1.6 nm and SiO_2 = 0.4 nm. Additionally, various configurations of conventional devices were considered, and the proposed device demonstrated superior ON current, reaching 1.01×10^{-5} A/μm, a threshold voltage (V_{th}) of 0.75 V, and a point subthresh-

Table 3 Performance comparison of ED-JL-TFET and DO-ED-JL-TFET with positive (negative) ITCs

Parameters	Conventional ED-JL-TFET		Proposed DO-ED-JL-TFET	
Trap charges	PITC ($1x10^{12}$)	NITC ($-1x10^{12}$)	PITC ($1x10^{12}$)	NITC ($-1x10^{12}$)
I_{on}	8.85% ↑	11.80% ↓	5.94% ↑	6.73% ↓
I_{on}/I_{off}	8.46% ↑	10.83% ↓	5.59% ↑	6.12% ↓
V_{th}	4.05% ↓	4.32% ↑	3.05% ↓	3.73% ↑
SS_{Avg}	5.48% ↓	2.35% ↑	4.45% ↓	3.77% ↑
C_{gs}	4.09% ↑	1.93% ↓	1.09% ↑	1.03% ↓
C_{gd}	1.57% ↑	3.77% ↓	0.12% ↑	0.62% ↓
g_m	2.14% ↑	6.68% ↓	1.72% ↑	2.93% ↓
f_T	25.08% ↑	46.33% ↓	15.13% ↑	25.02% ↓
GBP	25.28% ↑	57.09% ↓	15.13% ↑	34.88% ↓

old slope (SS) of 20.05 mV/decade. To assess the device immunity and reliability of both devices, ITCs with trap charge density (N_f) = $\pm 1.0\times10^{12}cm^{-2}$ were introduced at the oxide semiconductor interface. The analysis reveals that the proposed device demonstrates superior immunity to various ITCs compared to conventional ED-JL-TFET to all simulated electrical characteristics as shown in Table 3. This concludes that the proposed device is showing better performance and is more reliable than the conventional device. Therefore, it can be inferred that the proposed device is a promising candidate for use in radioactive environments.

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Author Contributions
1. Bandi Venkata Chandan: Resource, Simulations, preparation of the Manuscript
2. Dharmender: Drafting and Formal Analysis
3. Kaushal Nigam: Concept and Methodology

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Availability of data and materials Data and documents pertaining to the manuscript may be made accessible upon request.

Declarations

Competing interests No Competing of interests

Ethics approval The manuscript follows all the ethical standards

Consent to participate Yes

Consent for publication Yes

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