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RESEARCH

Effect of Defects on the Switching Performance of Silicon-Gate All Around Dielectric Window Spaced-Multi-channel MOSFET

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Abstract
Investigation of the proposed Silicon gate all around dielectric window spaced-multi-channel (Si-GAA-DWS-multi-channel) MOSFET is carried out through 3D-ATLAS TCAD simulator. The proposed device parameter has been compared with the existing devices, mainly with Silicon-Nanowire-Dielectric Pocket Packed MOSFET (Si-NW-DPP FET) and Silicon-Nanowire MOSFET (Si-NW FET). The Si-GAA-DWS-Multi-channel FET is found to be the better device than the other two structures with a threshold voltage of 0.40 V, an on current of 0.326×10^{-3} A, off current of 5.9×10^{-13} A, on/off current ratio of 5.52×10^{8}, sub-threshold swing of 63.4 mV/dec and DIBL of 26.25 mV/V. Impact of interface fixed charges and multi state defects have been studied for the Si-GAA-DWS-multi-channel MOSFET. Presence of fixed negative charges and multi state defects at semiconductor-oxide interface causes a step in the potential profile which results in the shift of threshold voltage, degradation of drain current, and I_{on}/I_{off} ratio.

Keywords Defect · Trap charge · Interface defect · Dielectric Pocket Packed (DPP) · Drain Induced Barrier Lowering (DIBL) · Sub-threshold swing (SS) · MOSFET · Ultra-Large-Scale Integration (ULSI) · Multi-channel · Nanowire

1 Introduction

The field of semiconductor devices continues to evolve rapidly, driven by the relentless pursuit of smaller, faster, and more efficient electronics [1]. Metal–Oxide–Semiconductor Field-Effect Transistors (MOSFETs) play a central role in modern integrated circuits, and understanding their behavior and limitations is crucial for further advancements [1–3]. The occurrence of short-channel effects (SCEs) in MOSFET, such as the reduction in threshold voltage, substrate bias force, current drivability and reliability, is observed as the dimensions of a device starts to scale down. To address the limitations and improve the performance of CMOS technology, researchers are currently investigating innovative device configurations such as double-gate MOS and surround-gate MOS, as well as novel materials like strained Si, GaAs, high-k gate dielectric, and metallic gate electrodes [4–7]. Nanowire gate-all-around (GAA) metal–oxide–semiconductor field-effect transistors (MOSFETs) when compared to planar transistors exhibit superior gate control [6]. Therefore, most of the research is now focused on it. Though nanowire MOSFET is the leader in present CMOS technology, the current driving capability of the device can be improved by introducing an array of nanowires which resembles to the small forest with tall trees. Due to the cylindrical structure, the potential is developed in the surface for thicker channel, however, in multiple channels, as the channel thickness is thin, so it will be throughout the body. As multiple numbers of channels are there, so the total current will be the sum of the individual channel drain current. So upon introduction of multiple channels in the channel region of the device, the amount of charge carriers flowing from source towards drain increases as each individual Si channel contributes to the total conductance of the multiple channel FETs. So, it results in improving the electrical characteristics of the device [8–10].

The exploration of charge transfer and interface effects in advanced devices has garnered increasing interest within the field of physics. As electronic devices continue to shrink in

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size, the behavior of charges at material interface becomes increasingly significant. Understanding how charges traverse these interfaces and how it impacts the device performance is crucial to improve device design and functionality. However, very few research papers shed light on various aspects of MOSFET performance, including charge trapping phenomena, interface charge traps, interface fixed charges, oxide charge trapping, surface and edge defects, etc. [11, 12]. Charge trapping phenomena in MOSFETs have gained considerable attention due to their impact on device operation and reliability. From noise-induced fluctuations to bias temperature instability, understanding and mitigating these trapping effects is vital for ensuring consistent device performance. Researchers have explored the underlying mechanisms of charge trapping and have developed models to accurately predict and simulate these phenomena, enabling the optimization of MOSFET designs [11–15]. The investigation of oxide charge trapping and detrapping in MOSFETs using the Gate-Induced Drain Leakage (GIDL) current technique is another important research area [11]. This technique enables the study of oxide charge trapping dynamics, shedding light on the behavior of charge traps in the oxide layer and their influence on device characteristics. Understanding these trapping mechanisms helps in devising strategies to improve device performance and reliability.

In this article a multi-channel surrounding gate MOSFET is developed to examine how charge transfer and interface effects potentially impact the performance of the proposed device. The device is modeled using Silvaco ATLAS 3D bundle. Interface trap simulation includes both fixed positive, negative, uniform interface and multi traps. The recombination process and generation of semiconductors are accounted for by the Shockley–Read–Hall (SRH), trap state recombination. Also models like band narrowing, field mobility and the velocity saturating model are considered for carrier movement and saturation. Furthermore, the quantum density distribution model and the drift–diffusion model incorporate carrier transport, taking into account quantum correction effects. This study investigates various trap models, and their implications to gain insights into the influence of interface traps on the performance of Silicon Gate-All-Around Dielectric Window Spaced-Multi-channel (Si-GAA-DWS-multi-channel). The obtained results are also compared with a base Silicon-Nanowire-Dielectric Pocket Packed MOSFET (Si-NW-DPP FET) and Silicon-Nanowire MOSFET (Si-NW FET) to prove it's superiority.

2 Device Structure

The proposed Si-GAA-DWS-multi-channel FET device is shown in Fig. 1. The structure comprises of an outer metal layer known as gate. Below the gate region there is a dielectric layer consisting of SiO_2. Generally we call it as the oxide layer in case of MOSFET. The central part of the structure consists of a silicon channel which is terminated by the dielectric (Si_3N_4) window on both sides. The channel thickness is 10 nm, so along with the central channel there are 8 more silicon channels which surround the central channel. On the extreme ends of the channel there are source and drain embankments. These source and drain surfaces are surrounded by the spacers made of dielectric material (Al_2O_3). The metal contacts which are used to surround the gate, source and drain regions acts as gate, source and drain electrodes respectively. The gate electrode is having a work-function of 4.7 eV. A gate-source voltage (V_{GS}) of 1 V and a drain-source voltage of 1 V is

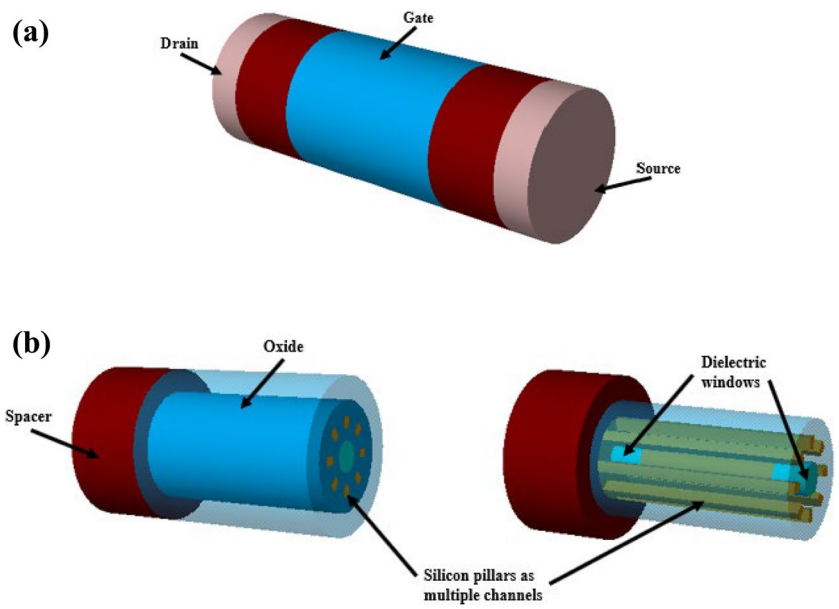

Fig. 1 **a** 3D-Schematic of Si-GAA-DWS-Multi-channel FET. **b** Internal architecture of Si-GAA-DWS-Multi-channel FET

Table 1 Physical parameter dimensions for Si-GAA-DWS-Multi-channel MOSFET

S.no	Parameter	Symbol	Value
1	Channel length	L_g	20 nm
2	Drain/ Source doping	N_D	10^{20} atoms/cm^3
3	Channel doping	N_A	10^{15} atoms/cm^3
4	Oxide thickness	t_{ox}	2 nm
5	Channel thickness	t_{si}	10 nm
6	Dielectric pocket length	DP_L	4 nm
7	Dielectric pocket thickness	DP_T	4 nm
8	Spacer length	L_{sp}	10 nm
9	Source/ Drain contact length	L_{SC} /L_{DC}	10 nm
10	Gate-Source voltage	V_{GS}	1 V
11	Drain-Source voltage	V_{DS}	1 V
12	Silicon pillars thickness	$t_{si\text{-}p}$	0.35 nm (surrounding pillars) 2 nm (central pillar)

considered for biasing the device in the active region of operation. Structure's physical dimension and thermal parameters are listed in Table 1. The SILVACO ATLAS 3D TCAD is utilized for the simulation and calibration of Si-GAA-DWS-multi-channel FET. The modeling of proposed nanotube structures incorporates the quantum confinement model along with the drift diffusion model. Mainly Bohm Quantum Potential is considered for the quantum effect as the multiple channels' individual thickness is less than 10 nm. For details regarding Bohm Quantum Potential ATLAS user manual can be referred. As NMOS is designed so the n type quantum models are taken for simulation purpose. The model introduces a position dependent quantum potential, Q, which is added to the Potential Energy of a given carrier type. This quantum potential is derived using the Bohm interpretation of quantum mechanics and takes the following form

$$Q = \frac{-h^2}{2}\frac{\gamma \overset{\nabla}{\rightarrow} (M^{-1} \overset{\nabla}{\rightarrow} (n^{\alpha}))}{n^{\alpha}} \tag{1}$$

where α and γ are two adjustable parameters, M^{-1} is the inverse effective mass tensor and n is the electron (or hole) density.

This will now affect Poisson's equation using the charge density terms as follows.

$$n = N_C \exp\left(-\frac{(E_C + qQ)}{kT_L}\right) \tag{2}$$

$$p = N_V \exp\left(-\frac{(qQ - E_V)}{kT_L}\right) \tag{3}$$

Additionally, carrier mobility is influenced by the electric field and carrier concentration in the device, with the activation of CONMOB and FLDMOB models. The modeling approach utilizes Fermi–Dirac statistics with the Boltzmann approximation for band structures. Recombination processes in the semiconductor are accounted for through the Shockley–Read–Hall and Auger models, including considerations for lattice heating and carrier energy exchange. Considering the required device models, its calibration has been performed as per the experimental results and shown in Fig. 2 [16].

3 Result and Discussions

Table 2 and Fig. 3 represents important FOM of the proposed device along with other standard Si-NW FET, Si-NW-DPP FET devices. Proposed Si-GAA-DWS-multi-channel FET shows superior FOM as compared to others. Si-NW-DPP FET shows better off current as compared to basic Si-NW FET due to the presence of Dielectric Pocket Packed (DPP) in the source and drain channel interface [17, 18]. Whereas a sharp increase in both on and off current is noticed for Si-GAA-DWS-multi-channel FET. The off current improvement is due to dielectric pockets, whereas the multiple channels help in improvement in on current [19–26]. It can also be concluded from surface potential graph shown in Fig. 4 (as it is well known that minimum the potential maximum is the current). As both the on and off are better, so it shows better figure of merits compared to the other two structure provided in Table 2.

In MOS devices, the interface at the drain side is exposed to strongest electric field. This high field generates hot carriers, which crafts permanent damage in the device [27]. Equally, radiation, stress induced damages results in interface traps near the gate oxide-Si channel interface [27]. This

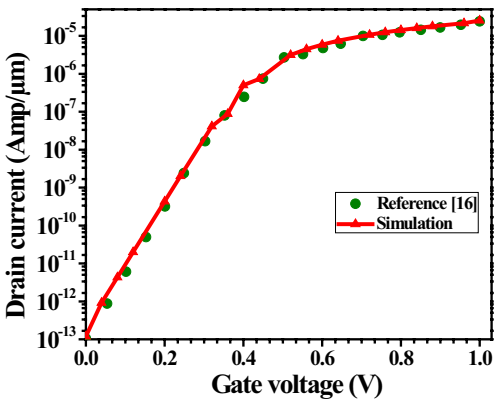

Fig. 2 Validation of simulation results with experimental data [16] for a GAA MOSFET (L = 28 nm, R = 5 nm, and tox = 2 nm)

Table 2 Comparison of Figure of Merits (FOM) of Si-NW FET, Si-NW-DPP FET and Si-GAA-DWS-multi-channel FET

	V_{th} (V)	I_{on} (A)	I_{off} (A)	I_{on}/I_{off}	SS (mV/dec)	DIBL (mV/V)
Si-NW FET	0.364	2.68×10^{-5}	1.35×10^{-11}	1.98×10^{6}	70.814	55.20
Si-NW-DPP FET	0.377	2.32×10^{-5}	4.5×10^{-12}	5.16×10^{6}	66.841	43.36
Si-GAA-DWS-multi-channel FET	0.40	0.326×10^{-3}	5.9×10^{-13}	5.52×10^{8}	63.4	26.25

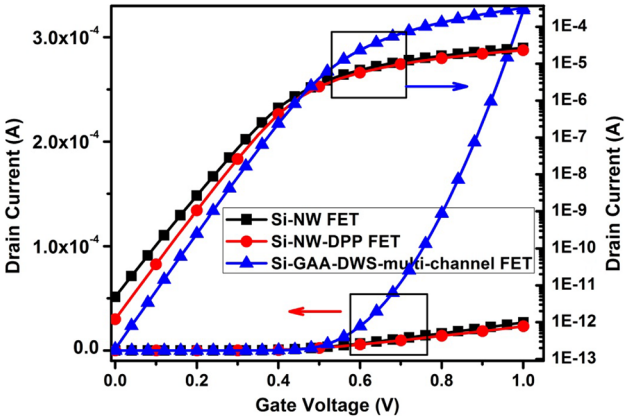

Fig. 3 Comparison of I_d Vs. V_{gs} for different MOSFETs in ideal condition

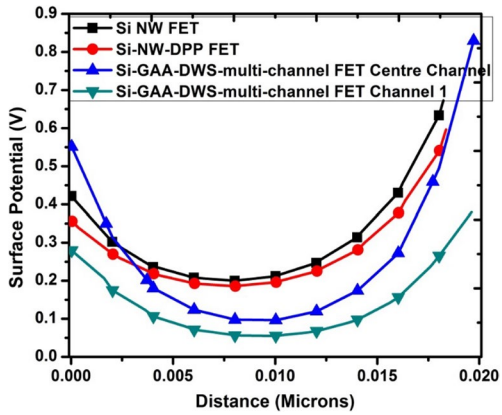

Fig. 4 Comparison of surface potential for different MOSFETs in ideal condition

traps near Si-oxide interface, also accepts an electron, if the trap level is located underneath the fermi level. Such case is known as a fixed negative charge. Likewise in case of donor type interface trap, it is known as fixed positive interface charge. So, interface traps can be transformed into equivalent interface fixed charges. The presence of these defect centers, or traps, in semiconductor substrates may significantly influence the electrical characteristics of the device. Trap centers, whose associated energy lies in a forbidden gap, exchange charge with the conduction and valence bands through the emission and capture of electrons. The trap centers influence the density of space charge in semiconductor bulk and the recombination statistics. Interface fixed charge is modeled as a sheet of charge at the interface and therefore is controlled by the interface boundary condition. Trap charges can also be modeled as interface trap states and bulk trap states. Interface traps and bulk traps will add space charge directly into the right hand side of Poisson's equation. It is possible to model traps that have two or more internal states by using the multi-state trap model. This allows you to model structural changes of a trap as well as trapping of multiple carrier types and ionic or atomic species [28]. So for further discussion on the effect of trap charges on the proposed device, three types of charges will be considered such as positive fixed charge, negative fixed charge, and multi-level trap charge.

Table 2, Figs. 3 and 4 concludes that proposed Si-GAA-DWS-multi-channel FET is superior as compared to Si-NW-DPP FET and basic Si-NW FET. From here onwards the effect of different trap charges are carried out only on proposed Si-GAA-DWS-multi-channel FET.

Table 3 compares different FOM of Si-GAA-DWS-multi-channel FET with varying trap charge conditions.

From Table 3 it can be seen that positive fixed charge has very minimum effect on the device FOM, whereas negative fixed charge has bad impact on the device characteristics. As the negative fixed charge goes on increasing the subthreshold slope (SS) and threshold voltage (V_{th}) goes on increasing. At the same time on current also deteriorates, which reduces the I_{on}/I_{off} ratio. Similarly, in multi trap states two different cases are considered having donor, acceptor and donor concentration $2\times10^{12}/cm^2$, $1\times10^{11}/cm^2$, $1\times10^{11}/cm^2$ as case 1, and $8\times10^{12}/cm^2$, $1\times10^{12}/cm^2$, $5\times10^{11}/cm^2$ as case 2 respectively. Here it can also be seen that the SS, I_{on} and V_{th} are also reducing. For better visualization the I_{ds} Vs V_{gs} curve is presented in Fig. 5. And to support it the surface potential curve is also given in Figs. 6 and 7.

Thus surface potential is lowered (raised) in case of negative (positive) interface fixed charges in the channel region (see Figs. 6 and 7 for both center and side channels). As a result from Fig. 5 it is visualized that the changes in magnitude of on currents respectively (Also see Table 3). But while coming towards the off current it happens due to the interface trap charge and trap state recombination. Figures 8, 9 and 10 shows the contour plot of interface trap charge and

Table 3 Comparison of different FOM of Si-GAA-DWS-multi-channel FET with variable trap charges

FOM	Fixed positive charge			Fixed negative charge			Multi Trap States	
	1×10^{10}/cm^2	1×10^{11}/cm^2	1×10^{12}/cm^2	1×10^{10}/cm^2	1×10^{11}/cm^2	1×10^{12}/cm^2	CASE-1	CASE-2
SS(mV/dec)	63.4	63.61	63.92	64.1	66.1	81.2	65.29	70.001
V_{th}(V)	0.404	0.404	0.395	0.407	0.524	0.94	0.421	0.551
I_{on}(A)	0.326×10^{-3}	0.327×10^{-3}	0.338×10^{-3}	0.322×10^{-3}	0.213×10^{-3}	1.12×10^{-6}	0.309×10^{-3}	0.189×10^{-3}
I_{off}(A)	5.96×10^{-13}	6.16×10^{-13}	8.52×10^{-13}	5.7×10^{-13}	2.34×10^{-13}	6.78×10^{-14}	5.7×10^{-13}	4.24×10^{-13}
I_{on}/I_{off}	5.46×10^{8}	5.3×10^{8}	3.96×10^{8}	5.66×10^{8}	9.07×10^{8}	1.65×10^{7}	5.43×10^{8}	4.47×10^{8}

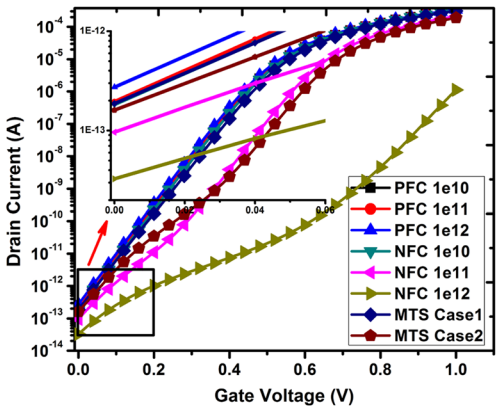

Fig. 5 I_{ds} Vs. V_{gs} of Si-GAA-DWS-multi-channel FET with variable trap charges

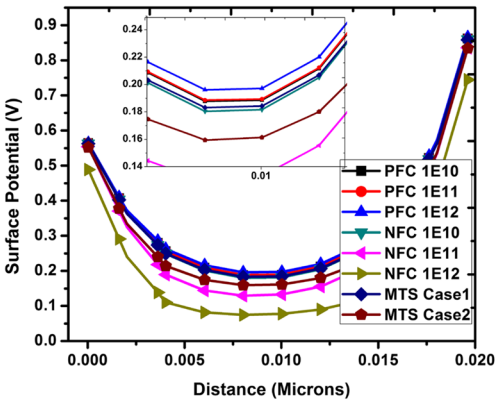

Fig. 7 Surface potential of Si-GAA-DWS-multi-channel FET with variable trap charges for center channel

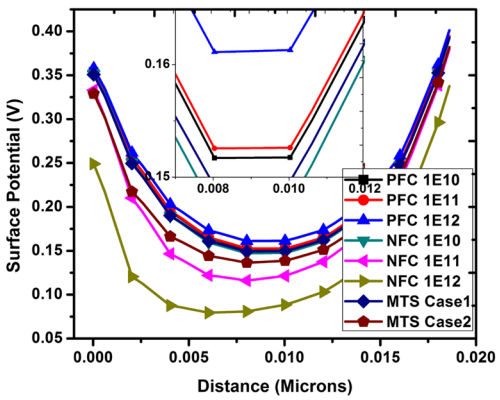

Fig. 6 Surface potential of Si-GAA-DWS-multi-channel FET with variable trap charges for channel number 1 out of 8 channels

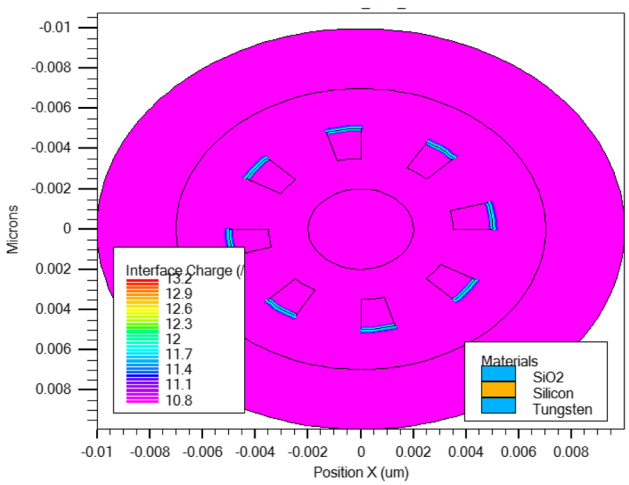

Fig. 8 Interface trap charges in Si-GAA-DWS-multi-channel FET for NFC of 1×10^{12} /cm^2

trap state recombination for negative fixed charge of concentration 1×10^{12} /cm^2.

Also positive (negative) fixed charges provides screening to the undamaged region from the higher drain to source bias (Vds) effects in case of fixed charges are present near the drain (source) side. Thus minimum surface potential and its position changes and induces a shift in the threshold voltage [27]. The changes in surface potential due to fixed charges depend on the oxide properties (relative permittivity and thickness) and the density of fixed charges.

The presence of interface trap charges can lead to several issues that contribute to an increase in the off-state current: such as barrier lowering and threshold voltage shifting (See Table 3). Interface traps introduce energy levels within the

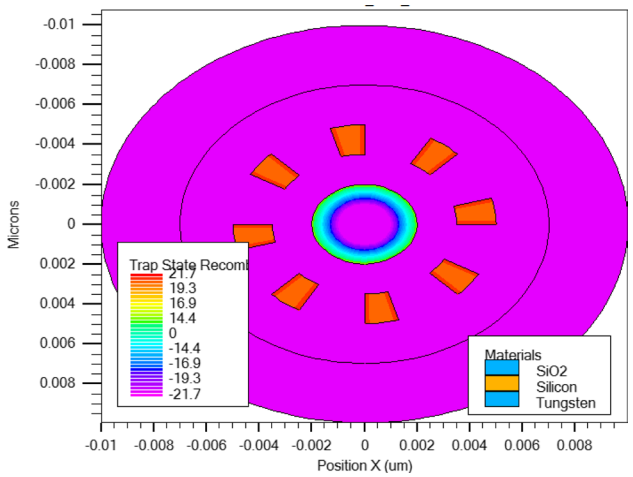

Fig. 9 Trap state recombination in Si-GAA-DWS-multi-channel FET for NFC of 1×10^{12} /cm^2

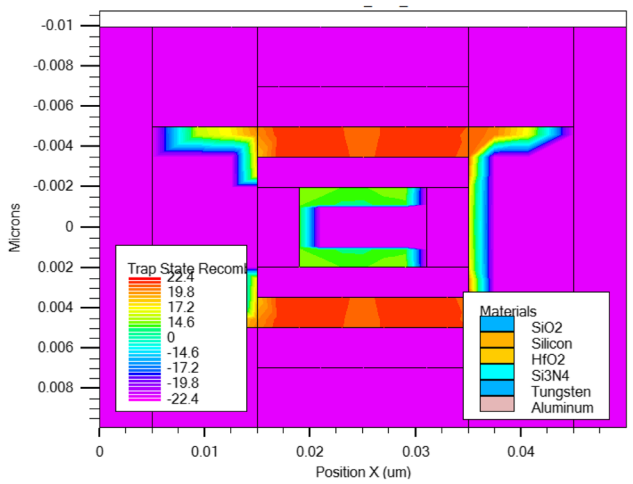

Fig. 10 2D cut section view of trap state recombination in Si-GAA-DWS-multi-channel FET for NFC of 1×10^{12} /cm^2

bandgap of the semiconductor material, that creates localized states. These states act as additional energy barriers or traps for charge carriers. As a result, the effective barrier for carriers to move across the semiconductor material is lowered, making it easier for electrons to tunnel through the barrier even when the transistor is supposed to be in the off state. So it reduces the off current further. It can be visualized from Fig. 8 that the interface trap is very high near multi-channel and oxide interfaces. As a result the off current deteriorates (see Table 3). Similarly, Interface trap charges can lead to a shift in the threshold voltage (V_{th}) of the MOSFET. The threshold voltage is the gate-source voltage at which the transistor switches from the off state to the on state. When interface traps are present, it can capture or release charge carriers, causing a shift in the threshold voltage. A higher threshold voltage can result in an increase in the off-state current. It can be seen from Figs. 9 and 10 that the recombination is very high near the oxide and Si surface. So the off current deteriorates rapidly (can be seen from Table 3 NFC case).

4 Conclusion

The electrical effects of different trap induced defects in MOSFETs are examined. The 3-D simulation results suggest that NFC and multi state defects are the potential source of variability in FOM in NW transistors. The threshold voltage (0.94 V) and SS (81.2 mV/dec) increase for the NFC and multi state defect at Si-oxide interface. The defect-induced leakage is the highest (6.78×10^{-14} A) in NFC, and depends on the charge concentration. In addition, simulation results show that the PFC has a small effect in Si-GAA-DWS-multi-channel FET in terms of both threshold voltage shift and leakage current. This is due to the well-controlled electrostatics in Si-GAA-DWS-multi-channel FET.

Authors' Contributions Dr. Girija Shankar Sahoo conceived and designed the simulation and written the manuscript; Ushodaya A performed the simulation study and generated the output; Dr. Girija Shankar Sahoo, and Dr. G P Mishra modified the manuscript and analyzed the data; Dr. Guru Prasad Mishra contributed by providing the Silvaco tool; all authors reviewed the entire manuscript.

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Data Availability The article submitted is an original work and has neither been published in any other peer-reviewed journal nor is under consideration for publication by any other journal.

Declarations

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b) On submission of the manuscript, the authors agree not to withdraw the manuscript at any stage prior to publication.

Competing Interests The authors declare no competing interests.

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