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RESEARCH

Electrical Performance of the Side Region in a Multi-crystalline Silicon Ingot

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Abstract
This paper investigates the impact of low minority carrier lifetime areas (red-zones) in multi-crystalline silicon ingots on cell efficiency. Wafers, sliced parallel to the sidewall, were analyzed using μ-PCD and PL to determine minority lifetimes and identify crystal defects. These wafers were then processed into solar cells, and their performance was assessed through cell conversion efficiency and electroluminescence (EL) measurements. The findings reveal a decrease in minority lifetime moving from the wall inward, followed by an increase beyond approximately 14 mm. This pattern is mirrored in cell efficiency. Notably, in regions where the minority lifetime is less than 1μs, cell efficiency drastically drops, and shunting areas are visible in EL images. Conversely, in areas with lifetimes exceeding 1μs, cell efficiency returns to normal levels. These results provide guidelines for optimally cropping the sides of the ingot.

Keywords Multi-crystalline silicon · Minority carrier lifetime · Cell conversion efficiency

1 Introduction

In the midst of escalating concerns regarding energy scarcity and environmental pollution, the photovoltaic industry has witnessed rapid global growth, driven by the abundance of green energy resources. Simultaneously, multi-crystalline silicon has emerged as the primary material in the solar industry due to its abundant raw material availability, modest purity requirements, high production efficiency, and capacity for large-scale manufacturing.

As technology in the photovoltaic industry continues to advance, there has been a notable improvement in multi-crystalline silicon cell efficiency. Simultaneously, solar cell manufacturers have raised their quality standards. Of particular concern among these standards is the issue of black edges in solar cells, which is attributed to the presence of the red-zone in silicon wafers and has garnered significant attention from manufacturers.

Low minority carrier lifetime areas are present in both the top and bottom sections of the multi-crystalline silicon ingot. As indicated by research [1], low cell efficiency is predominantly observed within the red zone. Presently, the practice involves employing minority lifetime testing and control during the cutting of silicon bricks for the top and bottom of the ingot. However, there is a scarcity of research reports addressing the impact of low minority carrier lifetime (red-zone) at the edge of multi-crystalline silicon ingots on solar cell efficiency. With the continuous improvement of solar cell technology, the influence of the silicon wafer red-zone on solar cell performance has become more pronounced. Consequently, the examination of the red-zone's effect on electrical performance in this study holds increasing importance and promises to offer valuable theoretical insights for crystal growth technology.

2 Experimental Methods

This experiment utilized a G5 (5 × 5 silicon brick) polycrystalline silicon ingot, processed via directional solidification growth. The ingot was squared by slightly adjusting

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the wire either left or right of the center, selecting a silicon brick near the crucible, which resulted in a brick with a large red zone. A 2μs minority lifetime threshold was then applied to remove the top and bottom of the silicon brick. Subsequently, a segment 156 mm above the bottom was cut to obtain a 156 × 156 mm cubic silicon brick. Its minority lifetime was scanned, the red zone's location marked, and it was sliced in alignment with the crystal growth direction. The red zone portion was kept parallel to the cutting surface, yielding silicon wafers containing the entire red zone, as illustrated in Fig. 1.

The silicon wafers were sorted, and every tenth wafer underwent testing for minority lifetime and photoluminescence (PL). These wafers were then processed into solar cells using the conventional screen-printing method, after which key parameters, including cell efficiency and leakage current, were assessed.

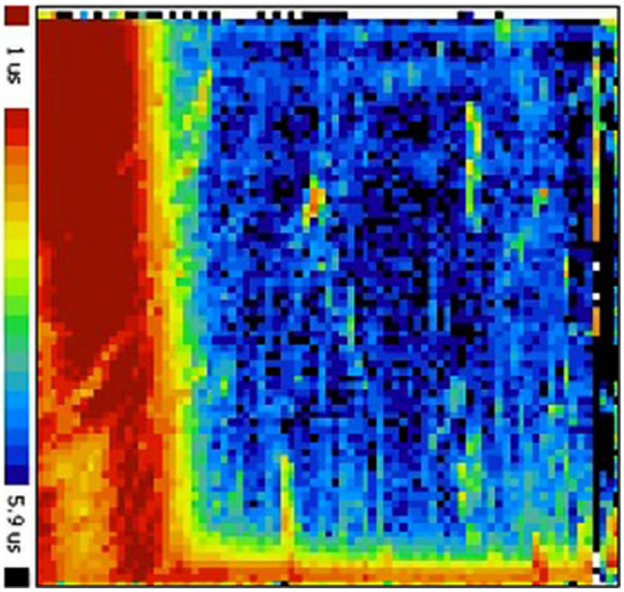

Fig. 2 Lifetime profile image of the squared

3 Results and Discussions

3.1 Inspection Result of Minority Life

Figure 2 presents the minority lifetime measurement results for a 156*156 mm cubic silicon brick, conducted using μ-PCD. Notably, there is a red edge zone, characterized by a minority lifetime of less than 2μs, located on one side of the silicon block. The width of the silicon brick's 100% red zone measures 32 mm. The slicing process utilizes a guide wheel with a slot distance of 350 μm, which theoretically yields 91 pieces of silicon wafers.

3.2 Wafer Minority Lifetime and PL Test Results

As depicted in Fig. 3, (a) represents the minority lifetime graph of the 1st, 30th, 60th, and 100th pieces of silicon wafers, counted starting from the red zone near the crucible, while (b) corresponds to the corresponding PL image.

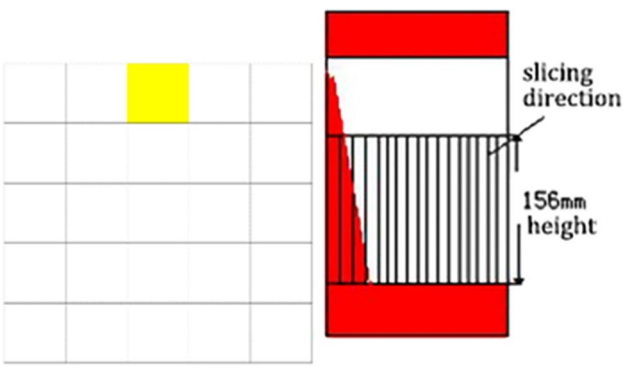

Fig. 1 Selection of silicon brick and wafer slicing

An observation from these two images reveals that the red zone in the minority lifetime graph aligns successively with the dark zone in the PL diagram. Additionally, the PL image indicates that the red zone in the silicon wafer primarily consists of impurity defects, resulting from the solid-phase diffusion of transition metal impurities such as Fe_i from the crucible coating into the silicon ingot [2, 3]. This phenomenon has also been corroborated by MD Pickett et al. [4]. In contrast, the low minority lifetime region within the non-red zone corresponds to filamentous black features in the PL image, which are predominantly crystal defects. T Trupke et al. [5] have reported similar findings. Comparing the PL images from the red and non-red zones reveals distinct differences in the crystal structure of wafers near the crucible compared to those in the non-red zone. Furthermore, the growth cross-section of the silicon ingot demonstrates that the crystal morphology near the crucible is influenced by the crystal growth on the sides.

3.3 Efficiency and Irev2 Results

To examine the impact of silicon wafers from the red zone on solar cells, these wafers were processed into solar cells and then subjected to efficiency distribution and leakage current (Irev2) measurements. As depicted in Fig. 4, the efficiency initially decreases, then increases, and finally stabilizes, moving away from the crucible wall. Irev2 similarly shows an initial decrease before stabilizing. Notably, Irev2 in the red zone is approximately six times higher than in the non-red zone. This suggests that the high

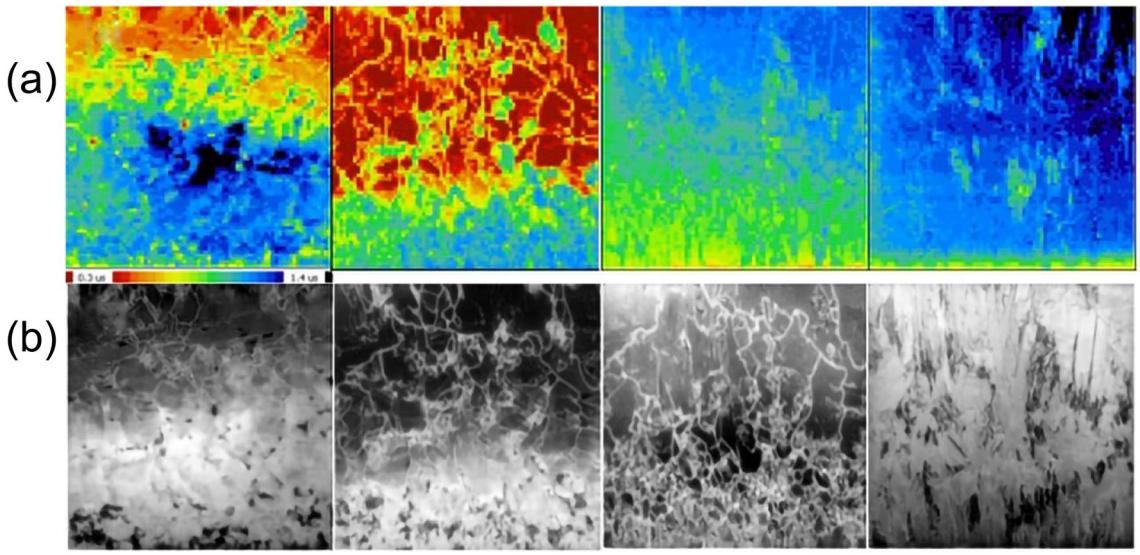

Fig. 3 Silicon wafer lifetime profile images & Silicon wafer PL profile images

concentration of metal impurities in the red zone is not fully mitigated during the cell production process. Consequently, this leads to the excessive accumulation of metal impurity and the creation of leakage pathways, resulting in elevated leakage currents.

The correlation between the minority lifetime of silicon wafers in the red zone and their cell efficiency was analyzed. Figure 5 illustrates that the trends in cell efficiency and minority lifetime are consistent. It was observed that a minority lifetime of 1μs in red zone wafers correlates with a cell efficiency of 16.5%. Above this threshold, the impact on efficiency and Irev2 markedly diminishes. Below 1μs, the influence of metal impurities on efficiency and leakage current intensifies. Given the ingot's 16 mm cut width, the maximum distance between the red zone and the crucible wall is estimated to be about 48 mm. The efficiency impact of the red zone significantly decreases beyond 12 mm from the non-red zone, where efficiency returns to normal. The variation in minority lifetime within the red zone, in conjunction with the data in Fig. 2, reveals a slightly elevated minority lifetime layer near the bottom edge, with half a wave peak remaining due to edge skin removal. This formation of an interlayer is possibly explained by excessive oxygen concentration in the area [6, 7], leading to oxygen precipitation. This acts as an impurity trap for Fe_i, reducing overall electrical activity and causing a minor increase in minority lifetime.

Data above-mentioned indicated that the red zone has a great impact on cell efficiency and leakage current. In mass production, as the slicing direction of silicon wafer is perpendicular to the direction of crystal growth, and the red zone circling the entire silicon wafer will not exist. In order to verify the effect of the red zone on the efficiency and leakage current in mass production, the adjacent silicon bricks

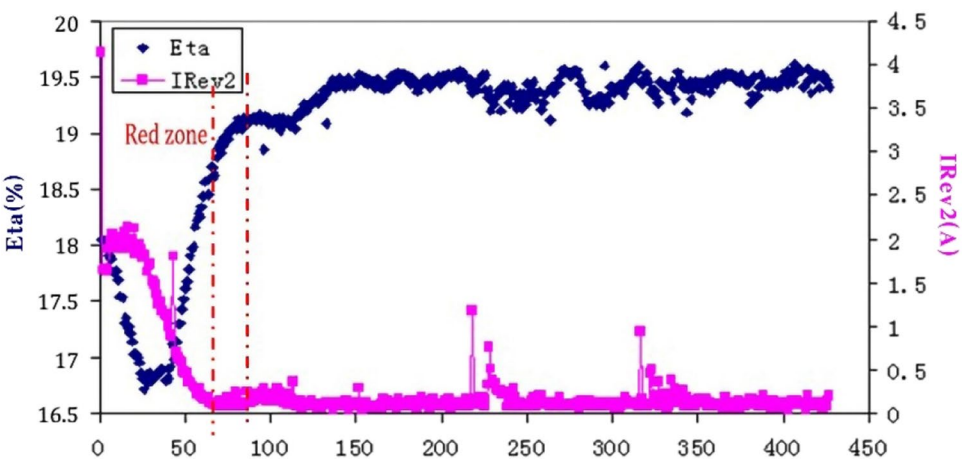

Fig. 4 Distribution of Eta and Irev2 of sorted wafers

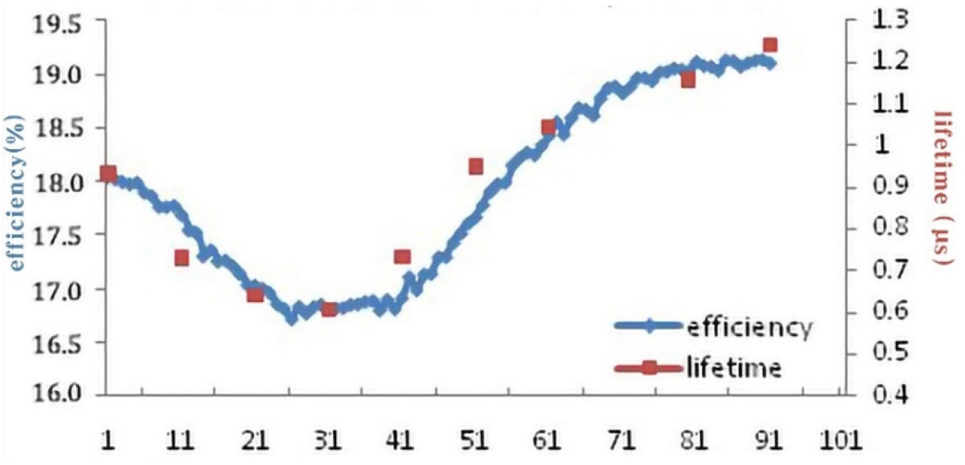

Fig. 5 Wafers lifetime and cells efficiency in red zone

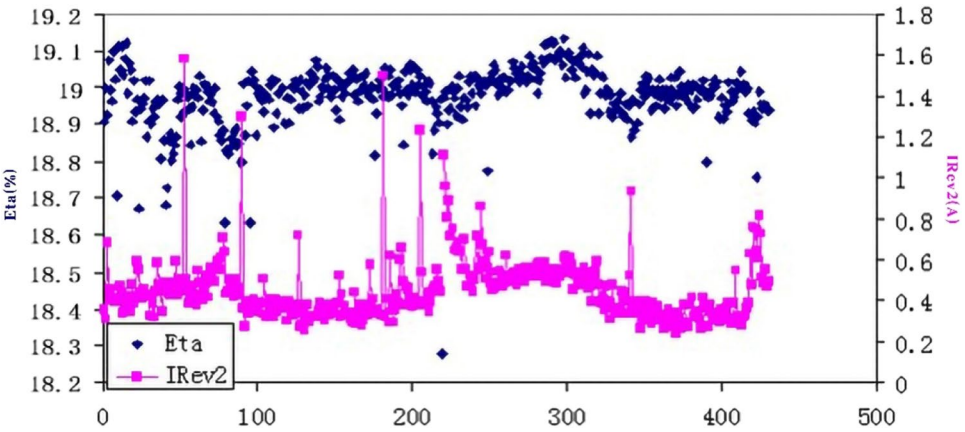

Fig. 6 Distribution of Eta and Irev2 of sorting cells from adjacent bricks

with the same width of red zone are selected for conventional slicing and made into solar cells. As shown in Fig. 6, both the cell efficiency and Irev2 are stable. The electroluminescence (EL) test shows that some cells have black edges, as shown in Fig. 7, indicating that the red zones can be improved by impurity absorption of solar cells production process.

Table 1 compares the efficiency of vertical-cut silicon wafers in both the red and non-red zones with conventionally-cut adjacent silicon bricks. The efficiency of vertically-cut wafers in the red zone is 1.5% lower than in the non-red zone. Florian Schindler et al. [8] have similarly explored the red zone's impact on efficiency, deriving theoretical calculations that align closely with the findings of this study. The deviation in cell efficiency between conventional and vertical cutting methods for silicon wafers is minor, suggesting that the discrepancy may be attributed to the number of wafers and variables in cell production; this is considered a normal variance by the author. However, it is noteworthy that the efficiency of conventionally sliced wafers in the non-red zone is approximately 0.4% lower than that of vertically-cut

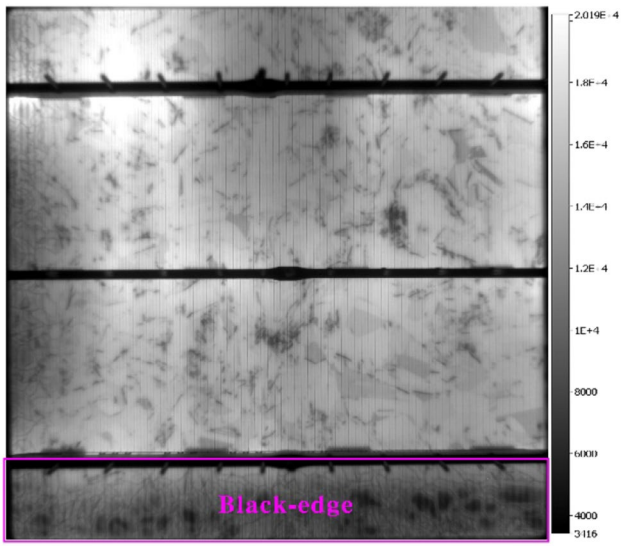

Fig. 7 "Black-edge" on solar cell

Table 1 The Ave. Eta and Irev2 of wafers by vertical and horizontal cutting

Silicon bricks		Eta	Irev2
Vertical-cut	Total	19.08%	0.62%
	Red zone	17.90%	0.95%
	Non-red zone	19.40%	0.14%
Conventional-cut		18.98%	0.45%

wafers, and their Irev2 is about three times higher. These observations indicate that the red zone created by conventional cutting does indeed affect cell efficiency and Irev2.

4 Conclusions

In contrast to the conventional approach, this study utilizes vertical cutting to investigate the electrical properties of the red zone located at the periphery of multi-crystalline silicon ingots. The comprehensive analysis included assessments of lifetime, photoluminescence (PL) images, cell efficiency, and leakage current. Initially, the lifetime in the red zone of multi-crystalline silicon ingots experiences a decrease followed by an eventual increase. A direct correlation was observed between cell efficiency and the lifetime of silicon wafers within the red zone at the ingot's edge, exhibiting an initial decline followed by improvement. Notably, beyond a distance of 12 mm from the non-red zone, the red zone's impact on efficiency diminishes significantly. Within the red zone, where the lifetime falls below 1 μs, a pronounced negative effect on cell efficiency is evident, with the average efficiency being 1.5% lower than that in the non-red zone. The insights derived from this study provide valuable guidance for the removal of silicon ingot edges.

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Data Availability No datasets were generated or analysed during the current study.

Declarations

Ethics Approval Not applicable.

Consent to Participate All authors will agree to participate.

Consent for Publication I have read and understood the publishing policy, and submit this manuscript in accordance with this policy.

Competing Interests The authors declare no competing interests.

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