Silicon (2023) 15:2703–2714
https://doi.org/10.1007/s12633-022-02191-8

ORIGINAL PAPER

Impact of High-temperature and Interface Traps on Performance of a Junctionless Tunnel FET

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Received: 29 July 2022 / Accepted: 19 October 2022 / Published online: 8 November 2022
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Abstract
Junctionless transistor (JLT) which does not have a PN junction in the source-channel-drain path, is reported to have a lower OFF-state current and therefore is more scalable to lower channel lengths compared to a conventional MOSFET, moreover a JLT also offers easy fabrication steps. Tunnel FET (TFET) provides a theoretically possible limit of subthreshold swing (SS) and has applicability for low-power electronics. Combining junctionless technology in a TFET (JL-TFET), the possible application of the device is looked into, for further low-power and high-temperature applications. This work analyses the performances of a JL-TFET for high-temperature applications and the same is compared with a conventional p-i-n silicon-on-insulator tunnel field effect transistor (p-i-n SOI-TFET). Using calibrated technology computer-aided design (TCAD) simulations, analog circuit performance parameters like ON-state to OFF-state current ratio ($\boldsymbol{I_{ON}/I_{OFF}}$), subthreshold slope (SS), transconductance ($\boldsymbol{G_m}$), gate-to-source capacitance ($\boldsymbol{C_{GS}}$), gate-to-drain capacitance ($\boldsymbol{C_{GD}}$), and cut-off frequency ($\boldsymbol{f_T}$) etc. are analyzed for temperatures till 500 K. ON-state current of JL-TFET increases in the order of hundreds of $\boldsymbol{\mu A/\mu m}$ at high temperatures, whereas p-i-n SOI-TFET shows lesser temperature sensitivity. JL-FET is more applicable to low-power applications, whereas a p-i-n SOI-TFET has more suitability for high-speed applications. Dual material technology adoption helps in improving the ambipolar behavior of the device. Analysis of interface traps is carried out in this architecture where the concentration, energy positions, and energy width of the distribution of acceptor-like and donor-like traps at the interface of semiconductor and oxide are also evaluated.

Keywords Analog applications · High-temperature · Junctionless Tunnel FET (JL-TFET) · Non-Local Band to band tunneling (BTBT) · p-i-n SOI-TFET · Gate-separation length

1 Introduction

Junctionless transistors (JLTs) exhibit better SCEs, and therefore, the channel length can be reduced further to a lower value compared to a conventional MOSFET. A JLT has homogeneous and uniform doping and bears no PN junction in the source-channel-drain path making the fabrication process of process relatively simpler and cost-effective than a junction-based device [1, 2]. Tunneling field-effect transistors (TFETs) have been studied immensely for low voltage applications. However, even if the device has a lower subthreshold slope; the ON-state current is lesser, resulting in a lower I_{ON}/I_{OFF} ratio (typically <$10^{-6}A$) at lower voltages [3]. Other drawbacks of TFETs are ambipolar conduction, large gate-to-drain capacitance, etc. [4, 5]. Pocket doping [6], gate work-function engineering [7], hetero material [8], gate-to-drain overlap [9], hetero-dielectric TFET [10], etc. are investigated to address these shortcomings. Interface traps influence the degradation of drain current in a TFET, because of which there is a finite density of states inside the semiconductor bandgap [11]. Under the influence of thermal force, these interface traps are emitted to the conduction band in a trap-assisted tunneling process, thereby expanding the switching response of the device [12].

Combining both junctionless transistors and TFETs, we study junctionless TFET (JL-TFET) for low-power and high-temperature applications. As JL-TFET is supposed to offer relatively easy fabrication steps as compared to a conventional TFET because of the removal of the PN junctions. Moreover, as the temperature changes,

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device performance parameters such as ON-OFF current ratio (I_{ON}/I_{OFF}), transconductance (G_m), threshold voltage (V_{TH}), and cut-off frequency (f_T) change significantly which will affect overall performance in an integrated circuit (IC) [13–15] and that we are studying for JL-TFET here.

Moreover, interface traps have a drain current dependency and therefore, are critically important to study their effect on device reliability. The type and position of interface traps [10] affect the drain current differently. Oxide traps are defects in the oxide layer of a MOSFET and interface traps are defects at the oxide–semiconductor interface. Interface traps are typically characterized as donor trap and acceptor trap types. The donor trap can act as a positive interface trap in an empty state. The acceptor trap is called a neutral charge when it is in an empty state and the negative interface trap is when the empty state is occupied by an electron. Holes or electrons that are trapped in the oxide region from ionizing radiation during the fabrication process and also due to hot electron stress. Oxide traps, often treated as fixed states do not transfer charges to or from Si on a time scale of measurements; however, switching states may exchange charges with the Si [16]. Mobile oxide charges are impurities/toxins from Na^+, Li^+, or K^+ ions that may occur during the fabrication process. Oxide traps may change the threshold voltage of the device and therefore affecting the device and circuit performances. Also, trap charges often introduce 1/f noise. Often low-temperature annealing process is used to reduce these defects. Here, we are interested in interface traps only. Interface trap densities at Si/SiO_2 the interface of a MOSFET was measured by the substrate bias dependence of the subthreshold slope quite reliably and accurately [17]. Dual gate material along with dual gate dielectric stack in a double gate TFET [18]; laterally stacked gate oxide TFET as compared to a vertically stacked gate oxide TFET [19]; source pocket engineered TFET [20] are reported to have better performance in presence of traps.

The interface traps are supposed to affect the drain current differently for different devices as per the working physics of the device. In tunnel FETs, these traps mostly occur due to a high electric field at the tunneling interface, and the effect of temperature and hot carriers influences them [21]. In TFETs, the drain current is due to band-to-band tunneling (BTBT). Because the BTBT rate depends on the electric field exponentially, interface traps have a greater influence on the drain current on TFETs [22]. The types of interface traps (donor or acceptor), their density (N_{OD}, $N_{OA} = N_O$), and the corresponding trap energy level (E_O) within the forbidden gap also carries a different impact on the drain current. Ehteshamuddin et al. observed that unlike donor-type traps; the acceptor-type traps deteriorate the BTBT mechanism in an n-TFET while it improves the same in a p-TFET [23]. The donor-like and acceptor-like interface traps play a critical role in threshold voltage and therefore drain the current of a device [24].

There are many reports on the effects of interface traps on drain current, random telegraph noise, in the presence of high temperature, etc., a few of them are discussed as follows. Pezzimenti et al. concluded that the intrinsic defect concentration may be at least one order of magnitude lower than the epilayer doping concentration to avoid the formation of high-resistive paths for current [25]. Fan et al. observed substantial random telegraph noise (RTN) amplitude for a single acceptor trap near the tunneling junction; moreover, a donor trap originated even more severe impact over a broader region across the channel region, with the help of atomistic 3-D TCAD simulations. Further, they added that thinner equivalent oxide thickness or longer L_{eff}, work function variation, etc. are some of the techniques that they found to control RTN amplitude depending on trap-type and the composition/orientation of metal-gate grain [26]. The location of the traps, bias conditions, and trap types impact RTN for both FinFETs and TFETs conferencing devices and circuit characteristics [27]. Ghosh et al. analyzed the effects of traps at higher temperatures for a buried oxide TFET and found that the linearity of the device improved with the rise in temperature [28]. They further added that the Gaussian trap influence is more compared to a uniform trap on the device and circuit performance of the device [29]. Gupta et al. proposed a heterogeneous gate dielectric junctionless-TFET (HD JL-TFET) that improved the transconductance, linearity, and distortion as compared with the conventional JL-TFET [30]. Huang et al., reported with positive-bias and hot-carrier (HC) stress experiments and TCAD simulation, that the drain current degradation is mainly induced by the interface traps and/or oxide charge located above the tunneling region, which eventually reduces the tunneling field and tunneling current. The interface traps primarily encourage the degradation in transconductance, while the oxide charge is responsible for a threshold-voltage shift in TFETs. Further, they added that the interface-trap generation is dominant with positive-bias stress, and the oxide-charge formation is vital under an HC stress in n-TFETs [31]. In conventional TFETs, high concentrations of acceptor-like interface traps suppress device ambipolarity, thus lowering the OFF-state current. With an optimized TFETs, namely, advanced $InAs$-based nanowire (NW) TFETs with Al_2O_3 as the high-κ gate insulator, they proposed that the effects of interface traps can be reduced to an acceptable value [32]. Pandey et al., investigated the effect of a single charge trap random telegraph noise (RTN)-induced degradation in III–V heterojunction tunnel FET (HTFET)-based SRAM, which exhibits significant energy/performance enhancements even in the presence of RTN. To be specific, HTFET-based SRAM provided 48X lower read access delay and 1.5X reduced power consumption over Si-FinFET ST SRAM

operating at their respective minimum supply voltages [33]. Sant et al., verified both theoretically and experimentally that the trap density at the semiconductor-oxide interface has to be suppressed to achieve a sub-thermal SS, eg., for a sub-thermal SS, the density of interface traps density, $D_{IT} \leq 10^{12} cm^{-2} eV^{-1}$ [34]. Conventional MOSFET and TFETs follow the same trend for threshold voltage shift and subthreshold swing degradation induced by interface traps, however, impacts on I_{ON} are different because of different conduction. N-type TFET is intrinsically more immune to V_{TH} shift induced by acceptor/donor interface traps than an n-type MOSFET [21].

Therefore, it is of utmost importance to know the effect of traps on JL-TFET at high temperatures that are not reported to the best of our knowledge. Moreover, both junctionless transistors and TFET are advantageous for low-power applications. It would be interesting to know if JL-TFET is opportunistic at a higher temperature. Section II of this article presents the device geometries taken up for comparison, and the simulation set-up. Effects of gate-separation length along with high-temperature performance of a JL-TFET is discussed in section III and section IV. Section V shows the dual materials gate JL-TFET for improvement of ambipolar behavior in the device and section VI discusses the interface traps effects on JL-TFET followed by the conclusion.

2 Device Architectures of JL-TFET and p-i-n SOI TFET and Simulation Set-up

Figure 1 shows the 2-D schematic of the JL-TFET architecture with a highly doped N-type Concentration of $1 \times 10^{19} cm^{-3}$. The device has two gates—a fixed gate (FG), and a control gate (CG) on both sides of the source, and channel region respectively. Two gates are used to make the carriers tunnel by employing gate workfunction engineering which aids in modulating the energy bands to form a tunnel barrier. The JL-TFET has a channel length, $L_{CG} = 20nm$, and height $T_{Si} = 10nm$. The gate dielectric (HfO_2) thickness is taken as $T_{OX} = 2nm$ in between metal gate contact and channel to get the optimized results of the device [35–38]. Also, inside Fig. 1. the conventional p-i-n SOI-TFET structure with the same dimension is used as in the case of JL-TFET with a single gate over the channel region with a metal workfunction $\varphi_M = 4.58eV$. This work function has been used to match the threshold voltage of both devices at room temperature. The threshold voltage is measured using the constant current method at a constant drain current $I_D = 1 \times 10^{-7}$ A/ µm. For the p-i-n SOI-TFET the doping concentrations in the source (p^+-type), channel (p^-), and drain (n^+-type) regions are $1 \times 10^{20} cm^{-3}$, $1 \times 10^{16} cm^{-3}$, and $5 \times 10^{18} cm^{-3}$ respectively as mentioned in [18] for best performance. The energy band diagram for JL-TFET is shown in Fig. 2 at a constant drain bias $V_{DS} = 1V$ for both ON states ($V_{GS} = 1V$) and OFF state ($V_{GS} = 0V$). It has been observed that a band-to-band tunneling path is forming while input bias is changing from $V_{GS} = 0V$ to$V_{GS} = 1V$.

All simulations are carried out using Sentaurus TCAD Version R-2020.09-SP1 by Synopsys Inc. [39]. The simulation set-up has been calibrated with the transfer characteristics of junctionless TFET as shown in Fig. 3. High doping concentrations in the substrate enable the bandgap narrowing (BGN) model. Because of the high impurity atom inside the channel, in the recombination part, Shockley–Read–Hall (SRH) model is used. Along with the SRH effect, recombination of the carrier is also temperature-dependent [40]. The performance of the TFET has been investigated at varying temperatures from analog design perspectives. As the gate bias increases beyond the threshold voltage, tunneling of the mobile carriers increases, so drain current increases exponentially. Figure 3 below shows the calibration of the simulation set-up with simulation data reported in [37]. The nonlocal band-to-band tunneling (BTBT) model is used for the tunneling of carriers. Calibration of the simulated dataset is traced by changing

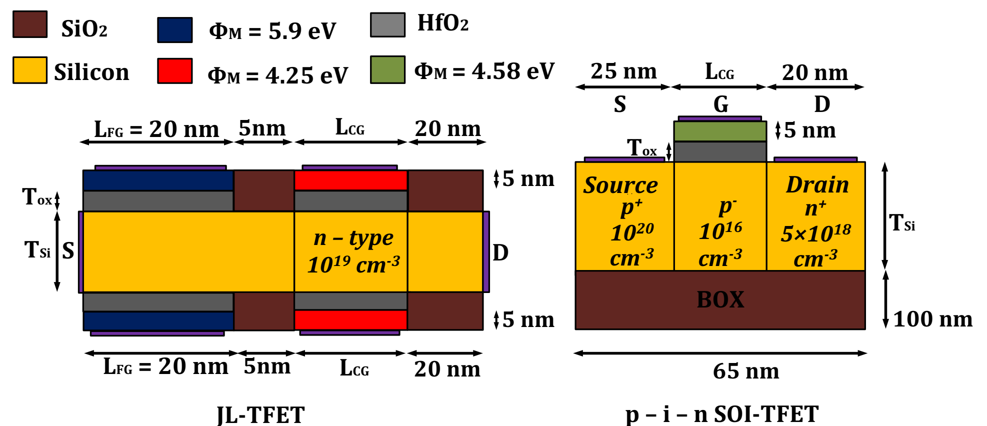


Fig. 1 Schematic of Junctionless Tunnel Field Effect Transistor (JL-TFET) and p-i-n Silicon-ON-Insulator Tunnel Field Effect Transistor (p-i-n SOI-TFET)

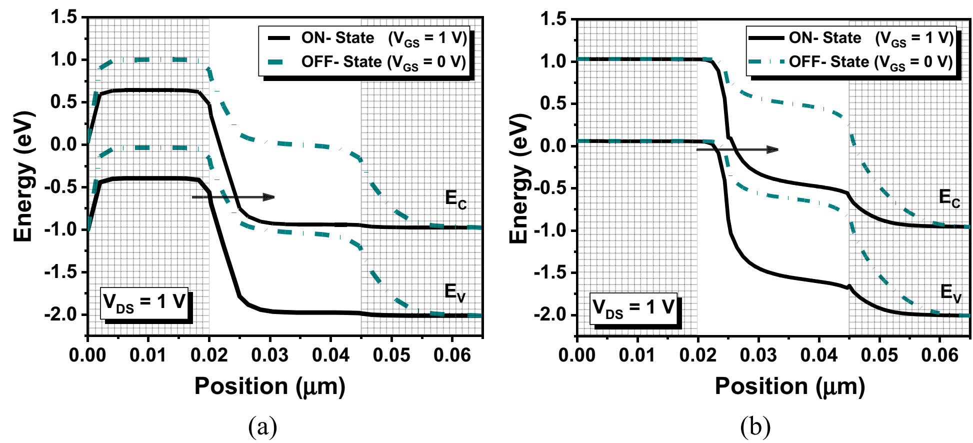


Fig. 2 Energy band diagram of (**a**) JL-TFET and (**b**) p-i-n SOI TFET at a fixed drain bias $V_{DS} = 1V$, in the ON state ($V_{GS} = 1V$) and OFF state ($V_{GS} = 0V$) at T = 300 K

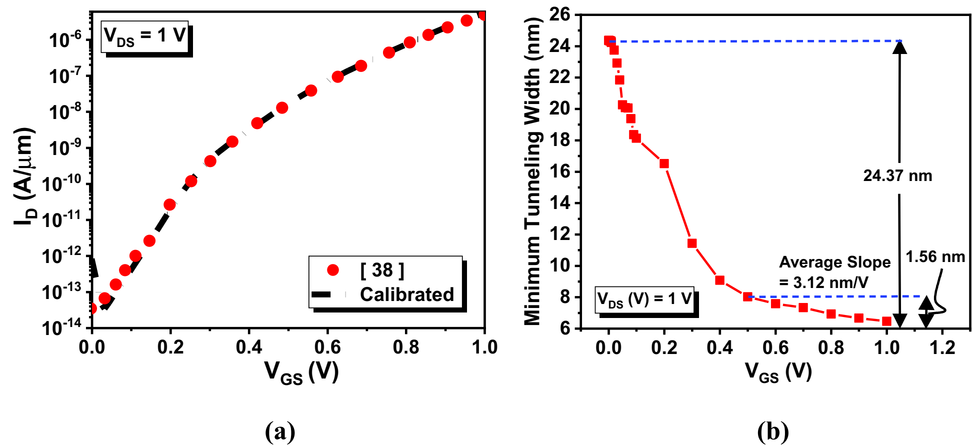


Fig. 3 (**a**) Calibration of the simulation set-up with simulation dataset [37] for gate length $L_{GC} = 20nm$, thickness $T_{Si} = 5nm$, Oxide (HfO_2) thickness $T_{OX} = 2nm$ and doping n-type concentration of $1 \times 10^{19} cm^{-3}$. (**b**) Minimum tunneling width vs. gate voltage (V_{GS})

Table 1 Parameter of nonlocal path band-to-band tunneling

Symbol	Parameter Name	Calibrated Value
A	A_{path}	$2.6 \times 10^6 cm^{-3}s^{-1}$
B	B_{path}	$4.2 \times 10^6 Vcm^{-1}$
D	D_{path}	$-0.45\ eV$
ε_{op}	P_{path}	$0.037\ eV$

A_{path}, B_{path} and D_{path} in the parameter section of the silicon substrate as shown in Table 1.

In Fig. 3(a) the calibrated transfer characteristics are in good agreement at higher gate voltages where the BTBT is dominant. Figure 3(b) shows the plot of minimum tunneling width versus gate voltage in BTBT-dominant region. Beyond V_{GS}= 0.5 V, the tunneling width almost saturates, indicating regions of high BTBT rates. The change in the tunneling width between V_{GS}= 0.5 V, and V_{GS}= 1.0 V is only 1.56 nm as compared to the total change being 24.37 nm. This accounts for only 6.41% of the total difference between the minimum tunneling widths at V_{GS}= 0 V, and V_{GS}= 1 V. However, there is a slight mismatch between the transfer characteristics in and around $0V \leq V_{GS} \leq 0.03V$, which is negligible as compared to the rest of the characteristics. A possible reason for this mismatch is extremely low BTBT in the off-state, which is supported by the minimum tunneling width in the said regime of V_{GS} from Fig. 1(b). In this voltage region, the corresponding drain current is negligible for practical measurements in fabricated devices.

3 Effects of Gate-separation Length Between Fixed Gate and Control Gate

Figure 4(a), shows the transfer characteristics at two different temperatures, where Fig. 4(b) traced the band diagrams along the channel length for the four gate-separation lengths at 300 K. As the gate-separation length increases from 5 nm, it is observed from Fig. 4(b) that the width of the tunneling region increases, and hence ON-state current decreases. With the increase in separation length at fixed drain bias, the ON-state resistance increases at the surface of the JL-TFET. As evident from the band diagram with the increase in gate-separation length, the gradient of the bands near the tunneling barrier decreases resulting in decrease in the magnitude of the electric field. The electric field has its maximum

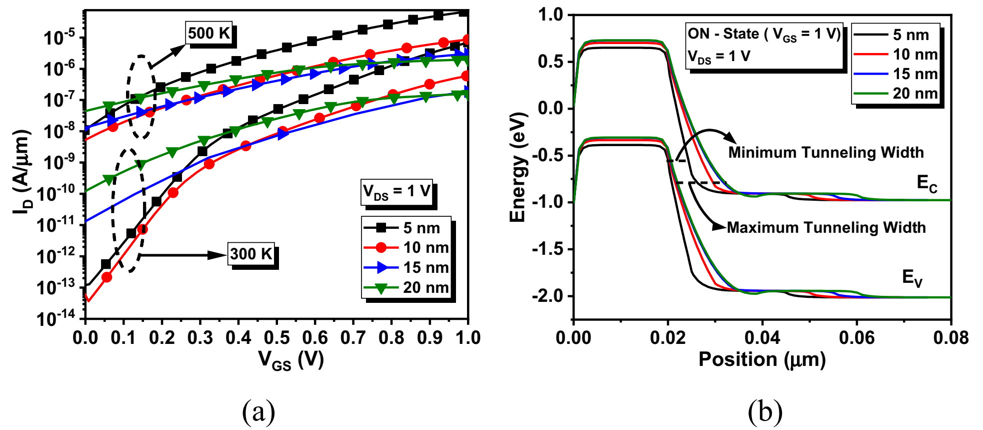


Fig. 4 (**a**) Transfer characteristics (**b**) Energy band diagram of JL-TFET for separation lengths of 5 nm -20 nm between the gates at fixed drain bias $V_{DS} = 1V$, channel length $(L_{CG}) = 20nm$, height $T_{Si} = 10nm$, $oxidethickness(T_{OX}) = 2nm$ for temperatures at 300 K and 500 K

value of 5883.17 V/cm for separation length of 5 nm and it decreases with the increase in the separation length. The least possible separation between the gates gives higher ON-state current and lower OFF-state current leading to a high $\frac{I_{ON}}{I_{OFF}}$ switching ratio of 7.18×10^6 at 5 nm and1.30×10^3 at 20 nm [41].

4 High-temperature Performance of JL-TFET

TFET was found to be more resistant to V_{TH} roll off with an increase in temperature. While the temperature dependency is feeble in the BTBT-dominated area, it is more in the low electric field range because of the strong temperature dependency of SRH generation–recombination [42]. On the other hand, junctionless transistors show high-temperature advantages in terms of lesser I_{ON}/I_{OFF} degradation with temperature [43]. Because JL-TFET is studied by many authors as advantages over TFET in terms of a) excellent ON–OFF characteristics b) lower subthreshold swing and better switching performance [37]. In addition, that they reported JL-TFET is relatively easy to fabricate, so it would be interesting to see the high-temperature performances of the device in comparison to p-i-n SOI-TFET.

In Fig. 5(a) the transfer characteristics are plotted for both the devices by varying the temperature from room temperature (~ 300 K) up to 500 K at $V_{DS} = 1V$. It is observed that there is more ON or OFF-current variation with temperature for JL-TFET. However, JL-TFET still holds better I_{ON}/I_{OFF} till $T \sim 400K$, after which p-i-n SOI-TFET outperforms. This is because the probability of band-to-band generation is increased more in JL-TFET than in p-i-n SOI-TFET with temperature. For p-i-n SOI-TFET the probability of band-to-band generation is more but less sensitive with temperature as shown in Fig. 5(b) and more is explained below.

The current ($|I| = q\int GdV$, where q is the charge of electron and G is generation rate and V is the applied field) is determined by Kane's Model, where G(E) is given by [44]

$$G(E) = A\frac{E}{\sqrt{E_g}}\exp(-BE_g^{\frac{3}{2}}/E) \tag{1}$$

where E = Electric Field, E_g= Band Gap, A, and B are the constant parameter depending on the effective mass of valance and conduction band. We have considered the phonon-assisted tunneling process in our physics model for which A and B can be expressed as

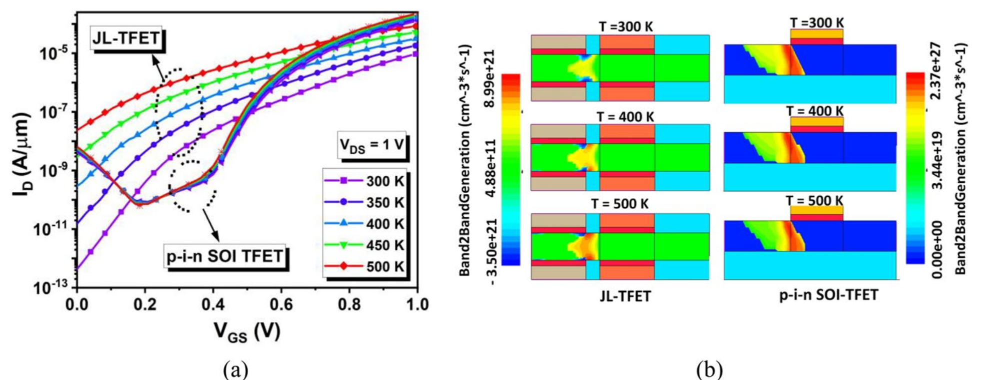


Fig. 5 (**a**) Transfer characteristics with temperature for JL-TFET and p-i-n SOI-TFET at a fixed drain bias $V_{DS} = 1V$ channel length $(L_{CG}) = 20nm$, height $T_{Si} = 10nm$, $oxidethickness(T_{OX}) = 2nm$ (**b**) Band-to-band generation profile with temperature for both JL-TFET and p-i-n SOI-TFET at gate bias $V_{GS} = 1V$ and drain bias $V_{DS} = 1V$

$$A = \frac{g\left(m_V m_C\right)^{3/2}(1 + 2N_{op})D_{op}{}^2(qF_0)^{5/2}}{2^{21/4}h^{5/2}m_r{}^{5/4}\rho\varepsilon_{op}[E_g(300K) + \Delta_C + \Delta_V]^{7/4}} \quad (2)$$

$$B = \frac{2^{7/2}\pi m_r{}^{1/2}[E_g(300K) + \Delta_C + \Delta_V]^{3/2}}{3qh} \quad (3)$$

The values of constants are directly related to a physical parameter that influences the device's characteristics. After calculating the m_r value from the default values while calibrating, we have changed the other parameters to get the expected transfer characteristics with the values shown in Table 1. On the other hand, in the non-local BTBT model, the current depends on the band edge profile along the specified path. In this model, the electric field is locally defined at each mesh point by setting length and permeable permission in the specified region interface within the math section of the s-device [39]. The crystal lattice of the semiconductor material gets expanded and interatomic bonds are broken with the increase in temperature which can be written as

$$E_g(T) = E_g(0) - \frac{\alpha T^2}{(T + \beta)} \quad (4)$$

$E_g(0)$= Band gap at 0 K, α, and β are constant for the best fit of the experimental data. Reduction of energy bandgap with temperature affects the ON-state current as well as OFF-state current as the tunneling distance is reduced [45]. With an increase in temperature, the number of broken bonds also increases more in n-type semiconductors than intrinsic type semiconducting material. A p-i-n SOI-TFET needs more thermal energy than n channel JL-TFET. Hence JL-TFET is more temperature sensitive.

The threshold voltage (V_{TH}) is matched for both devices at room temperature by tunning the metal work function of p-i-n SOI-TFET. Metal workfunction $\varphi_M = 4.58eV$ of p-i-n SOI-TFET matches the threshold voltage ($V_{TH} = 0.56V$) at room temperature. Table 2 shows threshold voltage variation with the temperature at fixed drain-to-source bias, $V_{DS} = 1V$. We have traced the threshold voltage by using the constant current method ($V_{TH} = V_{GS}\ at\ I_{DS} = 10^{-7}A$). For a p-i-n SOI-TFET, V_{TH} is marginally altered compared to a JL-TFET, where is a good chance; because of lesser reduction of an energy band gap in p-i-n SOI-TFET with temperature as the channel is intrinsic-type which contains a smaller number of mobile charges, than the n-type heavily doped charges and from the band diagram we can see small tunneling width is present. For a p-i-n SOI-TFET channel in intrinsic and drain is n-type, but less doped compared to n-channel JL-TFET. At higher gate voltage, velocity gets saturated, mobility degrades more in p-i-n SOI-TFET than JL-TFET). For the same reason, subthreshold swing $[SS = \partial V_{GS}/\partial(\log_{10}I_D)]$ is lesser temperature sensitive for p-i-n SOI-TFET than a JL-TFET as shown in Table 2.

Transconductance ($G_m= \partial I_D/\partial V_{GS}$) is slightly better for p-i-n SOI-TFET. Moreover, G_m of p-i-n SOI-TFET is lesser sensitive to temperature than the other device. However, G_m/I_D is better for a JL-TFET at a higher temperature. The cut-off frequency of the device, $f_T = G_m/2\pi C_{GG}$, where C_{GG} is the total gate capacitance is better for p-i-n SOI-TFET and lesser sensitive to temperature than JL-TFET. For the same reason, the gain bandwidth product of the device, $GBW = G_m/2\pi\times 10 \times C_{GD}$ at DC gain of 10 units, is better for p-i-n SOI-TFET even at a higher temperature than JL-TFET. Overall, from Table 2, it can be concluded that a) I_{ON}/I_{OFF} the ratio is comparatively higher for JL-TFET till $T = 400K$, after which the p-i-n SOI TFET has moderately better value b) p-i-n SOI TFET has better transconductance from low–high temperatures, c) there is more threshold voltage variation with T for JL-TFET, d) JL-TFET offers relatively better subthreshold swing compared to p-i-n SOI TFET, e) p-i-n SOI TFET has better gate-to-source capacitance (C_{GS}), gate-to-drain capacitance (C_{GD}), cut-off frequency (f_T) and gain bandwidth product (GBW)

Table 2 Electrical parameters for variation in temperatures of JL-TFET and p-i-n SOI-TFET

Temperature (*K*)		$I_{ON}(\mu A/\mu m)$	$I_{OFF}(pA/\mu m)$	$I_{ON}/I_{OFF}(\times 10^6)$	V_{TH} (*V*)	*SS* (*mV*/*dec*)	G_m (mS)	(G_m/I_D)	C_{GG} (*fF*)	f_T (*GHz*)	*GBW* (*GHz*)
300	JL-TFET	6.91	0.963	7.18	0.56	56	0.049	14.1	1.4	5.6	0.6
	p-i-n TFET	90.8	10,091	0.00899	0.56	58	0.61	1478.8	0.23	420	130
350	JL-TFET	13.91	3.65	3.8	0.43	58	0.083	16.65	1.5	9.2	0.99
	p-i-n TFET	106	11,690	0.00906	0.55	62	0.71	1486.6	0.24	480	150
400	JL-TFET	26.49	121	0.2189	0.30	61	0.12	2119.2	1.6	13	1.4
	p-i-n TFET	124	13,444	0.00922	0.55	73	0.82	1508.5	0.25	520	170
450	JL-TFET	42.53	1311	0.03244	0.22	69	0.17	2501.7	1.7	17	1.9
	p-i-n TFET	143	15,322	0.00933	0.54	87	0.93	1526.1	0.26	560	180
500	JL-TFET	68.52	11,166	0.00613	0.12	123	0.25	2740.8	1.8	22	2.5
	p-i-n TFET	164	17,298	0.00948	0.53	143	1.06	1547.1	0.29	570	200

performance than JL-TFET. In conclusion, JL-TFET is a better fit for low-power applications and p-i-n SOI TFET is more profitable for high-speed applications compared to a JL-TFET.

5 Improvement of Ambipolar Behavior in a JL-TFET

In this section, two different gate materials in the control gate part of different work function φ_{M1} and φ_{M2} are considered, where φ_{M1} is kept fixed to 4.25 eV, and φ_{M2} is varied to study the transfer characteristics of JL-TFET for different temperatures. The increase in the work function in the channel drain region increases the tunnel length for both the ON-state and OFF-state current. Thus, increasing φ_{M2}, slightly decreases the current as tunnel length increases. There is an increase in ambipolar current as φ_{M2} is increased which is shown in Fig. 6(b) through a BTBT contour for φ_{M2} = 4eV and φ_{M2} = 4.25eV at $V_{GS} = -0.1V$. Decreasing the value of φ_{M2}, increases the OFF-state current which is the leakage current. This increase in leakage current is due to the shift in energy band in the upward direction that leads to increasing tunnel length as shown in Fig. 6(c). At the superthreshold region, there is no change in ON-state current (Fig. 6(d)) because the energy band remains fixed without any shift in the upward and downward direction in the source channel region. As the gate voltage decreases, the energy band of the channel region shifts upward due to which the electrons from the valence band of the channel tunnel to the conduction band edge of the drain, thereby increasing the ambipolarity [46, 47]. So, for better performance ambipolar behavior can be reduced by shifting the energy band of the channel/drain region to a downward direction which can be done by reducing the value of the work function. The work functions in the dual material gate JL-TFET can be optimized for the improvement of I_{ON}, which is a drawback for the device.

6 Role of Interface Traps on Junctionless -TFET at High-Temperature

In a dielectric material like SiO_2, HfO_2, and many more oxides, charges may be trapped in the form of impurities at the interface. The trapped oxide charges arise out of the defects which are caused due to empty atomic valences at the Si-SiO_2

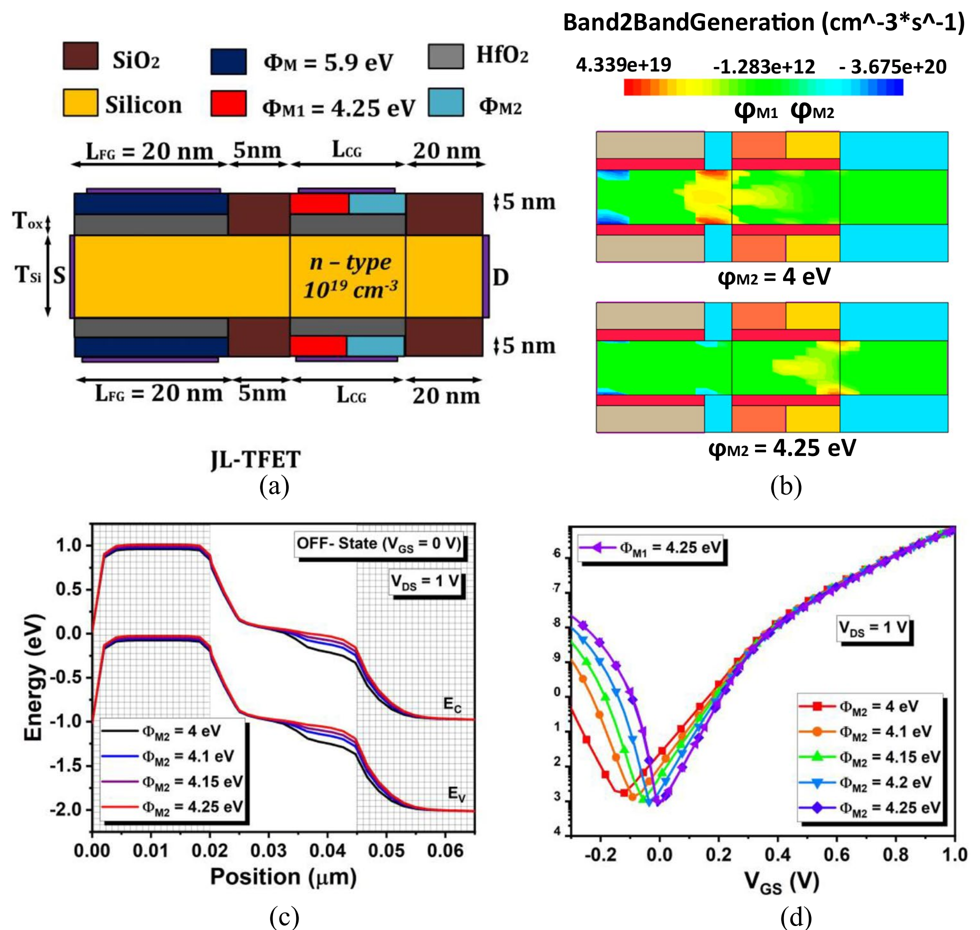


Fig. 6 (**a**) Schematic diagram for dual gate material JL-TFET, (**b**) BTBT contour for the dual control gate material $\varphi_{M2} = 4$eV and $\varphi_{M2} = 4.25$eV at$V_{GS} = -0.1V$, (**c**) Energy Band diagram variation of φ_{M2} at $V_{GS} = 0V$ (OFF-State condition) at T = 300 K, (**d**) Transfer characteristics for a work function of the material near the fixed gate at T = 300 K

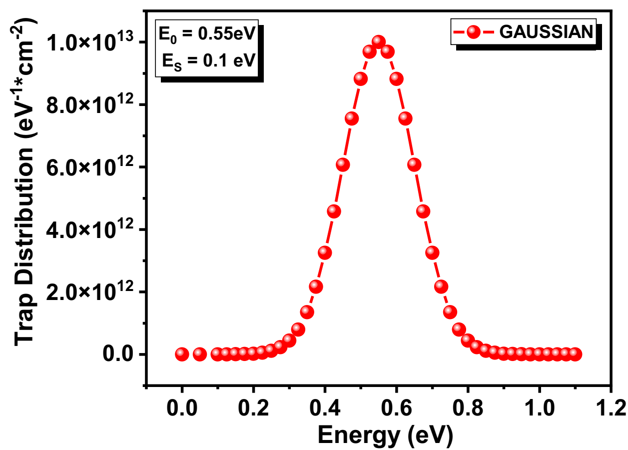


Fig. 7 Gaussian distribution trap in the oxide–semiconductor interface

interface causing charges to get trapped at the interface [48]. In this section, a circumstantial investigation of the role of trap type, trap density concentration, trap energy levels and trap energy width in affecting the characteristics of JL-TFET with HfO_2, high $-k$ gate dielectric is presented.

In this analysis, the Gaussian trap distribution is selected as it closely follows experimental evidence as compared to uniform and exponential distributions [49], defined mathematically Fig. 7 as [39]

$$D_{Gau} = N_0 e^{\left(-\frac{(E-E_0)^2}{2E_S^2}\right)} \tag{5}$$

where, N_0 is the peak density concentration, E is the variable energy, E_0 is the position of energy corresponding to peak density concentration, and E_S defines the width of the Gaussian distribution such that if $E = \sqrt{2}E_S$ then the concentration of the traps is $1/e$ of the peak density concentration, N_0. Two types of traps are taken into consideration, namely, acceptor-like traps, and donor-like traps. The former type of trap is considered in the upper half of the energy bandgap, while the latter is considered in the lower half of the energy bandgap. We have assumed that the localized interface trap charges are located at Si/HfO_2 interface where the capture cross section σ, $(\sigma_e = \sigma_h)$ is 10^{-14} cm^{-2}.

Figures 8(a), and (b) exhibit the transfer characteristics for the gate-separation lengths in presence of acceptor-like, and donor-like interface traps. From the above figure it is clear that for all the cases, an increase in gate-separation lengths degrade the device performance, resulting in extremely poor switching ratios as evident from the transfer characteristics. The acceptor- like traps and donor-like traps are taken into consideration where both the characteristics follow the same trend as for the case of no trap JL-TFET for aforementioned reasons. Further analyses are done for both acceptor-like traps and donor-like traps for two different concentrations taking 5 nm as gate-separation length.

Figure 9 shows the transfer characteristics concerning traps for the increase in temperature, where two interface trap density concentration is taken into consideration having maximum trap density concentration $N_0 = 10^{13} cm^{-2}$ and minimum trap density concentration of $N_0 = 10^{10} cm^{-2}$ for both acceptor-like traps and donor-like traps. The ON-State current and OFF-State current increase as the forbidden gap of the silicon decreases with an increase in temperature [50]. The more the trap concentration, the more the trapping of carriers, and the lower the current for acceptor–like traps. If the dissimilarity of the characteristics among acceptor-like traps and donor-like traps is observed, acceptor-like traps are found to affect the ON state of the device as opposed to donor-like traps which affect the ambipolar state of the device [51]. However, the fact that both are similar in dominance in the OFF state is observable from the characteristics.

6.1 Effect of Traps Due to Variation in Gaussian Peak Location

The peak position of the Gaussian distribution of traps has great significance in the current characteristics of JL-TFET.

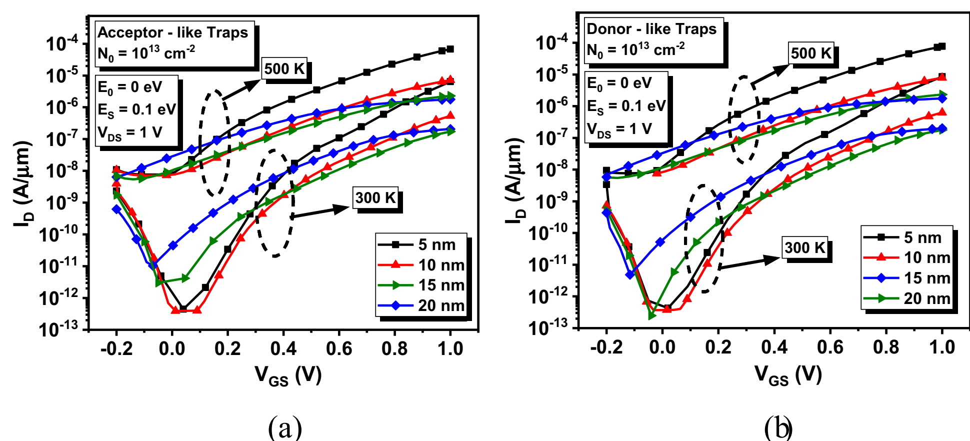


Fig. 8 (**a**) Acceptor-like traps and (**b**) Donor-like traps transfer characteristics curve with the separation length between the gates taking Gaussian distribution peak location for temperatures at 300 K and 500 K

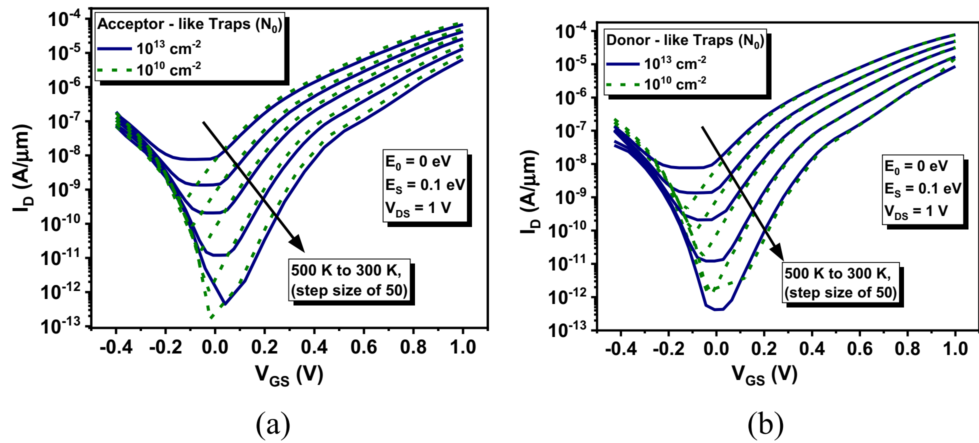


Fig. 9 Trap transfer characteristics curve for drain current versus gate-to-source voltage for different peak density concentrations for different temperatures (**a**) acceptor-like traps, (**b**) donor-like traps

The results of these variations for both acceptor-like traps and donor-like traps from deep to shallow levels are shown in Figs. 10(a) and (b), respectively. We assume that the peak density concentration of interface traps such as donor-like traps and acceptor-like traps type is $10^{13}cm^{-2}$ where the energy distributions are located between $E_i + 0.3eV$ and $E_i - 0.3eV$ considering E_i as the reference level for an increase in temperature from 300 to 500 K. Out of them, the peak position in the deep level at zero gate voltage has the maximum OFF-state current which decreases as we move to the shallow trap levels, whereas the ON-state current remains nearly same for all [52].

6.2 Effect of Standard Deviation on Gaussian-like Traps

Figure 11 represents the transfer characteristics due to variation of the standard deviation of Gaussian widths from 0.1 eV to 0.4 eV for temperatures ranging from 300 to 500 K. Figure 12 shows the Gaussian distributions for different E_S for the two temperatures. The widening of the Gaussian distribution with an increase in E_S shows a high distribution of interface trap density over the energy bandgap. As a result, more carriers have the probability to get trapped, and hence, the current changes. On the other hand, due to the impact of temperature, the energy bandgap for T = 500 K is lower than that for T = 300 K due to temperature-dependent bandgap shrinking. In the case of donor-like traps, a dominant effect is observed in its ambipolar state as pointed out in Fig. 9(b), and in case of acceptor-like traps, a dominant effect is observed in its on state as pointed out in Fig. 9(a).

7 Conclusion

This article describes the study of temperature analyses for a JL-TFET on analog design parameters at higher temperatures and reported a descriptive investigation into the device performance using calibrated TCAD simulations and compared the results with a p-i-n SOI-TFET. An effort was also to improve the ambipolar performance of a JL-TFET. The effects of interface traps on the device performance are also investigated. The significant conclusions are listed below:

- Increasing the separation length between the fixed gate and the control gate reduces the surface electric field and hence the ON-state current.

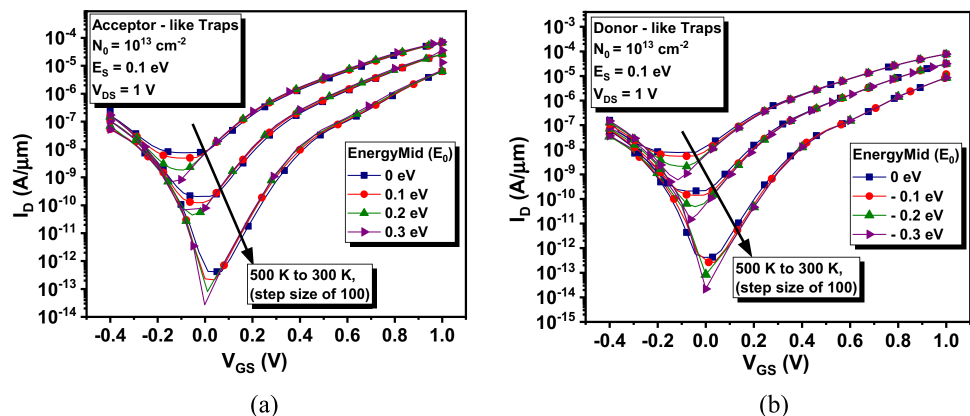
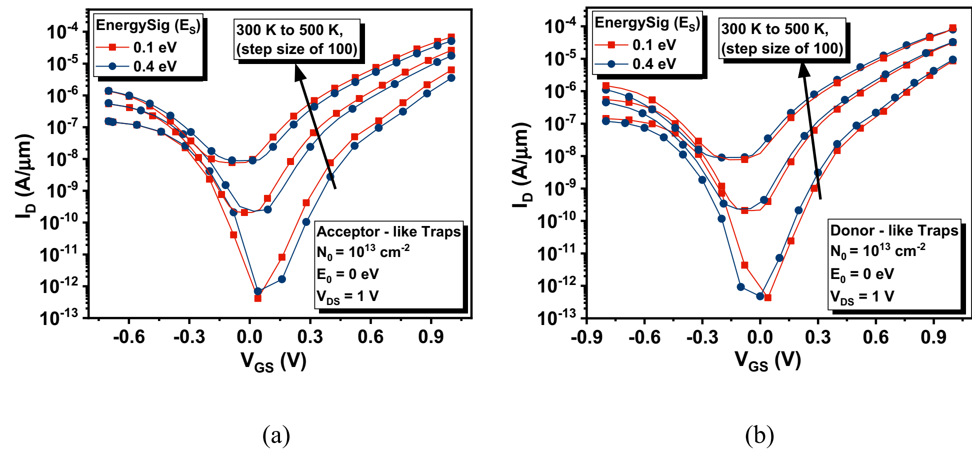


Fig. 10 Trap transfer characteristics curve for drain current versus gate-to-source voltage for different variations in Gaussian peak location for different temperatures (**a**) acceptor-like traps, (**b**) donor-like traps

Fig. 11 Trap transfer characteristics curve for drain current versus gate-to-source voltage for various standard deviations on Gaussian-like traps for different temperatures (**a**) acceptor-like traps, (**b**) donor-like traps



- As the temperature increases, the ON-state current (I_{ON}) for both JL-TFET and p-i-n SOI-TFET increases, unlike an inversion mode MOSFET, where I_D degrades with temperature.
- JL-TFET has a better I_{ON}/I_{OFF} ratio compared to a p-i-n SOI-TFET till T = 400 K, after which p-i-n SOI-TFET outperforms in temperature behaviour.
- JL-TFET outperforms in terms of better SS resulting in better quick switching to high T.
- Because of its better I_{OFF} and hence scalability; JL-TFET is a better fit for low-power applications such as memory devices. In addition, JL-TFET has fewer fabrication steps, and therefore, is cost-effective, compared to a p-i-n SOI-TFET.
- p-i-n SOI-TFETs offer better cut-off frequency (f_T) and better gain bandwidth product (GWP) till higher temperature making the device suitable for high-speed analog applications.
- Dual material technology helps in controlling ambipolar performance in a JL-TFET.
- Acceptor-like traps dominantly affect the transfer characteristics in the ON state region again donor-like traps dominantly affect the ambipolar state region where the observation is done accordingly the more closer the peak trap density value to the mid bandgap region, the traps get degraded more.

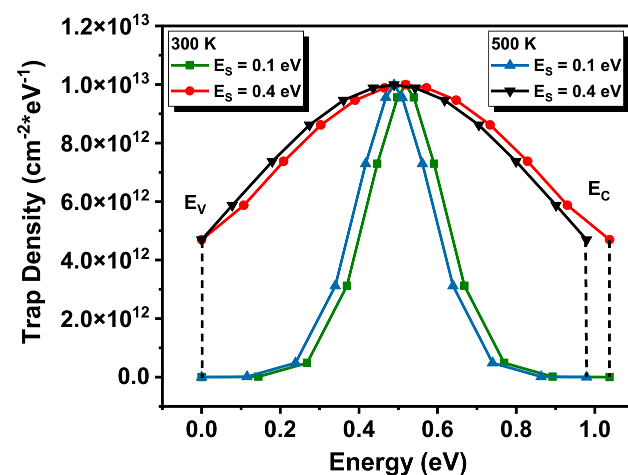


Fig. 12 Interface trap density as a function of energy for different standard deviations of the Gaussian distribution at T = 300 K, 500 K

Author Contribution Ratul Kumar Baruah conceptualized the work. Simulation and analysis were performed by Sujay Routh, Deepjyoti Deb supported by Ratul Kumar Baruah and Rupam Goswami. The first draft of the manuscript was written by Ratul Kumar Baruah, Sujay Routh, and Deepjyoti Deb and all authors commented on previous versions of the manuscript. All authors read and approved the final manuscript. Sujay Routh and Deepjyoti Deb contributed equally to this work.

Funding This work was supported by DST FIST II (Grant number: SR/FST/ET-II/2018/241). Author A has received research support from All India Council for Technical Education (Grant number: 1–6382306131).

Data Availability All the material/Simulator license is owned by the authors and/or no permissions are required. The data(s) are available to the journal if required.

Declarations

Ethics Approval The results/data/figures in this manuscript have not been published elsewhere, nor are they under consideration from any of the Contributing Authors by another publisher.

Consent to Participate All authors have consent to submit the work in this journal.

Consent for Publication We have read and understood the publishing policy and submit this manuscript in accordance with this policy.

Competing Interests We declare that the authors have no competing interests as defined by Springer, or other interests that might be perceived to influence the results and/or discussion reported in this paper.

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