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REVIEW ARTICLE

A Critical Review on Reliability and Short Circuit Robustness of Silicon Carbide Power MOSFETs

S. Sreejith[1] · J. Ajayan[2] · S. Babu Devasenapati[1] · B. Sivasankari[1] · Shubham Tayal[2]

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Abstract
Superior electrical and physical properties of SiC (Silicon Carbide) make them ideal for various high voltage, high frequency and high power electronic applications. When compared to GaAs and GaN, the advantage of SiC is that its natural oxide is SiO_2 and is used as the gate-dielectric in SiC MOSFETs. Better performance of SiC Power MOSFETs has made it as an ideal substitute to its Si counterpart. Even though the performance of SiC Power MOSFETs has improved significantly over recent years (breakdown voltage over 3300 V [144], field effect channel mobility over 160 cm^2/Vs (Cabello et al. in Appl Phys Lett 111, 2017), specific on state resistance as low as 1.63 mΩ.cm^2 (Fu et al. in Microelectron Reliab 123, 2021) and short circuit withstand time over 80 µS (Wang et al. in IEEE Trans Power Electron 31:1555–1566, 2016)), reliability issues due to the presence of near interface oxide defects and degradation due to poor quality of interface and gate dielectric is its major drawback. In this article we have extensively studied various reliability and stability issues that affect the performance of Silicon Carbide Power MOSFETs. The short-circuit behaviour and robustness of various SiC Power MOSFETs were also discussed.

Keywords SiC Power MOSFET · Short Circuit Robustness · Stability · Threshold Voltage · Gate-Oxide Reliability

1 Introduction

In various industrial applications like EVs (Electric Vehicles), renewable energy harnessing, aircrafts and in solid state switches there is a huge demand for high capacity and high frequency power converters. Higher dielectric-breakdown field strength, wider band-gap and excellent thermal-conductivity make SiC MOSFET as a suitable alternative in high capacity power convertors when compared to its silicon counterpart [1–3]. The major advantage of SPM (SiC Power MOSFET) is its capability to block high voltage with a low R_{DSON} (on state resistance/ on resistance) [4]. In the year 1992, J.W.Palmour et al. [5] designed the first SPM with U-Shape MOSFET (UMOSFET) design. J.N.Shenoy et al. [6] in the year 1996 fabricated the first double implant MOSFET (DMOSFET). The first SiC 10 kV Power MOSFET was designed in 2006 at 5A current rating by CREE [7]. Ever since rapid progression has been made in the fabrication of various SiC based MOSFET power modules [8, 9]. SPMs have replaced Si IGBTs in medium voltage applications because of its low R_{DSON} specifications and simple gate drive requirements. SiC MOSFET is broadly used in motor drives, switching mode power supplies and in grid-connected inverters due to its fast switching frequency, high junction temperature and low power loss [10–13]. Lower losses in SiC MOSFET also makes them ideal candidate in medium voltage applications. When fabricating SPMs, favorable material properties of SiC results in few design challenges. Surface electric-field is increased twice the value compared to Si, due to the wide band gap of SiC, thereby decreasing inversion layer channel mobility. Similarly energy stored in the output capacitance is increased 10 times in SiC devices due to its large critical electric-field, compared to Si device thereby limiting its operation frequency with hard switching [14]. Figure 1 shows the structure of SPM with body diode. SPM is considered as a superior candidate in power electronics field. However factors degrading its performance need to be nullified for wide scale commercialization.

✉ S. Sreejith
sreejith5488@gmail.com

[1] Department of Electronics and Communication Engineering, SNS College of Technology, Coimbatore, India

[2] Department of Electronics and Communication Engineering, SR University, Warangal, Telangana, India

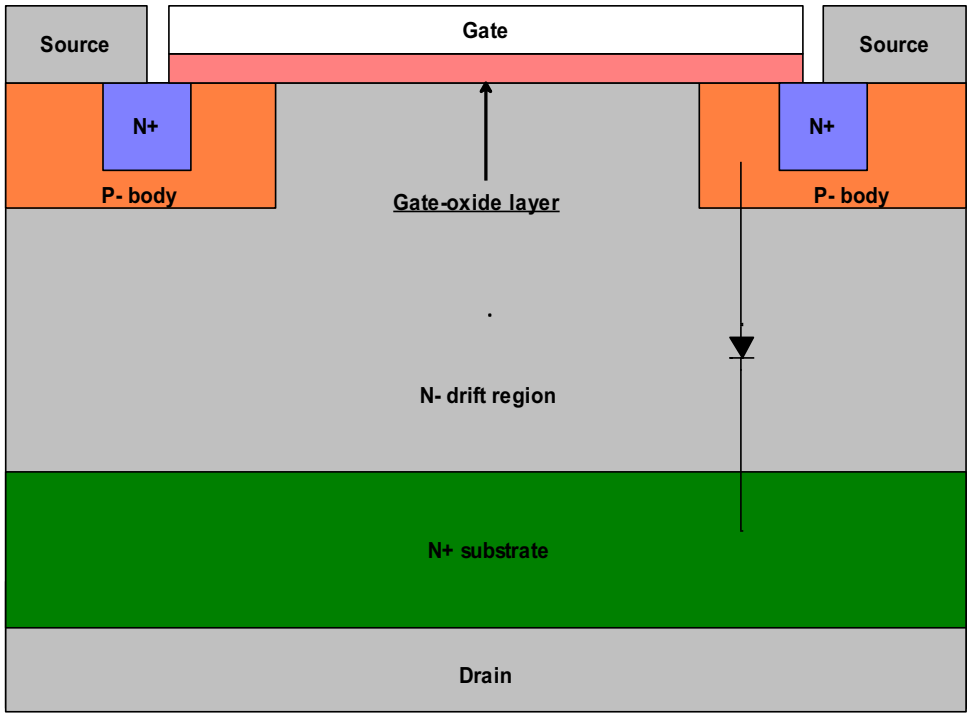

Fig. 1 Structure of SPM [15]

Table 1 Comparison of Material properties [16]

Material Property	Unit	Si	GaAs	GaN	SiC
Bandgap (Eg)	eV	1.12	1.42	3.42	3.3
Dielectric constant (ε)	-	11.8	12.9	9	9.7
Electron mobility (μ_e)	cm^2/Vs	1400	8500	2000	1000
Hole mobility (μ_h)	cm^2/Vs	600	400	850	100
Thermal Conductivity (k_T)	W/cmK	1.3	0.55	1.3–2	4.2
Critical electric field (E_c)	MV/cm	0.3	0.4	3.3	2.5
Baliga's FOM ($\varepsilon\mu Ec^2$)	-	1	-	1450	340

2 Overview of SiC Power MOSFETs

The large band-gap of SiC (~ 3.3 eV) has made it a potential semiconductor material in emerging power devices. The comparison of key material properties of SiC with Si, GaAs and GaN is given in Table 1.

When compared to 6H-SiC semiconductor materials, 4H-SiC has approximately two fold higher bulk mobility. Hence in high power switching devices 4H-SiC MOSFET is an ideal choice with high switching speed and low switching loss [17–19]. In the year 1999, S.F.Shams et al. [20] has investigated the performance of 4H-SiC MOSFET and 6H-SiC MOSFET at high temperature. Due to higher band-gap, 4H-SiC Power MOSFET gave a higher threshold voltage when compared to 6H-SiC power MOSFET (Fig. 2). In 4H-SiC MOSFET, channel-mobility is affected by the presence of high density traps at SiC/SiO_2 interface. In 2001,

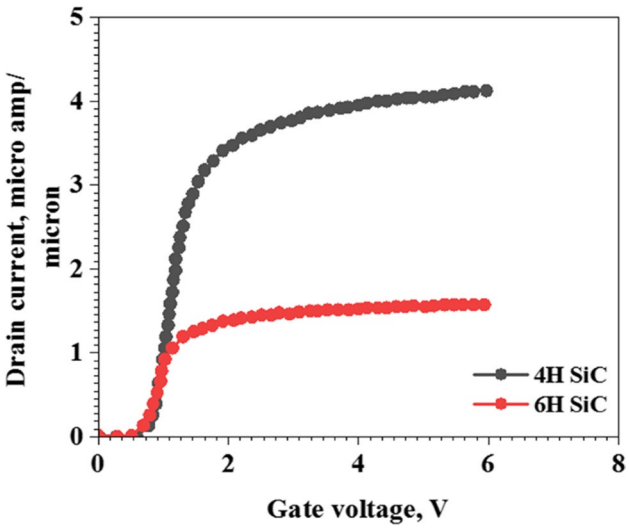

Fig. 2 Gate voltage vs. drain current plot of 4H- SPM and 6H-SPM at 500 K with N_A (p-region doping density) value as 1×10^{16} cm.$^{-3}$ [20]

S.Harada et al. [21] reported improved channel-mobility of 140 cm^2/Vs in 4H-SiC MOSFET with a BC (buried channel) structure. This increase in channel-mobility is due to the flow of large number of electrons in deep position where the channel region expands to the inside of SiC substrate away from SiC/SiO_2 interface. In 2002, J.Senzaki et al. [22] investigated the impact of H_2 POA (hydrogen post oxidation annealing) on 4H-SiC MOSFET's inversion channel-mobility. Improved inversion channel-mobility of 110 cm^2/Vs was reported in 4H-SiC MOSFET as a result of H_2 POA.

In 2004, Md Hasanuzzaman et al. [23] experimentally demonstrated the temperature dependency of lateral MOSFET fabricated in both 6H-SiC and 4H-SiC. It was reported that when compared to 4H-SiC lateral MOSFET, 6H SiC lateral MOSFET exhibited better device performance. In the study of MOSFET temperature dependence, V_{TH} (threshold voltage) is an important parameter. Calculation of V_{TH} accuracy with variation in temperature is significant because large change in output current occurs due to small changes in V_{TH}. V_{TH} can be computed as [24]

$$V_{TH} = V_{fbo} - \frac{\Delta Q_{it}}{C_{ox}} \pm 2\Phi_f \pm \sqrt{2V_0(2|\Phi_f|)} \quad (1)$$

where V_{fbo} represents flat band voltage, ΔQ_{it} represents interface state density, C_{ox} represents oxide capacitance and Φ_f represents surface potential. Φ_f can be computed as [24]

$$\Phi_f = \frac{kT}{q}\ln\left(\frac{n}{n_i}\right) \quad (2)$$

where T represents temperature, k represents Boltzmann constant, q represents electron charge, n represents density of carriers in the doped semiconductor substrate and n_i represents intrinsic carrier concentration. In 2004, S.H Ryu et al. [25] fabricated a 10 kV 4H-SiC Power DMOSFET. 42% reduction in specific on resistance (123 $m\Omega.cm^2$) was reported using a thinner highly doped drift epilayer. Also 100 ns switching time was reported in 1.3 A, 4.6 kV switching measurements thereby making it ideal for high speed switching applications. In 2005, T.Kimoto et al. [26] fabricated 1330 V (0 0 0 1) 4H SiC RESURF (reduced surface field) MOSFET. 67 $m\Omega.cm^2$ low specific on resistance, 1330 V breakdown voltage and enhanced figure of merit of 26 $MW/cm.^2$ was reported. R_{on} (on resistance) at negligible drain voltage can be computed as [26]

$$R_{ON} = \frac{Ld_{ox}}{\{\mu_{ch}W\varepsilon_{ox}(V_G - V_T)\}} + R_{drift} + R_c \quad (3)$$

where L represents channel length, d_{ox} represents oxide thickness, W represent channel width, μ_{ch} represents channel mobility, ε_{ox} represents dielectric constant of gate-oxide, V_T represents threshold voltage, V_G represents gate voltage, R_c represents resistance of n^+ contact regions including contact resistance and R_{drift} represents resistance of drift region. 4H-SPMs with AMS (adjusted multi section) guard-ring edge termination structure is ideal as a high voltage operation device with enhanced robustness. In 2017, X.Deng et al. [27] fabricated 4H-SiC AMS Power MOSFET with lightly-doped p-well guard-rings. More than 500 V to 1000 V enhancement in reverse blocking capability was reported in 4H-SiC AMS Power MOSFET with 2.5 kV blocking capacity compared to traditional SPM having same edge termination. Figure 3 shows the temperature dependence transfer curves of 4H-SiC AMS Power MOSFET.

From Fig. 3 it is evident that against high temperature 4H-SiC AMS MOSFET has better robustness. Significant improvement in electrical characteristics of planar high voltage 4H-SPM was reported with boron gate oxide treatment [28]. Remarkable enhancement in inversion channel mobility and decrease in specific R_{DSON} was observed in planar 4H-SPM as a result of boron gate-oxide treatment. Enhanced device characteristics were reported in 4H-SPM by using AIN (Aluminium nitride) as interfacial layer instead of SiO_2 between SiC and HfO_2 (hafnium oxide) (Fig. 4). When compared to SiO_2, AIN exhibited lesser dependence on interface trap density [29].

In 2018, T.Yang et al. [30] fabricated trench 4H-SiC MOSFET with DSS-MOS (double stacked shielded) region underneath the trench bottom. It was reported that this DSS-MOS structure helps in improving the gate-oxide reliability and in reducing the switching loss when used in high frequency applications. Enhanced figure of merit was also reported in DSS-MOS 4H-SiC MOSFET. In power electronics applications, SiC MOSFET's intrinsic superiorities make them an ideal alternative to traditional Si IGBTs [31–35]. In 2018, A.Marzoughi et al. [36] investigated and compared the performance of medium voltage SPM with Si IGBT. Specific R_{DSON} of 25 $m\Omega.cm^2$and R_{DSON} of 70 $m\Omega$ was reported in 3.3 kV, 30 A SiC MOSFET. At 30 A load current, switching on loss of 3 mJ and switching off loss of 0.55 mJ was reported in SPM which is 8 times smaller when compared to Si IGBT at same current and voltage rating (Fig. 5). In the same year, L.Zhang et al. [37] compared the performance of high power 1700 V, 325 A SPM under different bus voltage,

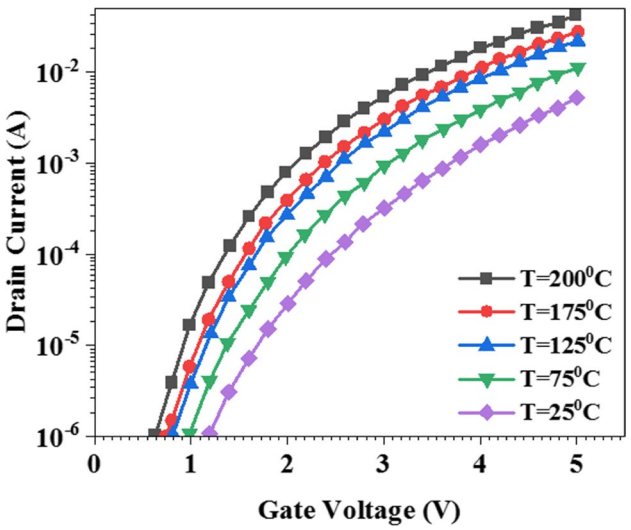

Fig. 3 Gate voltage vs. drain current plot of 4H-SiC AMS Power MOSFET from 25^0C to $200.^0$C measured at $V_{gs} = V_{ds}$ [27]

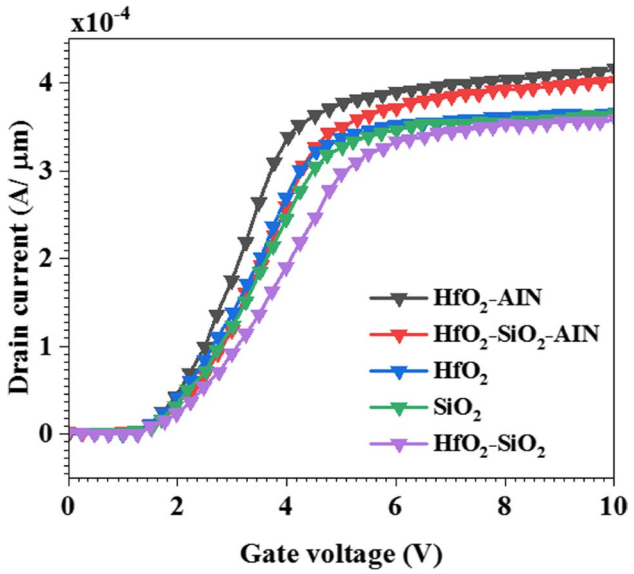

Fig. 4 Gate voltage vs. drain current plot of 4H-SPM at 300 K for various di-electric stacks [29]

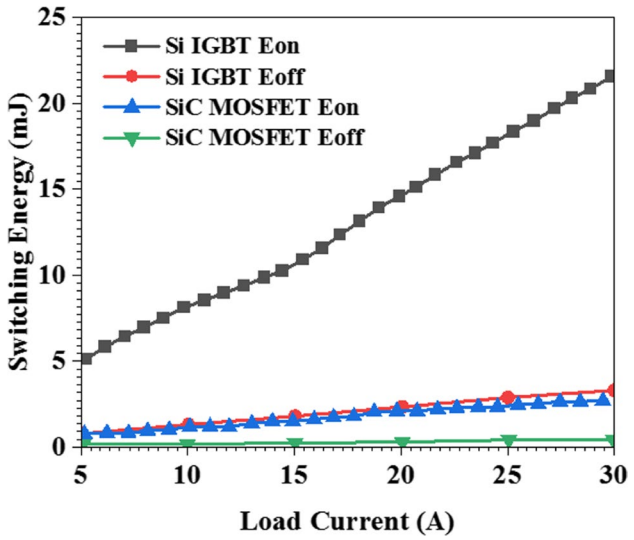

Fig. 5 Switching losses comparison plot of SiC MOSFET and Si IGBT at same current and voltage rating [36]

load current and gate resistors to Si IGBT with same power ratings. When compared to Si IGBT, linear increase in over shoot current with increase in load current was reported in SPM. In 2019, R.Chaujar [38] investigated the performance of 4H-SiC RC (recessed channel) trench gate mosfet structure with black phosphorous as gate material. Enhancement in electrical parameters like electron mobility, electron velocity and electric field was reported in of 4H-SiC RC MOSFET structure. 2.3 mA higher drain current and 10^{16} enhanced switching ratio were also reported in 4H-SiC RC MOSFET. Also from RF- figure of merit simulation results, five times increase in f_{MAX} (maximum oscillator frequency) and two times enhancement in f_T (cut off frequency) were reported in 4H-SiC RC design making it ideal for high power, high frequency and high switching applications.

The cut-off frequency can be computed as [38]

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})} \tag{4}$$

where g_m represents trans-conductance, C_{gs} represents gate to source capacitance and C_{gd} represents gate to drain capacitance.

Maximum oscillator frequency can be computed as [38]

$$f_{MAX} = \frac{f_T}{\sqrt{4R_g(g_{ds} + 2\pi f_T C_{gd})}} \tag{5}$$

where R_g represents gate resistance and g_{ds} represents drain-source conductance.

Even though 4H-SPMs were active commercially, higher value of on resistance than theoretically anticipated values remains as a major drawback. Poor value of channel mobility because of carbon clusters, dangling-bonds at the interface and in the oxide layer as well as residual carbon results in this performance deterioration [38–41]. In the year 2020, C.Fei et al. [39] experimentally demonstrated that post oxidation annealing and pre oxidation nitrogen implantation on 4H-SPM results in significant enhancement in channel mobility and reduction in R_{DSON}. The field effect channel mobility (μ_{FE}) can be computed as [39]

$$\mu_{FE} = \frac{Lg_m}{WC_{ox}V_{ds}} \tag{6}$$

where W represents gate width, L represents gate length, g_m represents intrinsic trans-conductance, C_{ox} represents accumulation capacitance and V_{ds} represents drain- source voltage.

In the same year, H.Bencherif et al. [40] investigated the impact of carbon vacancy trapping in the performance of 150 V low voltage 4H-SiC low power MOSFET. Decrease in channel mobility, increase in V_{TH} and increase in R_{DSON} was reported as a result of intrinsic defect states $EH_{6/7}$ and $Z_{1/2}$ centers on 4H-SiC low power MOSFET. Figure 6 shows the variation of channel mobility as a function of $Z_{1/2}$ trap density. From Fig. 6 it is evident that channel mobility decrease with increase in $Z_{1/2}$ trap density and temperature. Channel mobility of SPMs can be enhanced by using both nitridation methods and gate oxide doping methods (Fig. 7). From Fig. 7 significant enhancement in μ_{FE} is evident in different SiC MOSFETs with various nitridation and gate oxide doping methods. μ_{FE} values of different SPMS are given in Table 2.

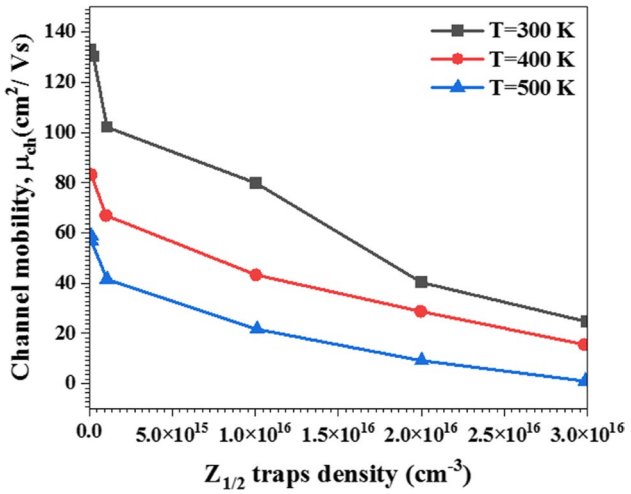

Fig. 6 Channel mobility vs. $Z_{1/2}$ trap density plot of 4H-SiC low power MOSFET for various temperature [40]

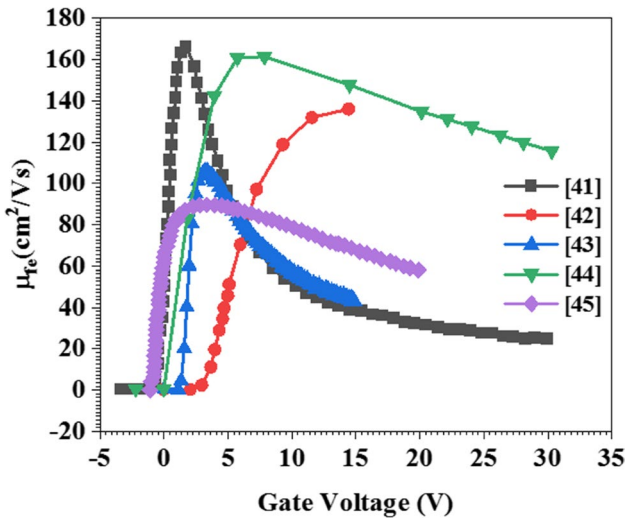

Fig. 7 Plot of μ_{FE} vs. gate voltage for different SiC MOSFETs with various nitridation and gate oxide doping methods

3 Reliability Issues in SiC Power MOSFETs

Even though SiC technology have better thermal and electrical properties specifically like higher thermal conductivity, higher break-down voltage, lower intrinsic carrier concentration and higher critical electric field their reliability and stability need to be improved further [58–61]. One of the major reliability issues in SPM is its V_{TH} instability [62–71]. In the year 2013, T.Kikuchi et al. [72] has investigated SiC MOSFET's V_{TH} instability using a novel TCAD (Technology Computer Aided Design) two dimensional degradation model. It was reported that deep and shallow level trap in the interface states as well as in the oxide can result in V_{TH} instability. In the same year, L.Yang et al. [73] investigated V_{TH} instability and leakage current degradation of SPM by performing HTGB (high temperature gate bias) and HTRB (high temperature reverse bias) tests. It was observed that positive gate-bias stress results in positive V_{TH} shift and negative bias stress results in negative V_{TH} shift. This indicates that V_{TH} shift is dependent strongly on bias stress condition including both bias magnitude and polarity under high temperature gate-bias. In 2014, A.Fayyaz et al. [74] investigated the performance and avalanche ruggedness of state of the art 1200 V SPM under Unclamped Inductive Switching (UIS) test condition. It was reported that as the number of UIS pulses increase, SPM exhibit positive V_{TH} shift. This V_{TH} shift is because of interfacial charge trapped near and at SiC-SiO_2 interface which causes significant degradation in device performance.

In the year 2015, O.Kusumoto et al. [75] has reported DioMOS (Diode integrated SiC power MOSFET) structure which exhibited enhanced device performance and better reliability with 1200 V blocking voltage. In DioMOS structure, highly doped n-type epiaxial channel layer which acts as reverse diode is formed under the gate oxide thereby eliminating external SBD (schottky barrier diode). Figure 8 shows the structure of DioMOS. SBD external diode elimination helps in reducing area consumption of SiC which helps in reducing the cost and enabling smaller packing size. HTGB test indicates very stable V_{TH} using negative and positive gate voltage stress after 2000 h at 150^{0}C. Also DioMOS is free from performance deterioration due to reverse-current since reverse-current does not flow onto the body-diode.

Table 2 An overview of μ_{FE} values of different SPMs

Ref.	μ_{FE} (cm^2/Vs)
[21]	140
[39]	25.3
[42]	133
[43]	120
[44]	160
[45]	89
[46]	19
[47]	125
[48]	108
[49]	107
[50]	55
[51]	17.8
[52]	80–110
[53]	80–85
[54]	16
[55]	102
[56]	45
[57]	150

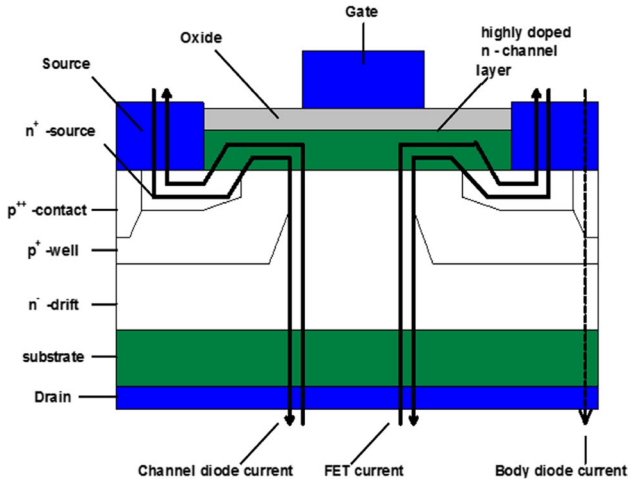

Fig. 8 Structure of DioMOS [75]

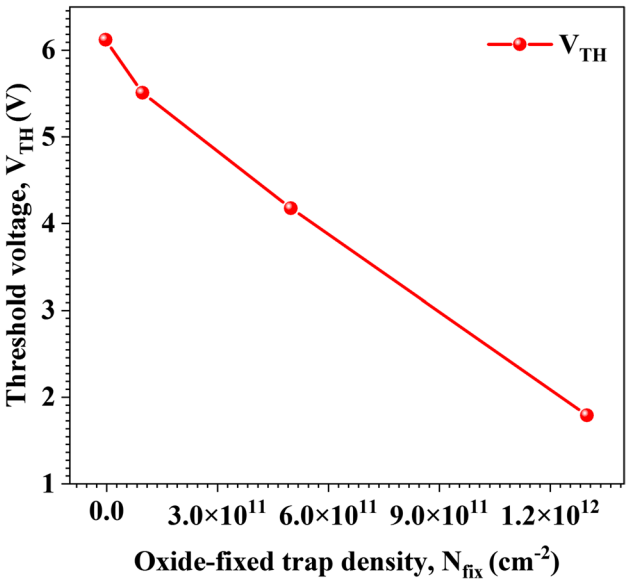

Fig. 9 Oxide fixed trap density vs. V_{TH} plot of 4H-SiC MOSFET at temperature 300 K [81]

Hence in order to prevent reliability issues, DioMOS can be an ideal alternative when compared to conventional SPMs [76]. In the year 2016, K.Matocha et al. [77] fabricated advanced SPM on 150 mm SiC wafer with specific R_{DSON} of 3.1 mΩ.cm^2 at room temperature. At 175^{0}C an increased specific R_{DSON} of 6.7 mΩ.cm^2 was reported. It was observed that at 175^{0}C after 750 h of gate stress and at gate bias of $V_{GS} = +20$ V, V_{TH} shift less than 250 mV was reported. Similarly at 175^{0}C and at gate bias of $V_{GS} = -10$ V, V_{TH} shift less than 100 mV was reported. In the year 2017, Y.Ren et al. [78] experimentally demonstrated a low inductive novel packing structure for SiC wire bond based multi-chip phase leg MOSFET module. This packing structure which is based on adjacent decoupling concept largely reduces the voltage overshoot, thereby enhancing the performance of SiC MOSFET modules. In the same year A.P.Camacho et al. [79] proposed a novel AGD (Active Gate Driver) open loop control system for SiC MOSFETs. It was reported that this AGD helps in reducing the overshoot voltage of SiC MOSFET. In the year 2019, X.Liao et al. [80] proposed a peak voltage suppression technique with MOV (Metal Oxide Varistor) as snubber circuit for SPM based DC solid state circuit breaker without compromising its fast switching capability. It was reported that this proposed method can interrupt fault current faster when compared with other traditional methods. In the same year, H.Bencherif et al. [81] has investigated the impact of carrier trapping effect and temperature on 4H-SiC MOSFET's electrical characteristics for low breakdown voltage.

The influence of 4H-SiC/SiO_2 interface-traps on V_{TH}, channel-mobility and R_{DSON} was analysed for both defective and defect free devices. It was demonstrated experimentally that oxide fixed traps have significant impact on V_{TH} value (Fig. 9). From Fig. 9 it is evident that in the presence of explicit oxide fixed trap density, V_{TH} value decreases significantly. Device failure under high electric stress due to gate oxide reliability issue is another main reason that affects the performance of SPMs [82–89]. Gate oxide reliability in OFF state can be enhanced using SiC CD (Central Dielectric) MOSFET structure (Fig. 10) [90]. When compared to conventional SiC MOSFETs, peak electric field in gate oxide decreases approximate to 30% at 2.9 kV break-down in SiC CDMOSFET (1.1 MV/cm) thereby improving the gate oxide reliability.

In the year 2020, H.Bencherif et al. [91] investigated 4H-SiC MOSFET's gate dielectric reliability under carrier trapping conditions and high temperature. The performance of 4H-SiC MOSFET was studied by using various gate

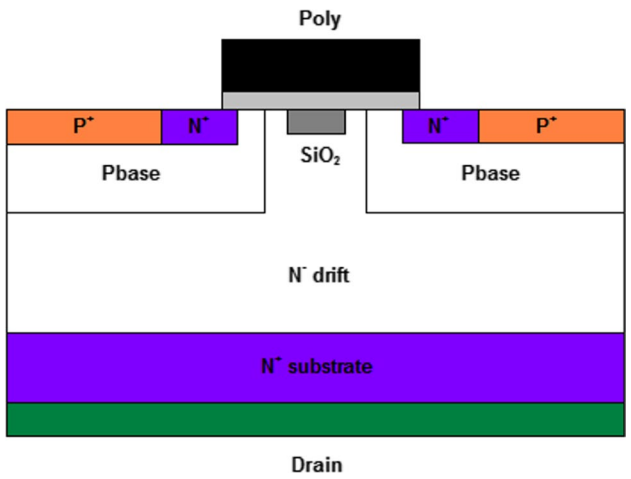

Fig. 10 Structure of SiC CDMOSFET with center dielectric layer (SiO_2) in the SiO_2/SiC surface [90]

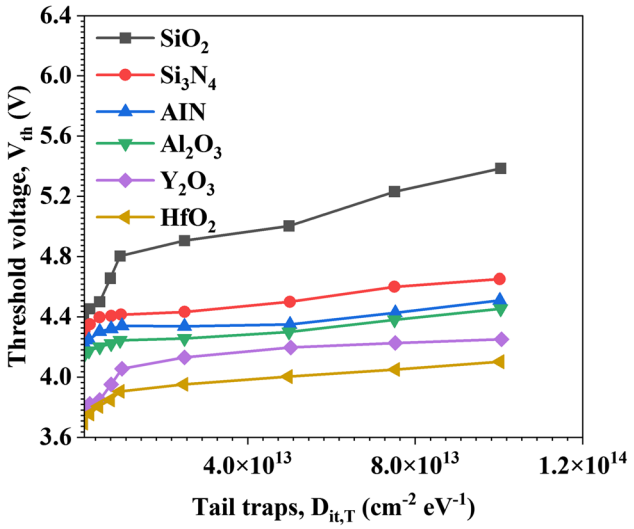

Fig. 11 Tail traps vs. V_{TH} plot of 4H-SiC MOSFET for various gate-dielectrics like SiO_2, AlN, Si_3N_4, Al_2O_3, HfO_2, Y_2O_3 [91]

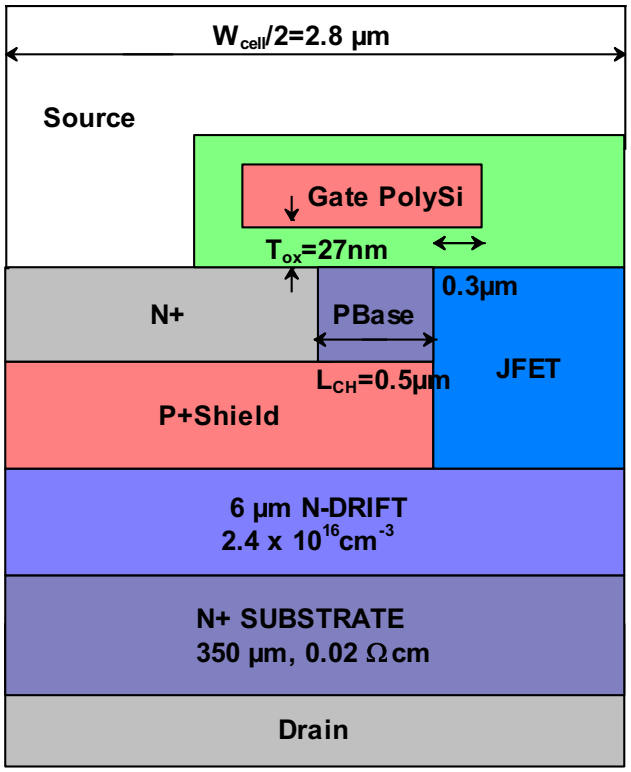

Fig. 12 Structure of ASPM with 27 nm gate-oxide thickness and inversion layer split gate structure with channel length (L_{CH}) = 0.5 µm [92]

dielectrics like SiO_2, AlN, Si_3N_4, Al_2O_3, HfO_2 and Y_2O_3. It was reported that HfO_2 gate dielectric exhibited better V_{TH} stability and good immunity against interfacial traps (Fig. 11). However by using HfO_2 increase in gate leakage current was observed which can be overcome by using a 2 nm thick thin interfacial layer in 4H SiC/HfO_2 MOS structure. In the same year, A.Agarwal et al. [92] has fabricated three novel ASPMs (Advanced SPM) with 650 V blocking-voltage without changing the gate-drive voltage of 10 V. When compared to planar gate SPMs, this ASPM exhibited enhanced characteristics and significantly longer short-circuit withstand time. Figure 12 shows the structure of ASPM with 27 nm gate oxide thickness and inversion layer split gate structure with channel length (L_{CH}) = 0.5 µm.

By reducing the L_{CH} from 0.5 µm to 0.3 µm, decrease in $R_{CH,SP}$ (Specific Channel Resistance) value was reported in ASPM. Further this reduced L_{CH} helps in increasing the G_m (trans-conductance) thereby reducing switching losses. $R_{CH,SP}$ can be computed as [92]

$$R_{CH,SP} = \frac{L_{CH}W_{Cell}}{2\mu_{ni}C_{ox}(V_{gs} - V_{TH})} \tag{7}$$

where C_{ox} represents capacitance per cm^2 for the gate oxide, μ_{ni} represents inversion channel-mobility at the on state gate bias, W_{cell} represents cell width and V_{gs} represents on state gate drive voltage.

G_M value can be computed as [92]

$$G_m = \frac{Z\mu_{ni}C_{ox}}{L_{CH}}(V_{gs} - V_{TH}) \tag{8}$$

where Z represents channel width. It was hence recommended that by reducing the channel length, gate oxide thickness and also by using split gate architecture superior performance in SPM can be achieved thereby replacing Si super junction devices. In the year 2021, H.Fu et al. [93] has reported a 1200 V class trench 4H-SiC MOSFET having P^+ shielding region surrounded partially by the buried n-region (Fig. 13) with superior FoM (Figure of Merit). Significant enhancement in forward and transfer characteristics can be achieved by the buried n-region as it restrain the depletion layer's lateral extension formed by P^+ shielding region at QS (quasi-saturation) state. 19.3% reduction in specific R_{DSON} (1.63 mΩ.cm^2) and 30% enhancement in g_{fs} (trans-conductance) were reported. 20.5% enhancement in FoM_1 value (1.45 kV^2/ mΩ.cm^2) was also reported.

The trade-off relationship between BV (breakdown voltage) and $R_{on,sp}$ (specific on resistance) can be judged using FoM_1 value which can be computed as [86]

$$FoM_1 = \frac{BV^2}{R_{on,sp}} \tag{9}$$

Similarly FoM_2 which is used to judge the dynamic characteristics can be computed as [93]

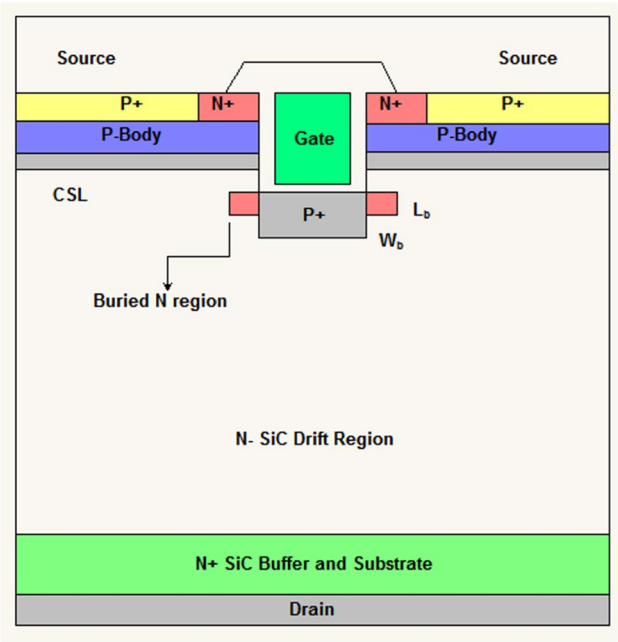

Fig. 13 Structure of 4H-SiC trench MOSFET having $P.^{+}$ shielding region surrounded partially by the buried n region [93]

Table 3 An overview of Specific R_{DSON} values of different SPMs

Ref.	R_{DSON} ($m\Omega.cm^2$)
[17]	18
[75]	4.7
[27]	32
[30]	1.95
[25]	123
[26]	67
[93]	1.63
[36]	25
[92]	5.18
[77]	3.1
[94]	4.31
[95]	6.4
[96]	15.7
[97]	2.17
[98]	1.64
[99]	2.31
[100]	5.1
[101]	6.9

$$FoM_2 = Q_{gd,sp}.R_{on,sp} \tag{10}$$

where $Q_{gd,sp}$ represents specific gate to drain charge.

Specific R_{DSON} values of different SPMs are given in Table 3.

4 Short-Circuit Robustness of SiC Power MOSFETs

SiC power devices exhibited reduced switching and conduction losses because it is capable of withstanding higher voltage stress with much lower R_{DSON}. Short-circuit test is used mostly in order to analyse the ruggedness of these power devices. In 2008, Y.Nakao et al. [102] investigated the short-circuit ruggedness of 4H-SiC MOSFET at 25^0C and 125^0C with 800 V dc bus voltage and + 20 V/ -10 V on/off state gate voltage. It was reported that at the destructive breakdown, temperature as high as $1400.^0$C was observed which can be computed using Wunsch-Bell formula as [102]

$$\frac{P}{A} = \sqrt{\pi.k.\rho.C_p}\left(T_m - T_c\right).t^{-1/2} \tag{11}$$

where A represents junction area, ρ represents density, P represents input power, C_p represents specific heat, T_m represents failure temperature, T_c represents initial temperature, k represents thermal conductivity and t represents time. t_{fail} (MOSFET destructive breakdown time length) of investigated 4H-SiC MOSFET was observed to be longer than 10μS which indicates its short-circuit safe operation potential for power electronics applications. In 2013, D.Othman et al. [103] et al. investigated the performance and ruggedness of 1.2 kV SiC MOSFET used in aircraft converters. Two SiC MOSFETs with different electrical characteristics namely SiC MOSFET-1 (R_{DSON} = 80 mΩ, Breakdown-voltage = 1200 V and Nominal current = 33 A) and SiC MOSFET-2 (R_{DSON} = 90 mΩ, Breakdown-voltage = 1200 V and Nominal current = 26 A) were subjected to short-circuit test. It was reported that when compared to SiC MOSFET-1, SiC MOSFET-2 sustained short-circuit operation until a t_{sc} (short circuit time) gate drive duration of 13μS without failure. In the same year, M.Riccio et al. [104] has investigated the electro-thermal instability of high voltage 1.2 kV SPM. It was reported that SPM was affected by hot spot formation (Fig. 14) which results in device damage and thermal runaway after a stressful short-circuit.

In 2015, C.Cheng et al. [105] compared the short-circuit robustness of SiC MOSFT and SiC BJT (Bipolar Junction transistor). Simultaneous short-circuit between drain and source and drain and gate as well as short-circuit between source and gate due to insulation degradation between source and gate were reported as the two major SiC MOSFET failure modes. In the same year, Z.Wang et al. [106] investigated the short-circuit capability of three commercial type 1200 V SiC MOSFET for DC bus voltage from 400 to 750 V and case temperature of 25^0C to 200^0C. It was reported that with 750 V DC bus voltage and 200^0C case temperature, commercial SiC MOSFET were able to withstand short-circuit current only for several microseconds.

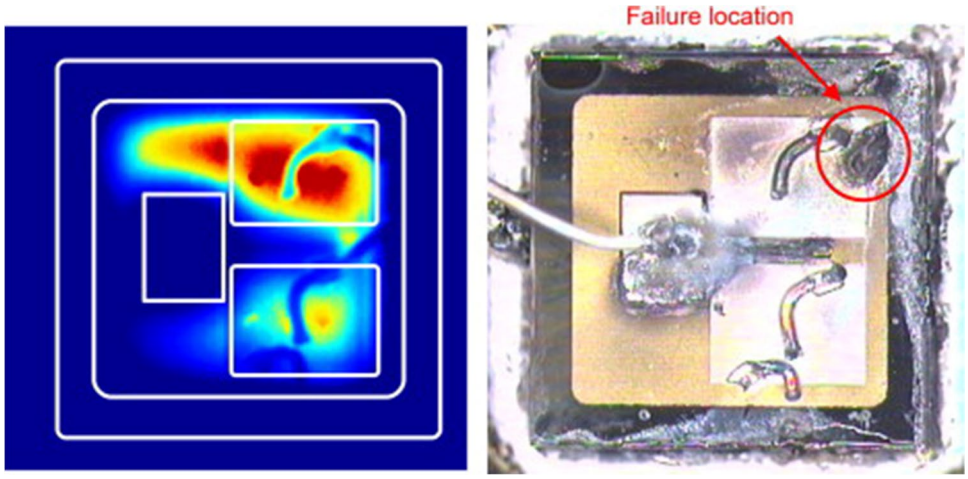

Fig. 14 IR Thermography of hotspot formation and subsequent device failure of a 1.2 kV SPM [104] (Reprinted from [104] with permission from Elsevier)

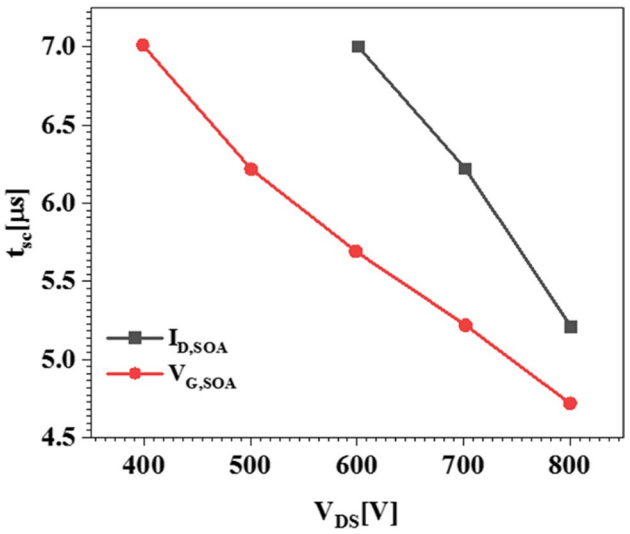

Fig. 15 SCSOA for 1.2 kV/180A SiC MOSFET power module at T = 25.^{0}C based on $V_{G,SOA}$ and $I_{D,SOA}$ criterion [107]

Gate-oxide damage due to high temperature or thermal runway induced due to thermal generation current was reported as a possible cause for short-circuit failure in SiC MOSFET. In 2016, P.D.Reigosa et al. [107] proposed a SCSOA (Short-Circuit Safe Operation Area) criterion for SiC MOSFET modules based on variation in gate source voltage and short-circuit current.

Two short-circuit safety criterion namely (a).gate voltage based criterion ($V_{G,SOA}$) and (b).short circuit current based criterion ($I_{D,SOA}$) has been formulated. When compared to $I_{D,SOA}$, $V_{G,SOA}$ was observed to be more restrictive (Fig. 15). In 2016, E.P.Eni et al. [108] investigated the short-circuit degradation of 10 A 10 kV 4H SiC MOSFET at a DC link voltage of 6 kV. Degradation of the device was reported as the short-circuit pulse length was increased and increase in R_{DSON} was observed as a result of continuous stressing. In 2018, M.D.Kelley et al. [109] investigated the single pulse avalanche energy tolerance of 10A 10 kV SiC MOSFET and the performance was compared with two 1.2 kV SiC MOSFETs. Energy density of 8.8 Jcm^{-2} was reported in 10 kV SiC MOSFET which is higher when compared to 7.4 Jcm^{-2} average value reported from two 1.2 kV SiC MOSFETs. In the same year, H.Du et al. [110] investigated the short-circuit performance and its effect on the static characteristics of 500 A 1.2 kV SPM with II generation planar technology. Two approaches namely (i) to apply the same short-circuit pulse once a static characteristic variation is observed and (ii) to increase the short-circuit pulse gradually even if there is a variation in static characteristics were adopted to analyse the degradation indicators that includes increase of gate-leakage current, increase of drain-leakage current, increase in on resistance and positive shift in V_{TH}. It was reported that both approaches confirm the degradation of gate structure with a few short-circuit test. Short-circuit current in SiC MOSFET can be effectively suppressed by introducing additional R_s (source resistance) in the source region (Fig. 16) [111]. It was reported that SiC MOSFET with additional R_s region exhibited low resistance in practical temperature range and high resistance in short-circuit. Also small C_{iss} (input capacitance) of SiC MOSFET with R_s region makes its appropriate for high speed devices.

In the year 2019, V.Soler et al. [112] fabricated 25 mm^2 large area high voltage SPM for 3.3 kV applications with boron doping process for gate-oxide formation. On investigating the electrical behaviour of the device, it was reported that the proposed device exhibited good short-circuit behaviour and enhanced robustness. t_{sc} of SiC Power MOSFET can be enhanced by employing BaSIC (Baliga Short Circuit Improvement Concept) EMM (Enhanced Mode MOSFET) topology. Enhanced t_{sc} of 11µS was reported in 1.2 kV SPM at 800 V drain bias with only 3.6% increase in on resistance using BaSIC EMM topology [113]. Trench gate SiC MOSFET has the advantage of higher cell density and faster switching speed. However

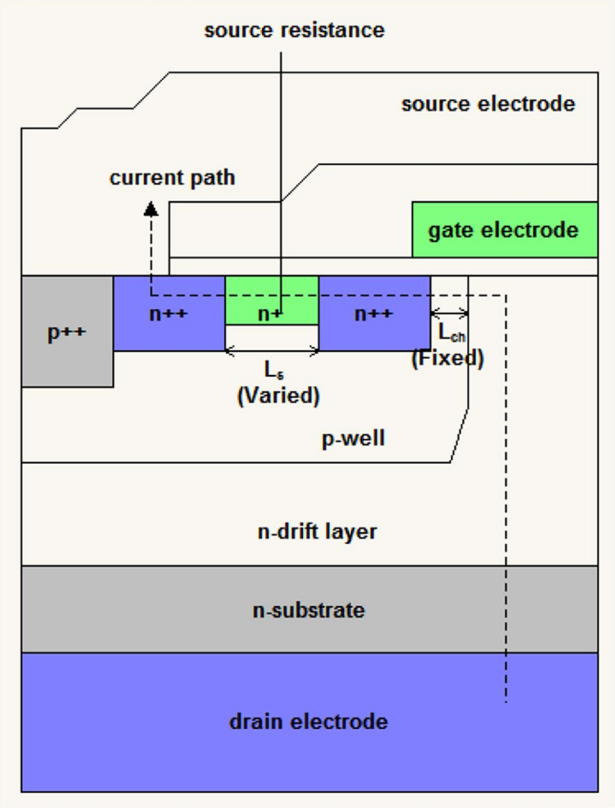

Fig. 16 Structure of SiC MOSFET with R_s region [111]

high electric field can cause damage to the trench-gate oxide since it extends deeply into the drift region. In 2018, R.Green et al. [114] compared the short-circuit behaviour of SiC trench MOSFET (80 mΩ, 1200 V) and SiC Planar DMOSFET. It was observed that SiC Trench MOSFET has smaller critical t_{sc} and less robustness when compared to SiC planar DMOSFET rated for 600 V DC bus operation with 16 V to 20 V V_{GS} value. In 2020, J.Wei [115] investigated the short-circuit behaviour of double trench SPM. It was observed that unlike traditional planar gate MOSFET technology, double trench devices gate-oxide breaks down during the short-circuit operation. In the year 2020, X.Liao et al. [116] reported a fault protection method for SiC MOSFET based on gate voltage. Very high fault response time less than 1 µS was reported with the proposed fault protection method and will be effective in ensuring safe and reliable operation of SiC MOSFET. In the year 2021, P.D.Reigosa et al. [117] compared the performance of 1.2 kV SPM having retrograde type channel doping profile (Fig. 17) with conventional 1.2 kV SPM. Enhanced short-circuit robustness was reported in SPM having retrograde type channel doping profile.

(SCWT) Short-circuit withstand time of different SiC Power MOSFETs are given in Table 4.

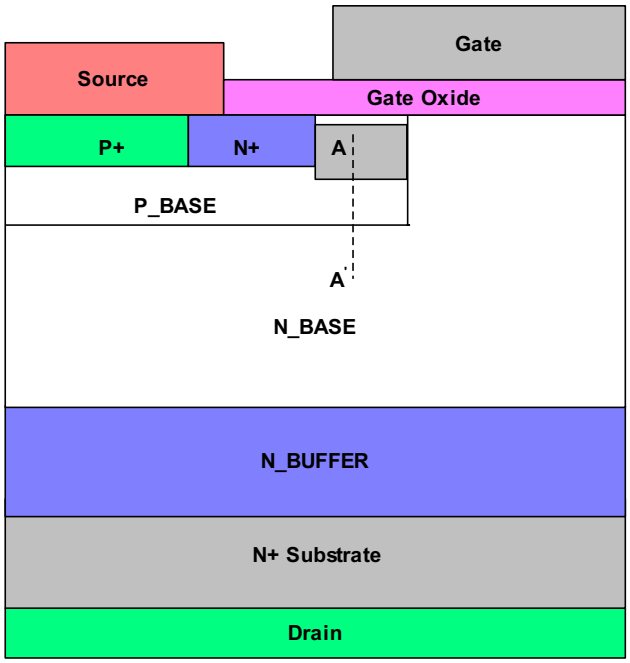

Fig. 17 Structure of SPM with retrograde channel doping profile [117]

5 Applications and Recent Developments of SiC Power MOSFETs

SiC MOSFETs are ideal for harsh switching and high frequency application because of its high switching speed. It is widely used in PV inverters, space electronics, accelerator-facilities and in nuclear power plants. It is also ideal

Table 4 An overview of SCWT values of different SPMs

Ref.	SCWT (µs)
[103]	13
[105]	10 to 15
[110]	12.4
[113]	11
[115]	19
[106]	80
[112]	15
[107]	7.2
[114]	6–8
[118]	7
[119]	4
[120]	18.7
[121]	7.9
[122]	23.5
[123]	14
[124]	15
[125]	11

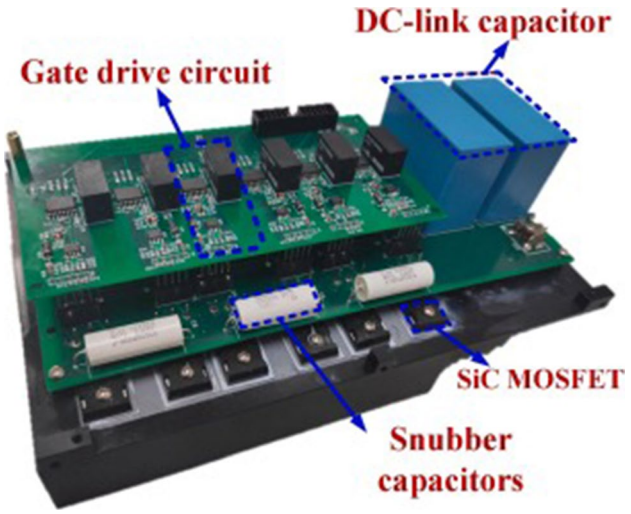

Fig. 18 SiC MOSFET based motor-drive inverters [141] (Reprinted from [141] with permission from Elsevier)

for harsh environments like aerospace, automotive and in wind turbine generators [126–139]. In 2017 X.Ding et al. [140] investigated the characteristics of Si IGBT and SiC MOSFET based EV traction system. By taking temperature effect into account both switching and conduction loss of SiC MOSFET was analysed. The conduction loss can be computed as [140]

$$P_{con} = I_{rms}^2 x R_{DS(on)} \quad (12)$$

where I_{rms} represents average value of current through MOSFET and $R_{DS(on)}$ represents on state resistance. It was observed that SiC MOSFET based EV traction system exhibited higher overall system efficiency (99.1%) when compared to Si based EV traction system. By using SiC MOSFET based next generation motor drives, EVs can become more efficient since the weight of motor drive can be reduced significantly. However for design optimization the power loss of SiC MOSFET need to be modelled accurately [140–144]. In 2021, X.Ding et al. [141] reported a switching-loss model for SiC MOSFET based on motor-drives in EVs. It was observed that when compared to conventional models, proposed switching loss model was highly accurate. Figure 18 shows the picture of SiC MOSFET based motor-drive inverters used in EVs.

WPT (Wireless Power Transfer) charging technology has been widely employed nowadays in EVs, mobile devices etc. SPMs find growing application in WPT systems. However effective junction temperature fluctuation suppression methods are required to reduce thermal failure as well as to enhance the reliability of WPT systems in EVs. In 2021, R.Wang et al. [142] proposed a novel SiC MOSFET junction temperature fluctuation tracking suppression strategy in WPT EV system. It was reported that with this proposed method 13.9^0C junction temperature fluctuations has be eliminated. In the year 2022, X.Chen et al. [143] investigated the steady state SOA of SiC MOSFET at room temperature (300 K) and cryogenic temperature (77 K). It was reported that the over current protection guidelines and SOA reported will be helpful in cryogenic MOSFET based applications.

6 Conclusion

SPMs have captured remarkable market attention as they meet most of the expected properties for high power and high temperature applications. SPMs find wide application in many fields of power electronics as they outperform their classical Si counterpart. However V_{TH} instability and gate-oxide degradation in SPMs affect its reliability. This long term reliability issues need to be addressed for extensive deployment of SPMs in industrial applications. DioMOS SPMs and SiC-CDMOSFET exhibited enhanced reliability and better device performance. Also the ability of SPMs to withstand stressful short-circuit and harsh conditions need to be improved further for its wide commercialization. Superior performance of SPM will make it emerge as an inevitable component in future power electronics applications.

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Data Availability NOT APPLICABLE.

Declarations

Ethics approval and consent to participate "All procedures performed in studies were in accordance with the ethical standards of the institutional and/or national research committee and with the comparable ethical standards."

"For this type of study, formal consent is not required."

Consent for publication Authors give consent for the publication of the Submitted Research article in Silicon.

Competing interests The authors declare that they have no known competing financial interests.

Conflicts of interest The authors declare that there is no conflict of interest reported in this paper.

Research involving Human Participants and/or Animals "Not Applicable".

Informed consent "Not Applicable".

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