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ORIGINAL PAPER

Investigation of Noise Characteristics in Gate-Source Overlap Tunnel Field-Effect Transistor

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Abstract

The analog circuit performance of tunnel field-effect-transistor (TFET) can be improved by implementing the concept of gate-source overlap. This paper investigates the impact of variation in gate-source overlap length on ON current, leakage current, capacitance and noise spectral density. Further the analysis has been carried out by excluding and including the effect of Gaussian traps. As the gate fully overlaps the source region a high ON current of $2.42*10^{-4}$ A/µm, low leakage current of $9.61*10^{-12}$ A/µm, I_{ON}/I_{OFF} ratio of 10^8, sub-threshold slope (SS) of 37 mV/dec are obtained. The optimised gate-source overlap length is 60 nm as it shows good electrostatic control and the maximum value of ON-current is achieved but the noise spectral density slightly increases for fully overlapped gate-source region.

Keywords Band-to-band tunneling (BTBT) · Hetero-junction · Gate-overlap · Noise analysis

1 Introduction

The rapid growth in wireless communication requires high level of integration and cost-effective technologies. The constant scaling of CMOS technology results in high speed metal oxide semiconductor field-effect-transistor (MOSFET) devices that can be used in analog RF applications [1, 2]. Nonetheless, extremely scaled device dimensions have to face a few challenges like short channel effects (SCEs), and punch through effect [3]. For low power applications, the conventional MOS devices can be replaced by tunneling mechanism based device i.e. Tunnel Field effect transistor (TFET) [4, 5]. Several experimental and simulation studies show that TFET is a suitable candidate for nanometer regime. TFET device is immune to SCEs, exhibit low leakage current and compatible to CMOS technology. Due to band-to-band tunneling (BTBT) mechanism, sub-threshold slope (SS) lower than conventional FET can be obtained in TFET devices [6]. Though, TFET devices have disadvantages like lower ON current, and ambipolar behavior [7, 8]. These issues can be resolved by using different structures like double-gate TFET [9], SOI-TFET [10], carbon-based TFETs [11], stacked source TFET [12], group III–V semiconductor-based TFETs [11], high-K dielectric-based TFET [13], hetero-junction TFET [14], and non-uniform body TFET [15].

The hetero-junction TFET based device shows five times reduction in power dissipation as compared to FinFET of the same dimensions [16]. The use of Ge material as source region though increases the ON current yet degrades the noise level [17]. For the Internet of Thing (IoT) applications, on-chip implementation of LTFET based analog circuits has gained the attention of researchers [18–20]. In general, the width of the device is used to improve the absolute drive current. But the increase in the device dimensions enhances the gate capacitances and reduces the output resistances. The low ON current in conventional TFET occurs as the BTBT remains independent of tunneling cross section area. The concept of gate-source overlaps in LTFETs is employed to increase the value of ON current without affecting the output resistance. Also, from the existing study it has been found that gate-source overlap length (L_{OV}) is very important parameter in LTFETs [21, 22]. The ON current increases linearly on increasing the L_{OV} because it enhances the increased area of BTBT [23, 24].

This paper is organized as follows: Section 2 describes the schematic diagram and device specifications. In Section 3 results and discussions is explained. The effect of variation in gate-source overlap length has been investigated using

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Synopsys TCAD tool. A detailed analysis of the devices has been carried out by including and excluding the effect of Gaussian traps. Finally, the important conclusions are drawn in Section 4.

2 Schematic Diagram and Device Specifications

The 2D schematic diagram of extended gate LTFET (EG-LTFET) with fully overlapped gate-source is shown in Fig. 1(a). For source regions, low band-gap material germanium (Ge) has been used as it offers higher tunneling in the on-state whereas silicon (Si) as drain region reduces the tunneling due to its high band-gap. The HfO_2 with dielectric constant value of 22 and Aluminum metal have been used as gate oxide and gate metal respectively. Furthermore, to verify the simulation setup accuracy, the simulation data of the proposed EG-LTFET device is calibrated against the experimental data [25], as shown in Fig. 1(b, c). It is observed that there is a good matching of both data, which certifies the validity of the selected models.

The optimized device dimensions of EG-LTFET with variable gate-source overlap lengths are tabulated in Table 1. The simulation of EG-LTFET devices has been performed using the Sentaurus TCAD tool. Band-gap narrowing model and Fermi Dirac statistics model have been activated for both proposed devices because of the high doping concentration [26]. The dynamic non-local BTBT model has been activated at the tunneling junction of both devices due to the tunneling probability of the carriers [27]. The Shockley-Read-Hall (SRH)

Table 1 Proposed device dimensions

Parameters	Symbol	Values	Units
Gate oxide thickness	t_{ox}	2	nm
Drain length	L_d	26	nm
Drain height	H_d	15	nm
Gate length	L_g	14	nm
Gate-source overlap	L_{OV}	Variable	nm
Gap between source edge and gate oxide	L’	3	nm
Gap between sources	G	5	nm
Source thickness	H_s	3	nm
Number of sources	N	4	–
Length of source	L_s	57	nm
Source doping concentration	N_s	4×10^{19}	cm^{-3}
Drain doping concentration	N_d	1×10^{18}	cm^{-3}
Channel doping concentration	N_{ch}	1×10^{17}	cm^{-3}
Gate work function	ϕ_m	4.3	–

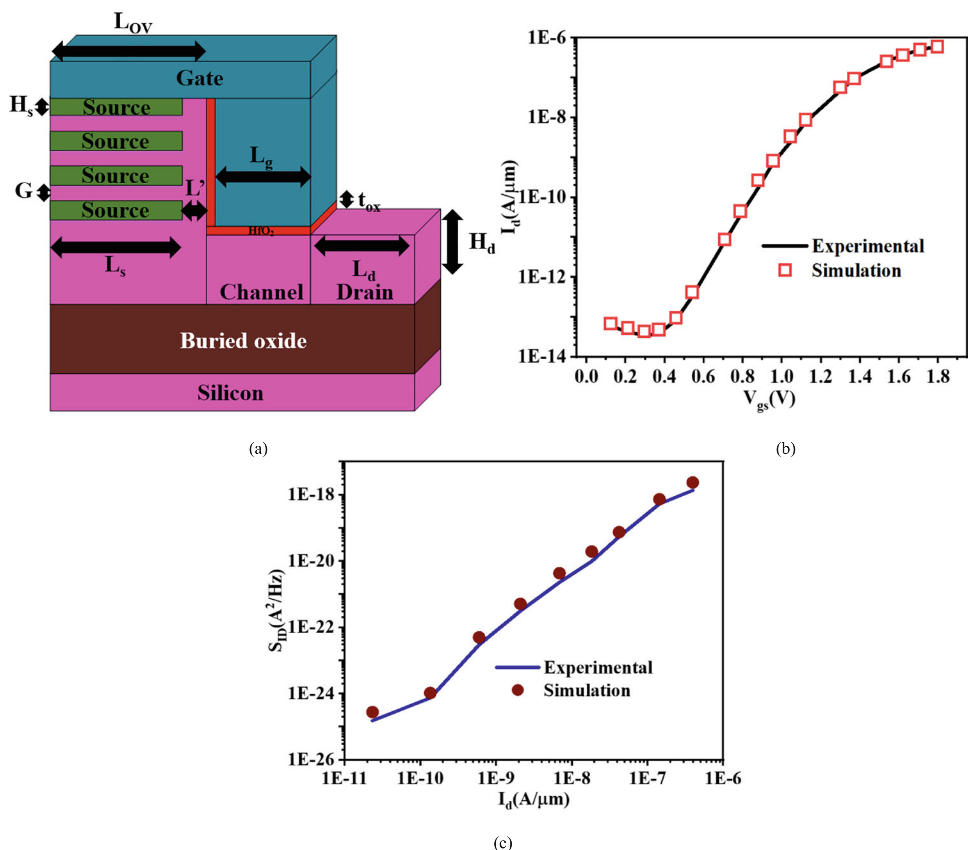


Fig. 1 (**a**) Schematic diagram (**b**) Calibrated transfer characteristics curves [25] (**c**) Calibrated Noise spectral density curve [25] of the proposed EG-LTFET

recombination model has also been incorporated. To account for the effect of doping on the mobility carriers, the doping-dependent mobility model has been enabled. Noise model of McWhorter's for free carrier fluctuations and Hooge's model for mobility fluctuations has been used for the investigation [28, 29].

3 Results and Discussion

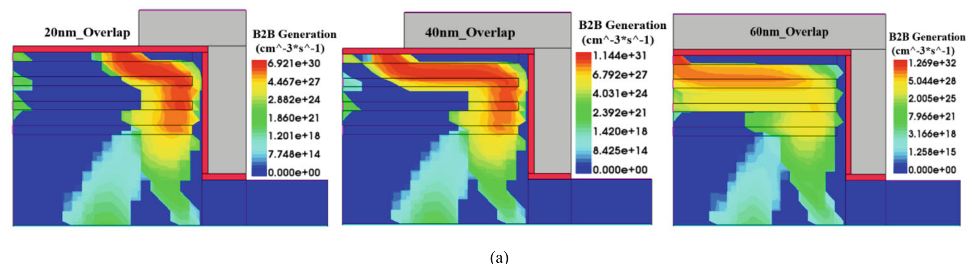
The simulation study of proposed EG-LTFET device is carried out in Sentaurus TCAD tool and device dimensions has been optimised. In this section the effect of variation of gate-source overlapping length on the DC, AC and noise analysis has been studied.

3.1 DC Analysis

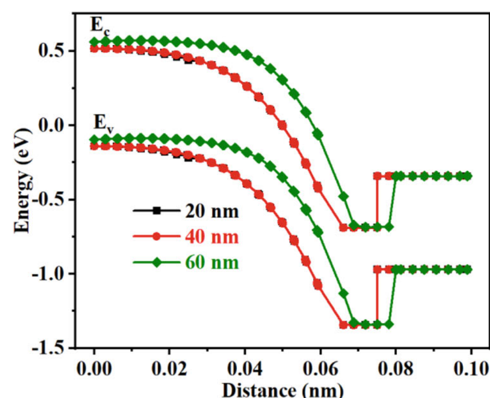
Figure 2(a) shows the contour plots of obtained BTBT rate for three different gate-source overlapping lengths. It is very evident that the electric field is very intense at the sharp source corner than the flat source region this is because of the field crowding effect [30]. Moreover as the gate-source overlap is increased, the tunneling rate increases and as the gate fully overlaps the source region, maximum tunneling is achieved. The energy band diagram for three different gate-source overlap values is shown in Fig. 2(b). As the gate-source overlapping length is increased, the variation in the position of E_c and E_v occurs.

Figure 3(a) shows the transfer characteristics of the proposed EG-LTFET. The analysis of transfer characteritics for three different gate-source overlapping lengths i.e. 20 nm, 40 nm, and 60 nm has been carried out at V_{ds} = 0.4 V. The effect of considering the traps and not considering the traps on drain current has been observed. The acceptor type Gaussian traps in Si/HfO_2 and Ge/HfO_2 interface with the value of *energymid* (peak of the Gaussian traps) is 0.55 eV for Si, 0.33 for Ge, with EnergySig of 0.1 eV and Maximum concentration of traps in a Gaussian distribution of 10^{12} eV^{-1} cm^{-2} is included. On changing the gate-overlap from 20 nm to 60 nm, it has been found the maximum ON current is achieved when the gate fully overlaps the source region. It is clear in the contour plot (Fig. 2(a)) that as the overlapping length increases, the BTBT tunneling increases and as the gate completely overlaps the source, maximum BTBT rate is achieved hence maximum ON current is obtained. It is clearly shown in the Fig. 3(a) that on adding the traps at source-gate oxide interface and channel-gate oxide interface, the ON current reduces and leakage current increases slightly. The trap effects the carrier tunneling and hence the ON current slightly decreases. The EG-LTFET with 60 nm overlap exhibits high ON current of $2.42*10^{-4}$ A/μm, low leakage current $9.61*10^{-12}$ A/μm, I_{ON}/I_{OFF} ratio of 10^8 and SS of 37 mV/dec. Hence the optimised gate-source overlap is 60 nm as it shows good electrostatic control and the maximum value of ON current is achieved.

The output charactertistics of EG-LTFET are obtained at V_{gs} = 1.0 V by varying the V_{ds} from 0 to 2.5 V. At low values of V_{ds}, the SRH generation-recombination (GR) conduction mechanism dominates. But as the V_{ds} is increased, the effect of tunneling increases and it increases until the I_d saturates.



(a)



(b)

Fig. 2 Proposed EG-LTFET (**a**) BTBT contour plot for different L_{OV} (**b**) Energy Band diagram

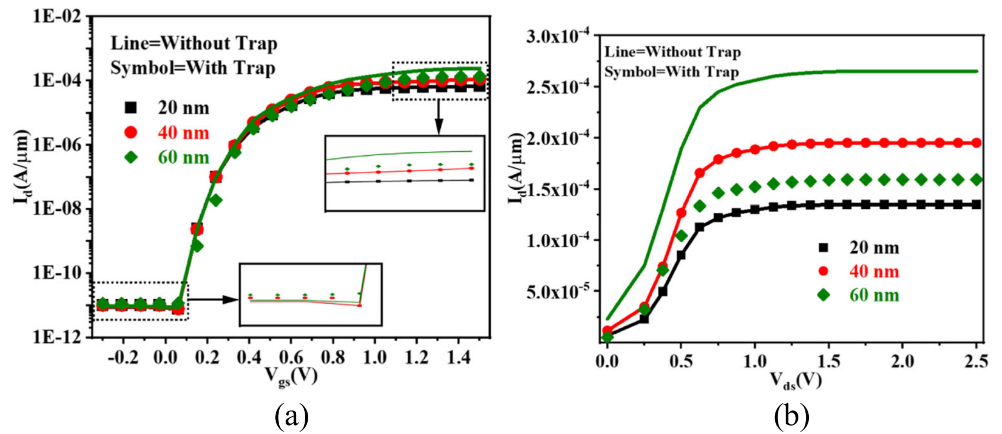


Fig. 3 Proposed EGLTFET with varying gate-source overlap (**a**) Transfer Characteristics (**b**) Output Characteristics with and without traps

The current saturation occurs because BTBT tunneling rate reaches at its maximum value. Also, higher V_{gs} value induces higher electric field and as a result I_d increases. The fully overlapped EG-LTFET have improved ON current and SS as compared to the other two cases. The effect of including Gaussian traps can be clearly seen from the Fig. 3(b).

3.2 AC Analysis

The electrical characteristic of the device relating the change in output current of the device to the change in input voltage is known as transconductance (g_m). The transconductance can be expressed by eq. 1 [31]:

$$g_m = \frac{\partial I_d}{\partial V_{gs}} \tag{1}$$

The transconductance of the proposed EG-LTFET device for three different gate-source overlapping lengths values is shown in Fig. 4(a). The transconductance depends upon the slope of I_d-V_{gs} from which the switching speed of the device can be determined. High value of g_m depicts high switching speed of device. It is very clear from the results for fully overlapped gate-source region, maximum value of g_m is obtained. Hence, high switching speed can be obtained.

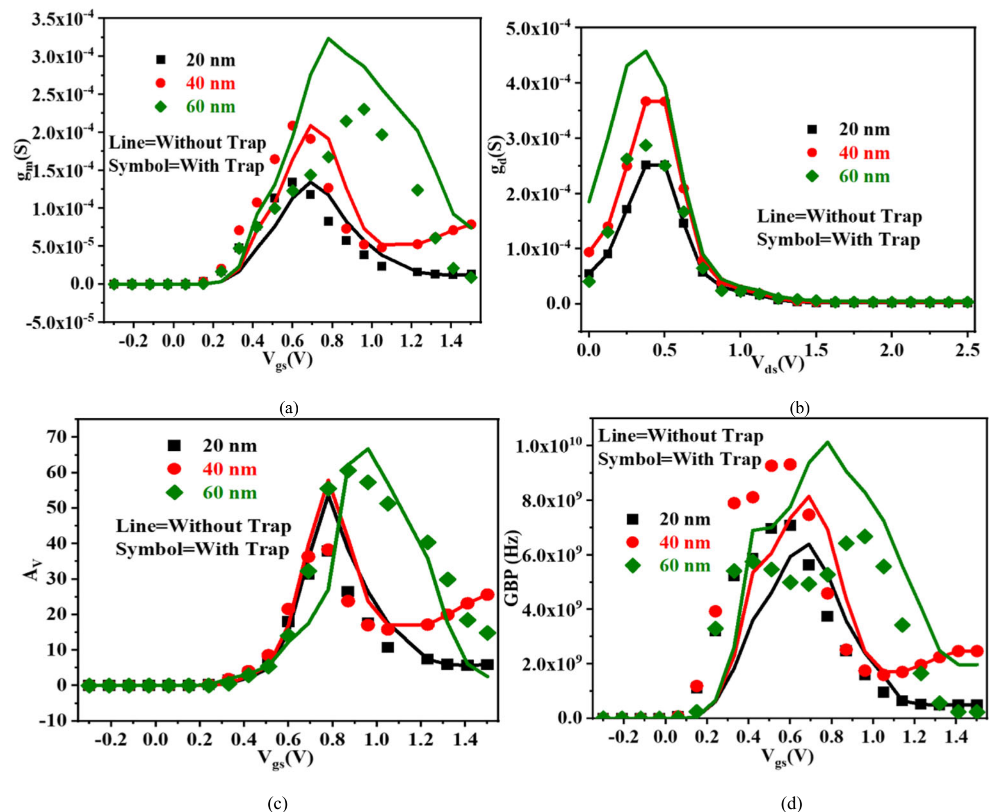
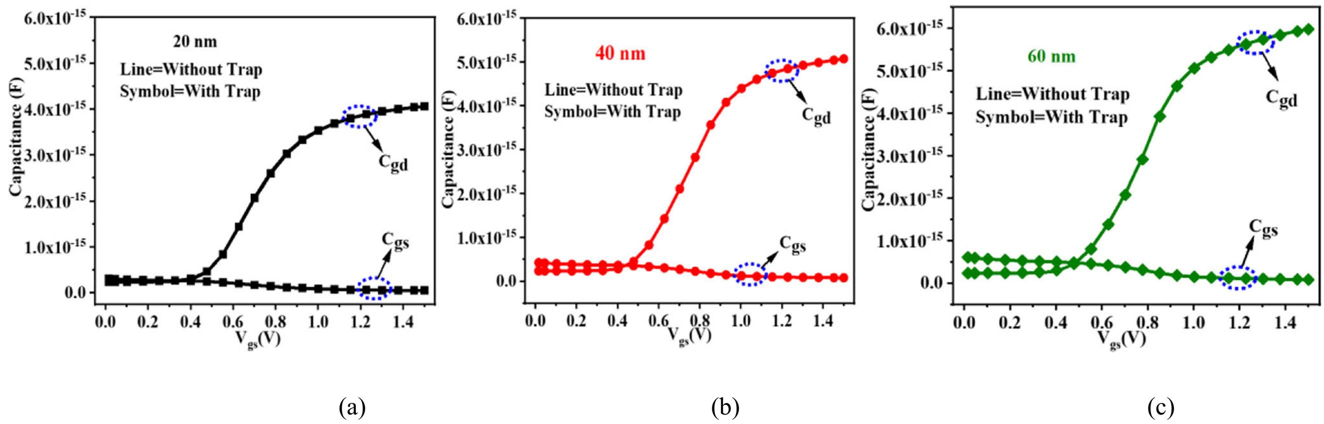


Fig. 4 Proposed EGLTFET with varying gate-source overlap (**a**) g_m (**b**) g_d (**c**) A_V (**d**) GBP with and without traps



(a) (b) (c)

Fig. 5 Simulated C_{gs} and C_{gd} of Proposed EGLTFET for (**a**) L_{OV} = 20 nm (**b**) L_{OV} = 40 nm (**c**) L_{OV} = 60 nm with and without traps

The output conductance (g_d) of the proposed EG-LTFET device is shown in Fig. 4(b) and can be expressed by Eq. 2 [31]:

$$g_d = \frac{\partial I_d}{\partial V_{ds}} \quad (2)$$

The maximum value of g_m and g_d is achieved for gate-source overlap of 60 nm. The effect of Gaussian traps on g_m and g_d is clearly shown in the results. The intrinsic voltage gain of TFET is the ratio of transconductance to output conductance and can be written as [32]:

$$A_V = \frac{g_m}{g_d} \quad (3)$$

Figure 4(c) clearly depicts that for the overlapping length of 60 nm, maximum intrinsic voltage gain of EG-LTFET is obtained. Another important parameters is gain bandwidth product (GBP). The GBP is calculated at fixed static gain and expressed as [32]:

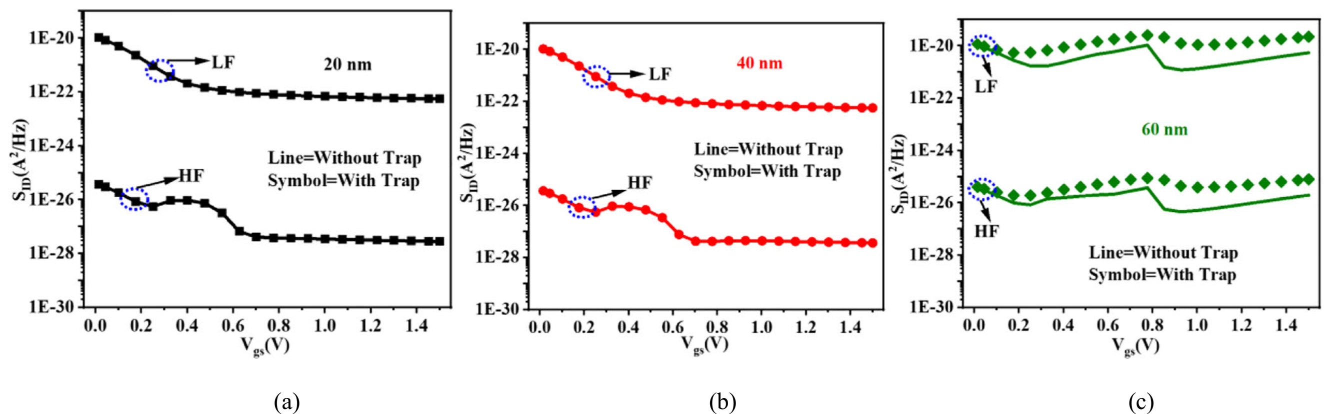
$$GBP = \frac{g_m}{2\pi C_{gd}} \quad (4)$$

Figure 4(d) shows the GBP curve obtained for different overlapping lengths. GBP directly depends upon g_m, and maximum GBP has been obtained for overlapping length of 60 nm.

For AC analysis of the device, the investigation of capacitance is highly desired. Figure 5(a, b and c) shows the dependence of gate-drain capacitance (C_{gd}), and gate-source capacitance (C_{gs}) on V_{gs} for L_{OV} = 20 nm, 40 nm and 60 nm. It is observed that on increasing V_{gs}, C_{gd} increases rapidly and C_{gs} changes slightly. The sudden rise in C_{gd} is due to the accumulation of electrons at the gate-channel interface [33]. In L_{OV} = 60 nm, the overlapping area increases hence increases the capacitance. The effect of introducing traps has not been seen in the capacitance curve of the device.

3.3 Electrical Noise Analysis

The detailed investigation of electrical noise analysis in terms of: drain current noise spectral density (S_{ID}) and noise voltage spectral density (S_{vg}) at low frequency (1 MHz) and high frequency (1 GHz) using TCAD tool is presented. All the variation has been done at fixed drain voltage (V_{ds}) of 0.4 V



(a) (b) (c)

Fig. 6 S_{ID} vs. V_{gs} of (**a**) 20nm_Overlap (**b**) 40nm_Overlap (**c**) 60nm_Overlap with and without traps at LF and HF

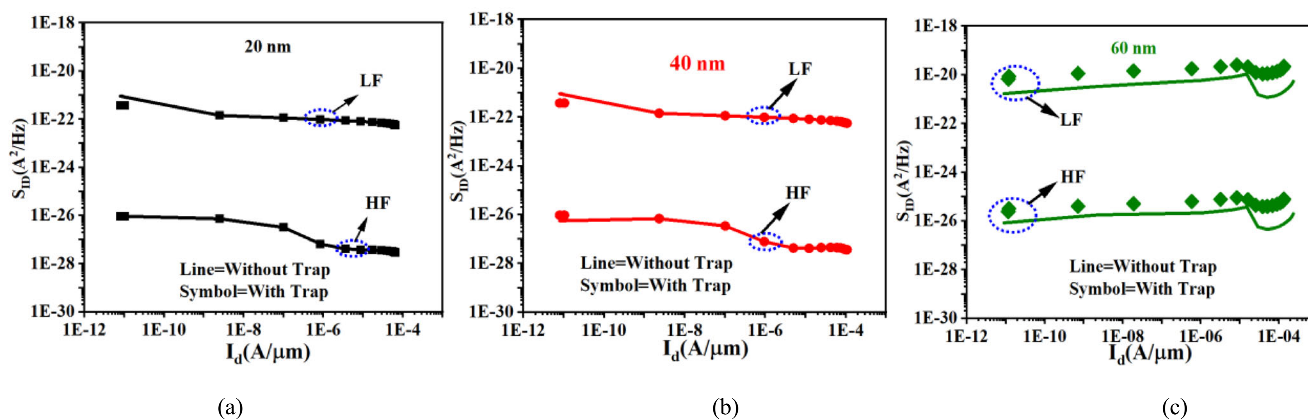


Fig. 7 S_{ID} vs. I_d plots of (**a**) 20 nm (**b**) 40 nm (**c**) 60 nm with and without traps at LF and HF

and by including and excluding the effect of traps. The acceptor type Gaussian traps in Si/HfO_2 and Ge/HfO_2 interface with maximum concentration of 10^{12} eV^{-1} cm^{-2} is included.

3.3.1 Current Noise Spectral Density (S_{ID})

Figure 6(a, b and c) shows the results plotted for S_{ID} vs. V_{gs} of EG-LTFET for three different overlapping lengths respectively at V_{ds} of 0.4 V. At both LF and HF, current noise spectral density for overlapping lengths of 20 nm and 40 nm is almost equal but as the gate fully overlaps the source, the noise in the device increases. Also, the effect of Gaussian traps is only observed when the gate fully overlaps the source region. For 20 nm and 40 nm overlapping lengths, no variation in the noise spectral densities is observed. As the overlapping length increases, the more number of traps get introduced at the interface hence the effect of traps is observed in the noise spectral density. The occurrence of electrical noise is attributable to fluctuations in the number of charge carriers in the channel. At lower gate voltage, the trapping and de-trapping of thermally generated carriers is high. As gate voltage increases, the generation of carriers due to BTBT increases. The trapping, and de-trapping also increase but their contribution is suppressed by enhanced BTBT at higher gate voltage [34]. Thus, S_{ID} at high V_{gs} increases comparatively the low V_{gs}. The drain current noise follows an inversely proportional relationship with frequency; hence, it has reduced values at HF than at LF [35].

3.3.2 S_{ID} Vs I_d

Figure 7(a, b and c) shows the results plotted for normalised S_{ID} vs. I_d of EG-LTFET with traps and without traps. At high frequencies, the less effect of noise sources is observed as compared to low frequency for all the cases because drain current noise follows an inversely proportional relationship with frequency; hence, it reduces the values at HF than LF [35].

3.3.3 Noise Voltage Spectral Density (S_{VG})

Figure 8 shows the results are plotted for S_{vg} vs. V_{gs} of EG-LTFET by taking into account the effect of traps and without traps at LF and HF. The overall effect of noise is considered for the analysis. The noise voltage spectral density is high for low gate voltages but as the applied gate voltage is increased, the noise voltage spectral density decreases. The noise voltage spectral density follows the same trend as current noise

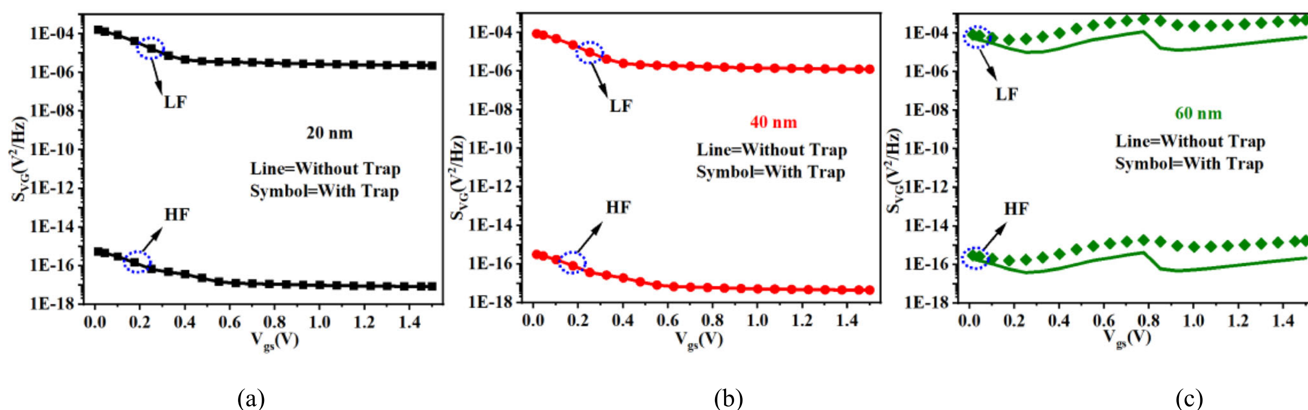


Fig. 8 S_{VG} vs. V_{gs} of overlapping lengths (**a**) 20 nm (**b**) 40 nm (**c**) 60 nm with and without traps at LF and HF

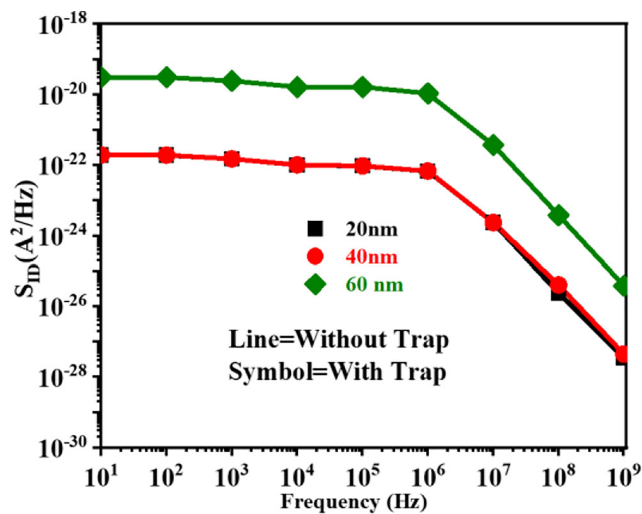


Fig. 9 S_{ID} vs. frequency of EG-LTFET for with trap and without trap

spectral density. At low V_{gs}, noise voltage spectral density is high. Because at low gate voltage the trapping-detrapping of thermally generated carriers is high but as the V_{gs} is increased, the BTBT rate dominates and the effect of trapping-detrapping reduces. Hence, noise voltage spectral density reduces for high V_{gs}. Moreover, the effect of Gaussian traps is more pronounced for the overlapping gate length of 60 nm than the other two cases. At LF, the noise voltage spectral density for EG-LTFET is comparatively higher than at HF because of the inverse dependence of noise spectral denisty with frequency.

3.3.4 Dependence of Noise Current Spectral Density on Frequency

Figure 9 depicts the change in drain current noise spectral density of proposed EG-LTFET for different frequency range. The analysis for all the three overlapping lengths has been carried out at fixed V_{ds} = 0.4 V and V_{gs} = 1.0 V by including and excluding the effect of traps. Based on the obtained results, it can be said that at LF the drain current noise spectral density is high but as we move to HF, the effect of noise decreases. The noise shows descending slope due to inverse dependence on frequency.

4 Conclusion

In this paper, a heterojunction EG-TFET by varying gate-source overlap length is reported. The DC analysis, AC analysis, and electrical noise analysis has been carried out by including and excluding the effect of Gaussian traps. For all the three cases, the maximum ON current is obtained when the gate fully overlaps the source region. This happens because of the increased area of BTBT [23]. The Gaussian trap does not affect the noise spectral density for 20 nm and 40 nm overlapping lengths but the variation is evident for the overlapping length of 60 nm. As the gate-source overlapping length increases, the more number of traps get introduced at the interface hence the effect of traps is observed in the noise spectral density. Similarly, at LF, the less effect of noise sources is observed than at HF because drain current noise follows an inversely proportional relationship with frequency.

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Authors' Contributions All the authors did equal contribution in the manuscript for the possible publication.

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Declarations

Ethics Approval Not Applicable.

Consent to Participate Not Applicable.

Consent for Publication All authors are giving consent for publication.

Competing Interests Not Applicable.

Disclosure of Potential Conflicts of Interest Not Applicable.

Research Involving Human Participants and/or Animals Not Applicable.

Informed Consent Not Applicable.

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