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ORIGINAL PAPER

Performance Evaluation of FinFET Device Under Nanometer Regime for Ultra-low Power Applications

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Abstract

For Ultra Large-Scale Integration (ULSI), the most promising device is multi gate Fin Field Effect Transistor (FinFET), as it offers reduced leakage current and better short channel performance. Modern design methodologies for 5 nm node NMOS FinFET transistors are examined in this paper to realize low power and low off state current (I_{off}) needs. Changing the punch through stop implant dose, source and drain junction placement, gate work function, Drain Induced Barrier Lowering (DIBL), and sub-threshold slope in combination with cut-in voltage yields the Ioff and Ion (on state current). Source drain expansion design, Fin doping concentration, and gate work function selection are exploited such that a FinFET device provides the requirements of low power and ultra-low power transistors.

Keywords DIBL · FinFET · Integrated circuits (IC) · Low power (LP) · MOSFET · Short channel effects (SCEs) · Sub-threshold slope · Nanometer regime

1 Introduction

In order to reduce area and power compared to vacuum tubes and need for a solid-state switch such as Si/SiO_2 based MOSFET was invented [1]. A lot of efforts have been carried out to reduce the device dimensions, improve packing density, and lower fabrication cost. Reduced transistors decreased chip cost per transistor while simultaneously increasing operational frequency. Continuous reduction of transistor size increases off current (I_{off}), higher on current (I_{on}) which made the designer to change the structure of transistor such as FinFET to improve short channel effects. Now a days billions of transistors are fabricated on integrated circuits (IC) obeying Moore's law [2]. Scaling of device is done to dwindle the area of device and power dissipation. In order to maintain Moore's law, Robert H. Dennard et al. proposed group of scaling constraints for lengthy devices in order to minimize negative impacts on its attributes [3–5]. To retain device performance and electrostatic stability, transistor scaling requires scaling channel length, oxide thickness, source and drain junction route, channel doping concentration, power supply, channel width, and connectivity. The channel length enhances the same order of magnitude as the source and drain-depletion layer thickness as the transistor size is reduced. The Short Channel Effect decreases gate control and generates unwanted consequences like DIBL, Punch-through, Cut-in voltage roll off, GIDL (Gate induced drain leakage), a band-to-band tunneling technique at heavily doped drain and gate intersection area etc. [6].

The use of a source/drain stressor and silicide in planar MOSFETs with a high-k dielectric and a metal-gate has resulted in a significant gate leakage current fall and mobility enhancement [7]. Planar MOSFETs with sub 30 nm gate length have weak sub threshold swing (> 40mv/dec) and substantially more off current (> 100nA/m), despite severe technological obstacles. As a result, planar bulk MOSFET scaling is getting increasingly channeling. The transistor's characteristics length is a metric of the channel's electrostatic control

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[8]. It reflects the distance between the drain and the body's channel, or the degree of control the drain has over the channel, since both the gate and the drain strive for to control [9]. The usual length of a multi-gate device is given by

$$\lambda_N = \sqrt{\frac{\epsilon_{Si}}{N\epsilon_{ox}} t_{ox} t_{Si}} \quad (1)$$

Here, N represents number of effective gates, ε_{Si} is the silicon permittivity, and ε_{ox} is thickness of gate-oxide, tox is oxide thickness, and tsi is the thickness of silicon. The first FinFET, depleted lean channel transistor (DELTA) is distinguished by the production of a huge single crystal employing selective oxidation, resulting in a fine-quality single Si crystal [10]. The DELTA FinFET gate effectively controls channel potential on both sides, resulting in significantly improved device characteristics. The surface of the Si-vertical Fin acts as a channel, allowing current to flow in a straight line parallel to the wafer surface [11]. Poly Si film is liberally applied to Si-fin. FinFET scaling and increased drive current for next generation devices were achieved using various gate work function designing and thinner gate oxide, thanks to the development of more efficient FinFET technologies.

Figure 1 shows the diagram of a tri-gate FinFET in which the gate control is increased by wrapping the gate around the channel as a Fin. GIDL is observed to be the preventive factor in obtaining ultra-low (< 100pA/μm) values during I_{off}. According to many studies elaboration of path will decrease the GIDL. Increasing the cut-in voltage of the transistor then Ioff value can be decreased. Multi-cut-in voltage strategies such as work function, design, SD extension region, and enhanced gate length have developed as a result. Longer gate switches for LP and ULP transistors reduce leakage and short channel effects (SCE). Cut-off frequency and analogue figure of merit, on the other hand, are disadvantages (FOM). Short channel effects (SCEs) and off current have been predicted to be mitigated using various strategies such as HALO implant graded channel design. To mention a few benefits, the FinFET offers well-suppressed short-channel effects, a near-ideal value for sub-threshold swing (70 mV/dec), and a small cut-in voltage roll-off.

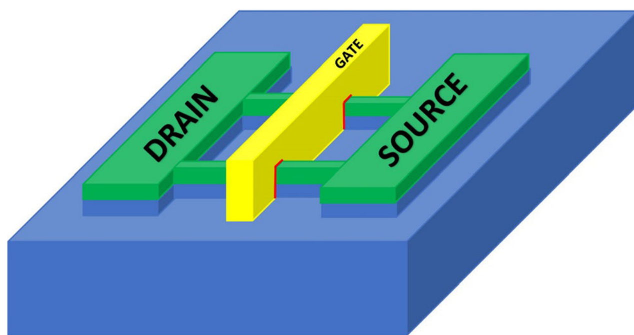

Fig. 1 Structure of FinFET

2 Model Development

The Generalized compact models of drain current experienced in non-planar multi-gate FinFET with different cross-sections such as rectangular, Re-TG, double gate, cylindrical, and triangular gates have been anticipated for long channel transistors. Here, a compact model based on analytical charge is developed for the drain current in short-channel rectangular trigate FinFET, is effective in all setup regions. The physical effects are also included in this model such as quantum mechanical effects, channel length modulation, series resistance, short channel effects, and field dependent mobility. In addition to that, the gate oxide capacitance C_{ox} and channel-capacitance C_{si} per unit area are same as planar devices, $C_{ox} = \varepsilon_{ox}/t_{ox}$ and $C_{si} = \varepsilon_{si}/W_{fin}$, where ϵ_{ox} is dielectric permittivity of silicon dioxide and ε_{si} as dielectric permittivity of silicon [12]. In FinFET compared to graded channel double gate MOSFET, short channel effects are improved.

In a classic planar FET with a long channel, the cut-in voltage is self-regulating of drain voltage because of appearance of bottleneck from drain contact during channel formation and it is shielded electrostatically from the drain by the combination of the gate and substrate. On the contrary in short channel transistors, the drain is nearer to gate, so bottleneck will be opened by high drain voltage turning on the transistor prematurely. In the sub cut-in region (Weak inversion), the effects of DIBL is visible in the initial phase as the channel is reduced, then as a simple conversion of the gate bias vs. sub cut-in current curve with drain voltage changes which can be altered as drain bias replaced with cut-in voltage. In addition to this, the slope of current vs. the gate bias curve is decreased at shorter lengths as large change in gate bias is required to bring the same change in drain current. The gate does not succeed to turn the device off, in the case of extremely short lengths and Conversion of these effects as cut-in adjustment cannot be done. Even in active mode, DIBL influences the current versus gate bias curve, since the current rises due to drain bias, lowering the MOSFET's output resistance. This increase is in addition to the effect of conventional channel length modulation on output resistance, and it cannot continually be changed as a cut-in alteration. In general, DIBL is given by,

$$DIBL = \frac{-V_{thDD} - V_{thlow}}{V_{DD} - V_{Dlow}} \quad (2)$$

Here, V_{thDD} is supply voltage cut-in volage measure and V_{thlow} is low drain cut-in voltage measured typically at 0.05 or 0.1 V. The supply voltage at the drain is given by V_{DD} and the low drain voltage is given by V_{Dlow}.

The gate voltage controls the behavior of the drain current, however it delivers an exponentially falling current in the sub cut-in area. As a result, a graph of gate voltage vs. drain

current in the MOSFET operating regime with source, bulk, and drain voltages unchanged will show essentially log linear behaviors. The slope of this curve (the subcut-in slope) is the inverse value of the sub cut-in swing S_{sth} represented as,

$$S_{Sth} = \ln(10)\ \frac{KT}{q}\left(1 + \frac{C_d}{C_{ox}}\right) \tag{3}$$

Here, C_d=depletion layer capacitance, C_{ox}=oxide capacitance, KT/q = thermal voltage. Fast transition of on and off current states are being exhibited by a device characterized by steep subcut-in slope. Sub cut-in slope (swing) is given by,

$$S = \left(d(log10I_{ds})/dV_{gs}\right) - 1 \tag{4}$$

Heavy body doping is not considered a viable method for adjusting the Cut-in voltage of scaled MOSFETs because it reduces mobility and thus speed. The cut in voltage can be conveyed as,

$$V_{th} = V_{FB} + 2_F + \frac{Q_D}{C_{ox}} + V_{in} \tag{5}$$

$$V_{FB} = \frac{_{MS} - Q_{ox}}{C_{ox}} \tag{6}$$

$Ø_{MS}$ denotes the metal semiconductor work function between the gate electrode and the semiconductor, $Ø_F$ denotes the fermi potential, Qd denotes the depletion charge in the channel, and Qss denotes the charge in the gate dielectric. Vin is the supplementary surface potential needed to induce inversion and reach the channel's cut-in point. By choosing the correct gate material, we may fine-tune the work function. Ta, TaSiN, and Mo have taken the place of the poly gate.

FinFET-based add and shift multipliers for wireless communication show minimal static power dissipation when employed in digital signal processors at various technology nodes. FinFET-based high-performance BZFAD multipliers for IoT applications have exhibited lower dynamic power dissipation at lower technology nodes, which is useful in cyber security and artificial intelligence. Thus, FinFET device is effective device for future devices. Hence, In the current study we have evaluated performance of FinFET device at deep submicron region. Taken care of devices in nanometer regime can help the researchers to highlight the same for many applications. Also, FinFET-based devices have explored many researchers in variety of applications [13–16].

3 Results and Discussions

The results obtained are for gate lengths of 5 nm, 10 nm, 20 nm with channel doping of Na = 1.45×10^{10}, source/drain doping = $N_d = 1 \times 10^{19.4}$ with variable dimensions of fin as follows.

The drain current obtained for the proposed 5 nm model is 447 micro Amperes, as shown in Fig. 2. As the length of channel of FinFET reduced from 20 nm to 5 nm, Ion current increased and I_{off}, decreased, DIBL increased, subcut-in slope increased, V_t cut-in decreased, I_{on}/I_{off} increased thus shown better performance in the analytical model of current which is obtained in simulation results of MATLAB by varying length of channel, oxide thickness, height of the fin, acceptor concentration and donor concentration.

The values which mainly contribute to analyzing characteristics of a FinFET device are mainly I_{on} current and I_{off} current. The values that are obtained for the 20 nm with various gate voltages and 0-1 V of drain voltages are shown in Figs. 3 and 4.

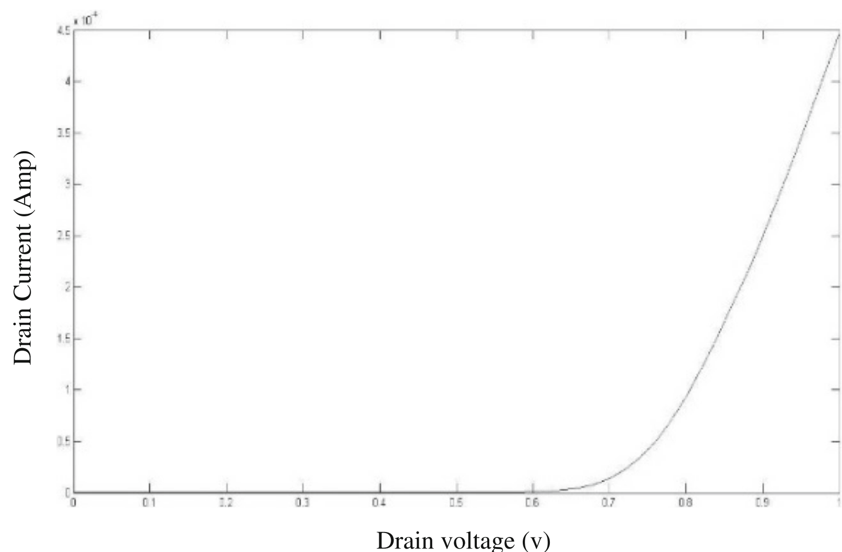

Fig. 2 Ion current value for 5 nm FinFET

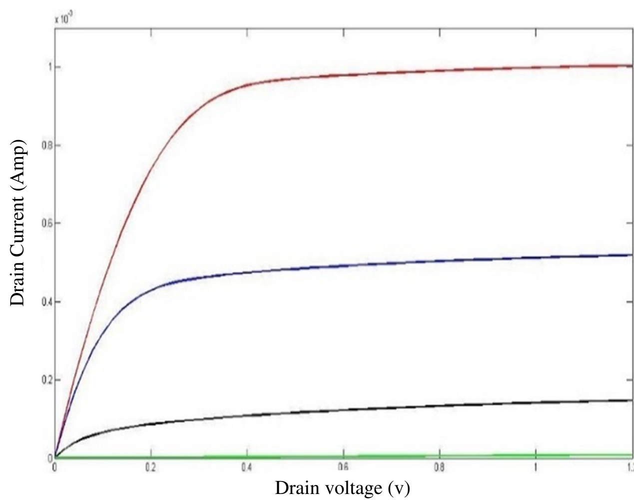

Fig. 3 I_{on} Vs. V_{gs} for 20 nm FinFET

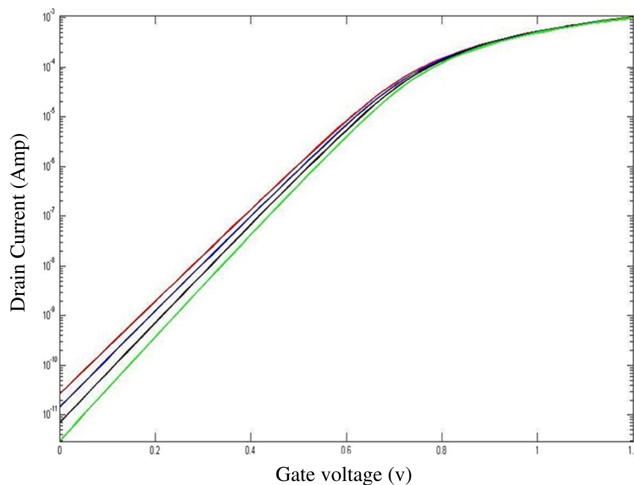

Fig. 4 I_{off} current value for 5 nm FinFET with various V_{gs} values

The above values show the on-current of 20 nm FinFET with $N_a = 1.45 \times 10^{10}$, $N_d = 1 \times 10^{19.4}$ /cm^3, ni = 2.4×10^{13}/cm^3, $W_{fin} = 15 \times 10^{-9}$ m, $H_{fin} = 25 \times 10^{-9}$ m. This can be made sure with considering off-current of the proposed FinFET with same inputs as of FinFET device as shown in Table 1 for the parameters of FinFET as stated in Table 2.

The various analytical model results like DIBL, sub cut-in, Cut-in voltage (V_t), and I_{on}/I_{off} plot for 5 nm, 10 nm, 20 nm FINFET are shown in Figs. 5, 6, 7 and 8 respectively. DIBL is low as we go deeper in the sub-nano meter regime as depicted in Fig. 5 and the variation is quiet low which will surely help the transistors to work even ultra-low power. Figure 6 represents sub threshold value of proposed FinFET at deep sub-nm regime. As ultra-low power transistors need high subthreshold

Table 1 FinFET simulation results for 20 nm and 5 nm FinFETs

Parameter	20 nm	5 nm
Ion	1000µA	1700µA
DIBL(mV/V)	55	80
Subthreshold slope(mV/decade)	86	60
Vt(V)	0.22	0.22
Ion/Ioff	15×10^6	15.5×10^6

Table 2 Parameters for FinFET proposed model

Sl. No	Parameters	20 nm	10 nm	5 nm
1	Length of gate	20 nm	10 nm	5 nm
2	Height of Fin	25 nm	15 nm	8 nm
3	Width of Fin	15 nm	5 nm	1 nm
4.	Acceptor concentration	1.45×10^{10}	1.45×10^{10}	1.45×10^{10}
5.	Donor Concentration	$10^{19.4}$	$10^{19.4}$	$10^{19.4}$
6.	Thickness of oxide	1 nm	1 nm	1 nm

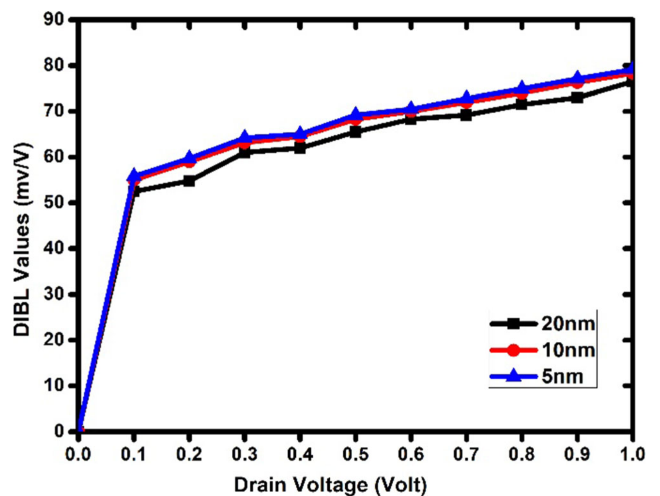

Fig. 5 DIBL for 5 nm, 10 nm, 20 nm FinFET

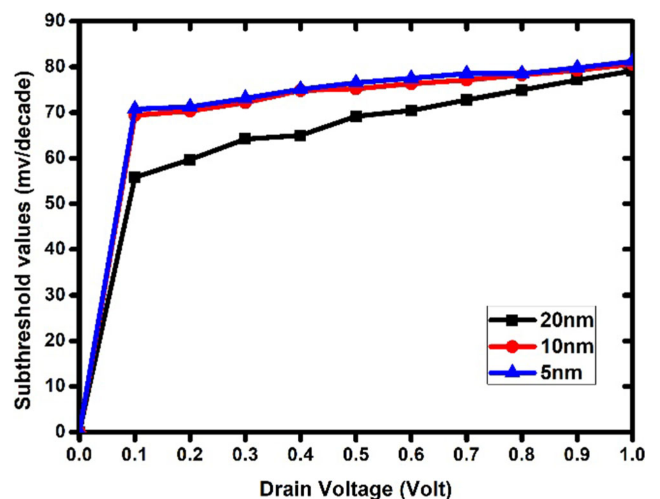

Fig. 6 Sub cut-in values for 5 nm, 10 nm, 20 nm FinFET

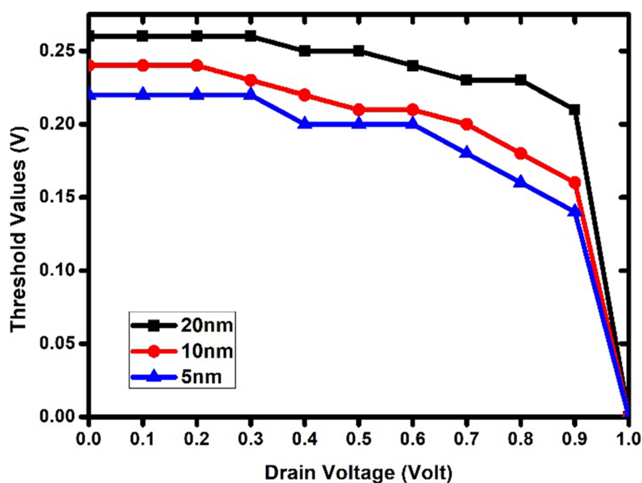

Fig. 7 V_t values for 20 nm, 10 nm, 5 nm FinFET

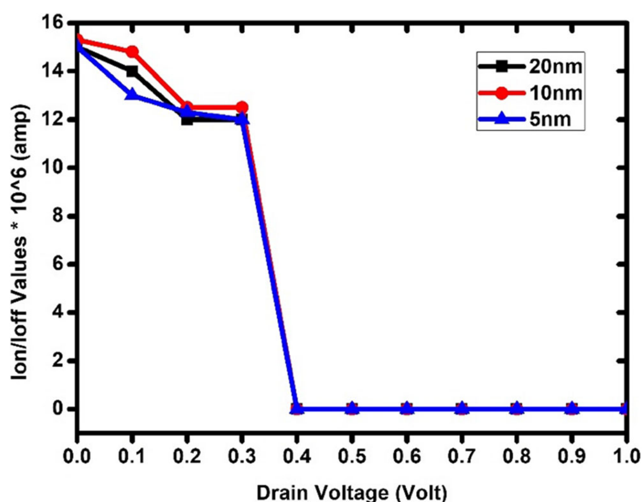

Fig. 8 Ion/Ioff for 20 nm, 10 nm, 5 nm FinFET

value and its quite apparent from the Fig. 6 as we go deeper and deeper in nanometer regime. It's really advantageous for the device to work at low power. Figure 7 depicts threshold voltage of proposed model of FinFET and its low as the transistor operates at deep sub nanometer. At 5 nm threshold voltage is low comparably and it surely help the device to work better in ultra-low power applications [17–19].

Figure 8 represents Ion/Ioff plot for increase in drain voltage ranges from 0 to 1 V and from the Fig. 8 one can easily visualize I_{off} value as required for ultra-low power requirement of transistors.

4 Conclusions

Here, effect of fin geometry on cut-in voltage is investigated for different fin widths of 20 nm, 10 nm, 5 nm using many FinFET device at 20 nm,10 nm,5 nm to meet ultra-low power requirements using device simulations. A novel optimised technique has been presented to drastically minimize leakage current. The underlying idea of FinFET device under deep sub nanometer regime, as well as its limitations compared to planar MOSFETs and operating principle, were investigated. It was discovered that as gate length reduces, ultra-low power transistor requirements can be met. During Analytical simulation work of FinFET it is observed that at decreased channel length of FinFET I_{on} current increases, Subthreshold slope increases, DIBL increases, threshold voltage decreases thereby causing superior performance of the device at reduced technology node.

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Data Availability No supplementary materials.

Declarations

Consent to Participate Yes.

Conflict of Interest The authors declare that they have no conflict of interest.

Research Involving Human Participants and/or Animals This article does not contain any studies with human or animal subjects.

Consent for Publication Author(s): M Parimala Devi.

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