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ORIGINAL PAPER

Drain Dielectric Pocket Engineering: its Impact on the Electrical Performance of a Hetero-Structure Tunnel FET

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Abstract

In this paper, a simulated $Si_{0.6}Ge_{0.4}$/Si hetero-structure double gate tunneling FET with drain dielectric pocket (DDP-SiGe-TFET) is reported for the first time. The high-*k* (HfO_2) dielectric pocket is positioned in the vicinity of the HfO_2/drain interface for improving the ambipolarity. The combination of low bandgap SiGe source and high bandgap Silicon channel improves the drain current performance without raising the OFF-state leakage current (I_{OFF}). The different electrical characteristics such as drain current, average subthreshold swing, switching current ratio, tunneling distance, band-to-band (BTBT) rate, and electric field of the suggested device have been studied. The outcomes are further compared with the conventional Si-TFET and hetero-structure TFET to justify its supremacy. The influence of the variation in the DDP length (L_p), thickness (t_p), and alloy fraction (x) of the $Si_{1-x}Ge_x$ source upon device performance is examined. DDP-SiGe-TFET offers a much higher I_{ON}/I_{Amb} ratio of 4.7×10^{10} with lower subthreshold swing (SS) of 24 mV/decade for an optimized $L_p = 40$ nm and $t_p = 8$ nm. Further, the RF performance investigation of the device in terms of transconductance (g_m), cut-off frequency (f_t), and maximum oscillation frequency (f_{max}) has been carried out. The different device structures presented here have been simulated using the Silvaco TCAD simulation tool.

Keywords TFET · Ambipolarity · Dielectric pocket · Current ratio · Tunneling distance

1 Introduction

The switching mechanism of a traditional MOS transistor based on thermionic emission of charge carriers over a barrier potential leads to higher power consumption. This current transport mechanism also doesn't permit the subthreshold swing (SS) to go below 60 mV/decade. Therefore, the researchers are in the constant quest of designing new devices which keep SS within 60 mV/decade [1–4]. In this regard, the band-to-band tunneling (BTBT) current transport mechanism can possibly presents the solution for providing much lower SS. Thus, the tunnel field-effect transistor (TFET) with the interband tunneling process can function as an energy-efficient switch [4]. TFET also provides superior performance over the traditional MOSFET in terms of minimal temperature dependency, smaller leakage current, and resilience to various short channel effects [5]. Besides these merits, TFETs suffer from few limitations such as low ON current (I_{ON}), unidirectional current flow and, higher ambipolarity [6]. Experts have demonstrated a number of techniques to improve I_{ON} performance in recent times. The use of lower-bandgap material as source [7], multi-gate technology [8], use of compound III-V material [9], presence of a pocket at the source/channel (S/C) interface, and using high-*k* material at the gate terminal [10–12] are few ways to enhance the drain current in the ON-state. All stated approaches are mainly based on the modulation of tunneling barrier width and formation of the higher electric field at the tunneling junction to enhance the ON current performance. In addition to this, several hetero-structures have also been proposed using the low bandgap compound material like GaAs, GaAsSb, InGaAs, InP, and InAs to achieve better drain current [13–15].

SiGe is one of the upcoming materials used in the design of tunnel FET due to its improved synthesis process, effective bandgap modulation, and fabrication possibility [16–20]. The alloy $Si_{1-x}Ge_x$ controls the bandgap energy by varying the Germanium alloy fraction (x). The presence

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of lower bandgap SiGe in the source region leads to a lower tunneling barrier width. Thus, an improved ON-current is achieved with increasing Ge alloy fraction in SiGe homo-structure TFETs [16, 18]. On the other hand, the OFF-state leakage current (I_{OFF}) and ambipolar current (I_{Amb}) degrade with the existence of SiGe in the channel and drain region respectively [16, 17]. Thus, TFET with the combination of $Si_{1-x}Ge_x$ source and Si channel/drain can provide higher I_{ON} without increasing I_{OFF}. Still, it suffers from higher unwanted ambipolarity similar to the n-type silicon TFET for applied negative bias. This creates a significant hindrance in low-power applications and inverter-based logic circuits [21]. To reduce ambipolarity, several techniques such as lower drain doping, gate dielectric engineering, gate-to-drain underlap/overlap, work-function modulation, spacer technology, and use of dielectric pocket [22–27] have already been employed. These methods are able to suppress I_{Amb} at the cost of fabrication complexity, and increased drain resistance, which further weakens the ON current performance. Hence, it is safe to conclude that even after much comprehensive research on TFET ambipolarity, the researchers still unable to reveal the fitting technique to accomplish the objective.

In the present work, a $Si_{0.6}Ge_{0.4}$/Si hetero-structure n-type double gate TFET with drain dielectric pocket (DDP) is proposed. The DDP is positioned exactly at the top gate dielectric/drain interface along the length of the drain. The primary objective of the simulated n-type proposed TFET is to get rid of ambipolarity without hampering I_{ON} and SS. A comparative DC analysis between the results of DDP-SiGe-TFET with Si-TFET and SiGe-TFET has been carried out. The DC performance is measured in terms of band energy, lateral electric field, e- and h + BTBT rate, tunneling distance, and transfer characteristics. The supremacy of the reported device is established as a result of its higher I_{ON}/I_{Amb} current ratio. This indicates the structure's ability to provide much suppressed ambipolar current without degrading ON current. The DDP length and thickness have been optimized to offer maximum I_{ON}/I_{Amb} ratio of 4.7×10^{10} and I_{ON}/I_{OFF} ratio of 3.0×10^{11} with 24 mV/decade average SS. The impact of drain doping concentration and gate oxide thickness on the drain current performance has been studied in this paper. The analysis is further extended to study the effect of the variation in the alloy fraction (x) of the source modulated $Si_{1-x}Ge_x$. Different RF parameters such as transconductance, cut-off frequency, and maximum oscillation frequency of DDP-SiGe-TFET have been reported. The Silvaco TCAD [28] simulator has been used to execute the simulation of the device structures.

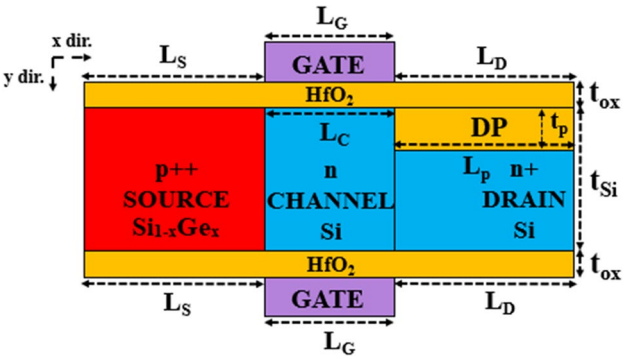

Fig. 1 Cross-sectional view of an n-type DDP-SiGe-TFET

Table 1 Parameters used in the simulated device structure

Parameters	DDP-SiGe-TFET
Source length (L_S), nm	40
Channel length (L_C) / Gate length (L_G), nm	30
Drain length (L_D), nm	40
Oxide thickness (t_{OX}), nm	1
Silicon body thickness (t_{Si}), nm	10
Source (P^{++}) doping concentration (N_S), cm^{-3}	10^{20}
Channel (i) doping concentration (N_C), cm^{-3}	10^{15}
Drain (n^+) doping concentration (N_D), cm^{-3}	10^{19}
DDP length (L_P), nm	10-40
DDP thickness (t_P), nm	2-8
Mole fraction for $Si_{1-x}Ge_x$	40%
Gate work-function (ϕ_m), eV	4.2

2 Proposed Device Description

Figure 1 shows the schematic view of the reported n-type structure. The source region is mounted with a compound material $Si_{1-x}Ge_x$ having the highest Germanium alloy fraction of x = 0.4 as per the industry standard [29] along with silicon channel and drain. A dielectric pocket is positioned in the drain region exactly at the HfO_2/drain interface. Here, the DDP (drain dielectric pocket) is considered with an optimized length (L_P) of 40 nm and thickness (t_P) of 8 nm to suppress the ambipolarity effect to the maximum extent. The high-*k* dielectric (HfO_2) is used in the DDP to provide reduced interband tunneling. The parameters used for the simulation of the reported device are provided in Table 1. The gate bias is applied at both the gates (top and bottom) symmetrically.

3 Simulation and Calibration

Here, the 2-D Silvaco TCAD simulator [28] is used to simulate the proposed DDP-SiGe-TFET. In the device simulation process, BBT.NONLOCAL tunneling model has been included to allow the tunneling of carriers in both the x- and y-direction. Here, the tunneling takes place on a series of one-dimensional slices through the junction. A separate QTX.MESH and QTY.MESH statements have been used to set up a rectangular area to activate the tunneling processes. The Fermi-Dirac statistic is used to incorporate the heavy doping regions of the device. The Band-Gap Narrowing (BGN) model is also part of the device physics to account for the change in the bandgap energy during simulation. The concentration dependent Shockley-Read-Hall (CONSRH) recombination model is incorporated to accommodate the recombination of minority charge carriers. In addition to these models, the impurity and temperature-dependent mobility models along with the high field velocity saturation are also included. The Newton Iteration method is considered for the drift-diffusion calculations, which also avoids the convergence issue in the simulator. It is highly essential to calibrate the simulator, which can be achieved by comparing the results with published experimental work. Figure 2 illustrates the calibration of a simulated n-type double gate TFET by comparing its I-V characteristics with the published experimental results [30]. The simulation is realized by considering the parameters reported by Wang et al. [30] and provides nearly similar results.

The detailed fabrication process for the reported device is provided in this section. At first, a highly doped p^{++} single crystalline $Si_{0.6}Ge_{0.4}$ 40 nm source with 40% Ge alloy fraction has been formed by using the auger electron spectroscope (AES) and the transmission electron microscope (TEM) [18, 31, 32]. The trivalent phosphorous ion implantation technique can be considered for the doping profile [33]. Thereafter, the intrinsic silicon (30 nm) can be grown by the epitaxial growth process. The final n^+ drain region can be implanted by the BF_2^+ ion implantation method [34]. The source and drain implant can be done by rapid thermal annealing at higher temperatures [35]. The dielectric (high-*k*) pocket engineering can be performed by selective masking and etching followed by deposition. Subsequently, by rotating the structure at the right angle and applying the physical vapor deposition (PVD) technique [34], HfO_2 (1 nm) can be formed at both ends of the p^{++}-i-n^+ layer.

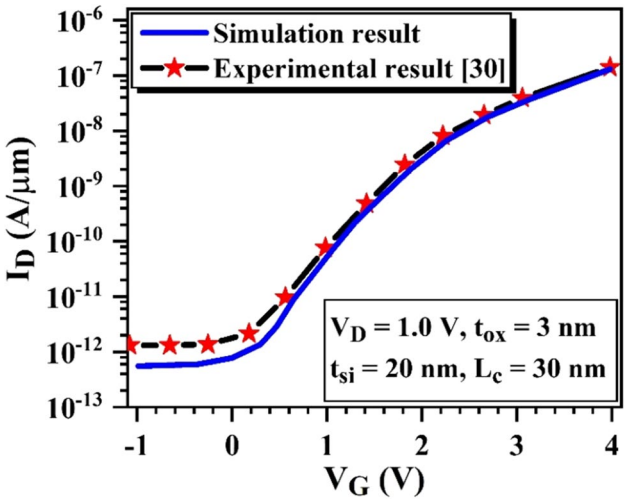

Fig. 2 Calibration of the simulated double gate TFET using the experimental results [30]

4 Results and Discussion

4.1 DC Performance Analysis

This sub-section includes the detailed investigation of the effect of the presence of DDP upon the DC performance of a hetero-structure double gate tunnel FET. Here, the drain current at a gate voltage of −1.5 V is considered as ambipolar current.

Figure 3(a) illustrates the $I_D - V_G$ characteristics of DDP-SiGe-TFET with drain bias of 1.0 V and the outcomes are further compared with that of conventional Si-TFET and SiGe-TFET. The SiGe based TFET provides 1-decade improved I_{ON} over Silicon TFET owing to the lower bandgap nature of the SiGe present in the source. On the other hand, the OFF current (I_{OFF}) performance degrades approximately by the same margin with the introduction of SiGe. Thus, the I_{ON}/I_{OFF} current ratio remains in the range of 10^{11} for all the structures discussed in this section, as seen in Fig. 3(b). However, there is a significant reduction of 8-decades in the ambipolar current (I_{Amb}) for the reported device. The device exhibits a much lower I_{Amb} of 9.15×10^{-15}A/μm at $V_G = -1.5$ V compared to Si-TFET (~10^{-7} A/μm). This is due to the smaller interband tunneling area and lower BTBT rate across the channel/drain (C/D) junction for DDP-SiGe-TFET. As a result of lower I_{Amb}, the current ratio I_{ON}/I_{Amb} for DDP-SiGe-TFET shows a spike increment (4.7×10^{10}). This magnitude of the current ratio is more than 7-decades higher as compared to SiGe-TFET. Thus, DDP-SiGe-TFET with DDP length of 40 nm and thickness of 8 nm offers the largest current ratio in the ambipolar condition with similar I_{ON}/I_{OFF} and lower average SS of 24 mV/decade. The ambipolarity reduction can be further examined by making use of energy band analysis and estimation of the tunneling junction distance.

The energy band comparison for the three different structures with applied positive and negative gate bias

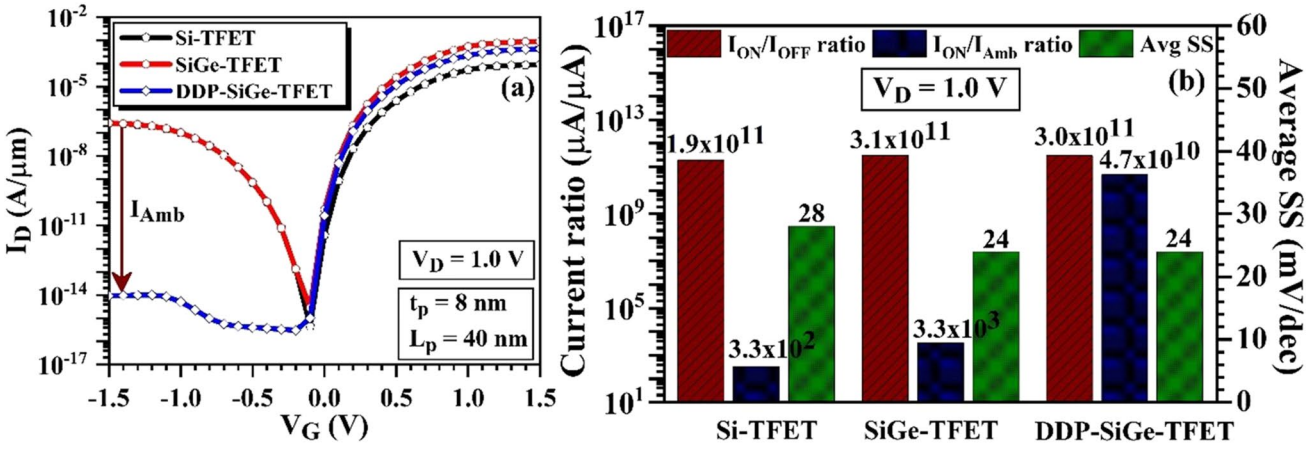

Fig. 3 A comparative analysis of (a) $I_D - V_G$ characteristics (b) current ratio for the reported device with SiGe-TFET and conventional Si-TFET

is illustrated in Fig. 4(a) and Fig. 4(b) respectively. For $V_G \geq 0$ V, the confined charge carriers beneath the gate electrode increase. This allows more bending of the conduction band in the channel which further decreases tunneling distance along the source/channel (S/C) interface. It can be seen from Fig. 4(a) that both the SiGe TFETs provide more band bending at the S/C junction compared to silicon TFET. This is due to the low bandgap energy nature of SiGe present in the source region with silicon channel, which results in the formation of a hetero-junction and improves I_{ON} as shown in Fig. 3(a). Similarly, Fig. 4(b) shows the band energy analysis at $V_G = -1.5$ V. The proposed TFET provides lower energy band bending at the C/D interface in comparison with SiGe-TFET and Si-TFET owing to the presence of high-*k* pocket. This alternately provides larger tunneling distance (t_W) in the ambipolar condition as provided in Fig. 5. The magnitude of t_W nm can be estimated using an energy band diagram as explained by Dash et al. [36]. In the ON-state, both SiGe TFETs exhibit lower t_W compared to the silicon TFET, which will provide better ON current performance. On the other hand, the overlapped tunneling width is ≥10 nm for the proposed device as shown in Fig. 4(b) (dotted lines). There is a significant 81% increase in the magnitude of t_W with the introduction of the drain dielectric pocket. This larger t_W (19 nm) doesn't allow any tunneling charge conduction and thus provides a much suppressed ambipolar current in the order of~10^{-15} A/μm. The analysis in terms of band-to-band (BTBT) generation rate and electric field has been examined in further discussion.

Figure 6(a) and 6(b) display the magnitude of BTBT rate and absolute electric field in the ON state and ambipolar state respectively. SiGe-TFET exhibits the highest BTBT rate

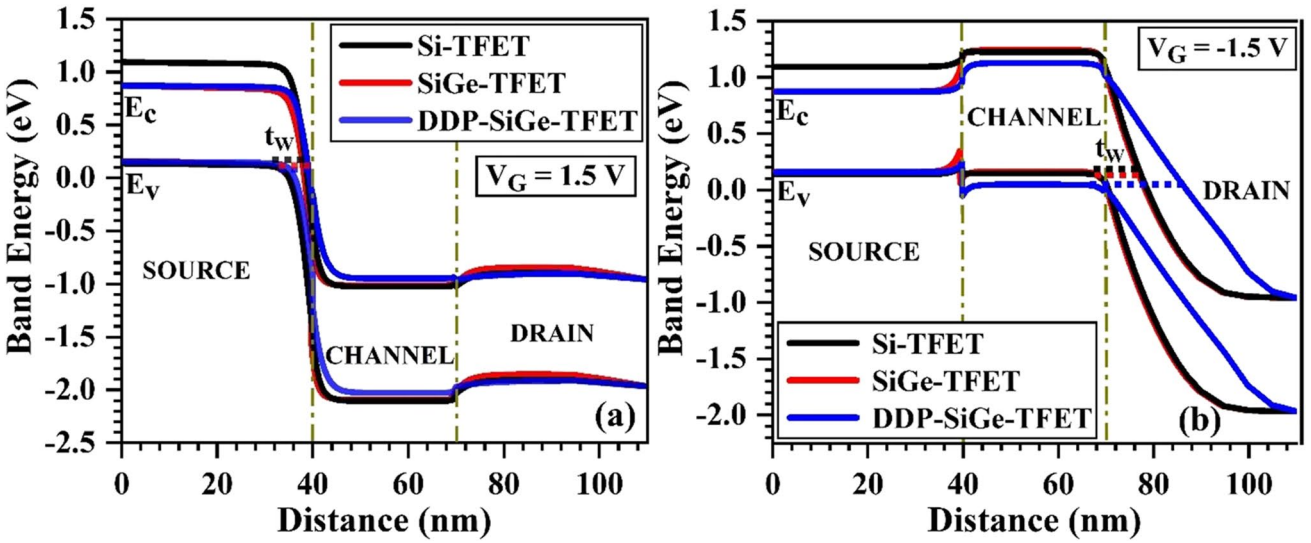

Fig. 4 A comparative band energy analysis w.r.t. distance in the (a) ON-state ($V_G = 1.5$ V) (b) ambipolar-state ($V_G = -1.5$ V)

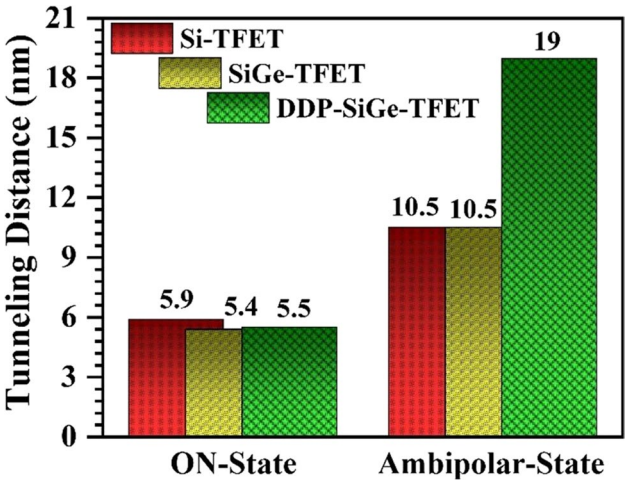

Fig. 5 Tunneling distance comparison in both ON-state and ambipolar state

of 3.43×10^{33} $cm^{-3}s^{-1}$ and lateral field of 6.1×10^{6} Vcm^{-1} at $V_G = 1.5$ V compared to other structures, which provides improved I_{ON}. However, in the ambipolar state, the existence of the dielectric pocket in the drain increases the tunneling width and provides a much-reduced BTBT rate of 1.43×10^{24} $cm^{-3}s^{-1}$. This lower BTBT of carriers suppresses the ambipolarity to the full extent. The reported device exhibits a BTBT rate lower by 7-decades compared to SiGe-TFET, which alternately reduces I_{Amb} by the same 8-decades margin as shown in Fig. 3(a). Similarly, DDP-SiGe-TFET offers a lateral electric field of 1.0×10^{6} Vcm^{-1}, which is 68% lower than other structures discussed in this paper. The influence of varying the DDP length and thickness on the DC parameters is investigated in the upcoming analysis.

The $I_D - V_G$ characteristic of DDP-SiGe-TFET with variation in the DDP length is shown in Fig. 7(a). Here, the magnitude of L_P is varied from 10 nm to 40 nm keeping a constant thickness of 8 nm. With the increase in L_P, the ambipolar current decreases consistently. The present device structure exhibits $I_{Amb}$of 1.28×10^{-9}A/μm for $L_P = 10$ nm and decreases significantly to 9.15×10^{-15}A/μm for a maximum length of 40 nm. This 6-decades reduction is due to the widening of the tunneling width in the neighborhood of the C/D junction. Oppositely, this leads to the enhancement in the magnitude of the I_{ON}/I_{Amb} ratio in the same order as shown in Fig. 7(b). The simulated DDP-SiGe-TFET offers a minimum average subthreshold swing of 24 mV/decade and I_{ON}/I_{Amb} of 4.7×10^{10} at 40 nm length. Figure 7(c) presents the energy band analysis for different values of L_P. The minimum tunneling width (t_W) gradually increases, as we go on increasing the pocket length as seen from Fig. 7(d). The largest t_W of 19 nm is estimated for the device with L_P = 40 nm, which is 46% higher than the magnitude at 10 nm. The overlapping area between the valence band and conduction band at the C/D interface is progressively reduced for larger t_W. This decreases the tunneling probability and BTBT rate along the respective interface. The comparison of the BTBT generation rate and electric field is described in Fig. 7(e). Both the parameters continuously reduce with the increase in L_P. The proposed TFET provides lower BTBT rate of 1.43×10^{24} $cm^{-3}s^{-1}$ and lateral electric field of 1.0×10^{6} Vcm^{-1} for $L_P = 40$ nm. This indicates the tunneling of very few carriers in the ambipolar state and hence offers lower ambipolarity.

The transfer characteristic of DDP-SiGe-TFET with the variation in the DP thickness is shown in Fig. 8(a). In this case, the DP length is considered as 40 nm. The ambipolar current decreases steadily with the increase in the magnitude of t_P. The device exhibits a much reduced I_{Amb} of 9.15×10^{-15}A/μm for $t_P = 8$ nm, which is approximately 7-decades lower than the magnitude at a thickness of 2 nm (3.80×10^{-8}A/μm). This significant reduction is due to the lower tunneling probability of the device in the ambipolar condition. This further leads to a higher I_{ON}/I_{Amb} ratio as shown in Fig. 8(b). It can be seen that DDP-SiGe-TFET

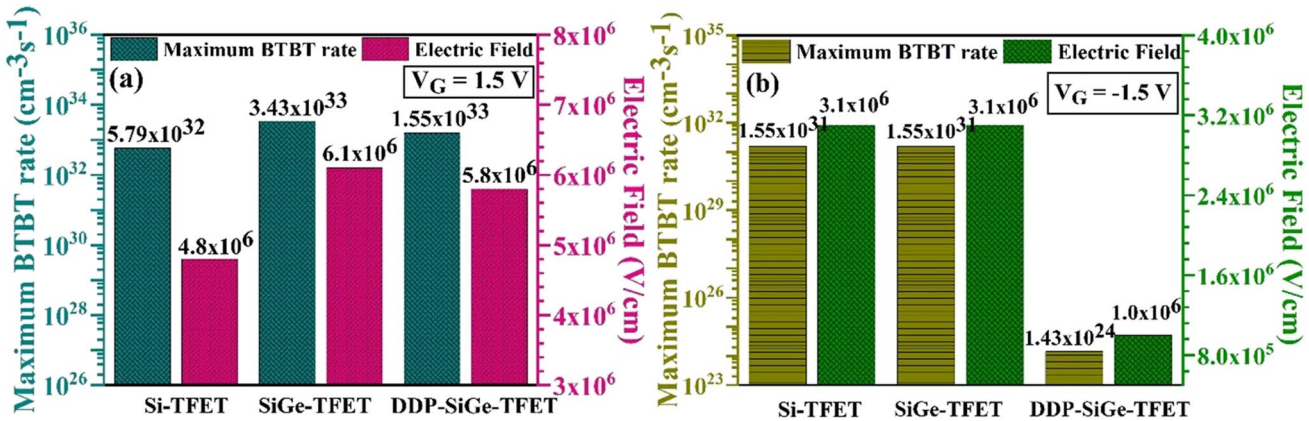

Fig. 6 A comparative plot of maximum BTBT rate and electric field in the (a) ON condition (b) ambipolar condition

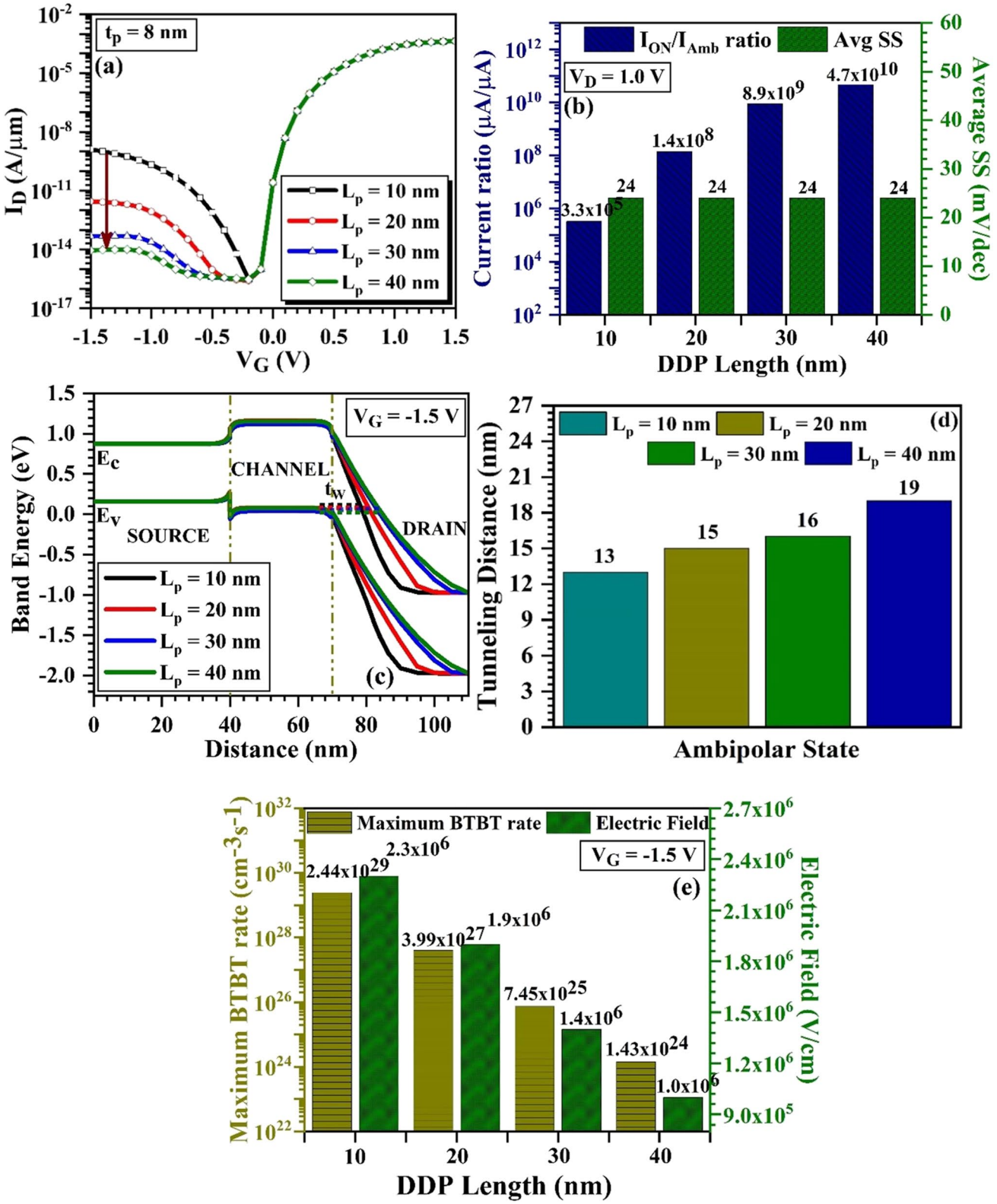

Fig. 7 Effect of the dielectric pocket length (L_P) variation on the (a) transfer characteristics (b) current ratio, and avg. SS (c) energy band analysis at $V_G = -1.5$ V (d) effective tunneling distance along C/D junction (e) BTBT generation rate, and electric field

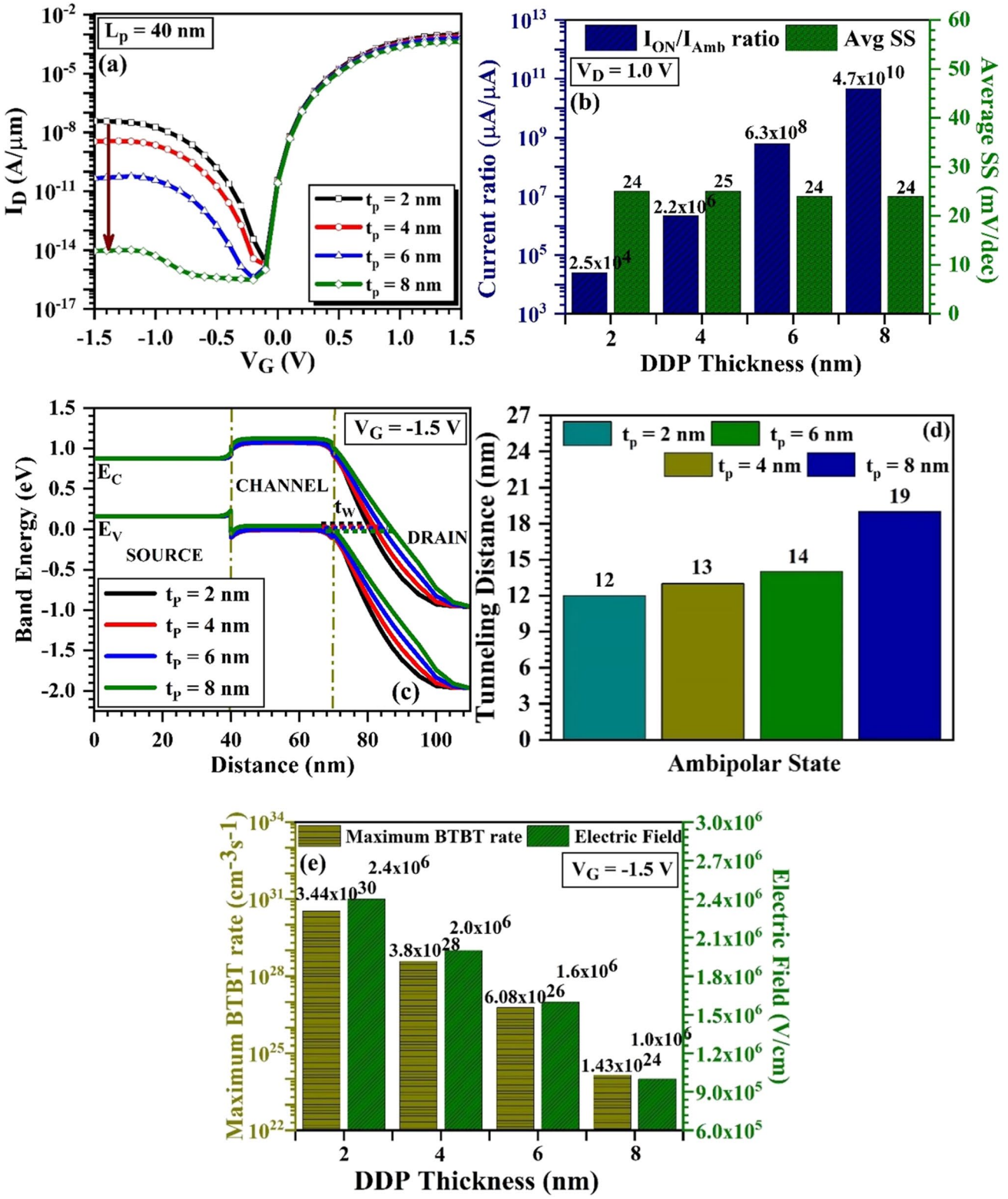

Fig. 8 Impact of dielectric pocket thickness (t_P) upon (a) IV characteristics (b) current ratio and SS (c) energy band analysis in the ambipolar state (d) tunneling distance along with the C/D interface (e) BTBT rate, and electric field

provides a maximum I_{ON}/I_{Amb} of 4.7×10^{10} with an average SS of 24 mV/decade for the thickness of 8 nm. The widening of the tunnel width in the locality of the C/D interface for $V_G=-1.5$ V is responsible for the lower ambipolarity and higher current ratio. Figure 8(c) presents the energy band analysis for the different values of t_P. It is interesting to note that the minimum tunneling width gradually increases, as we go on increasing the pocket thickness as seen from Fig. 8(c). Because of this, the overlapping of valance band and conduction band at the respective interface is reduced and the tunneling probability gets reduced. The tunneling distance variation is shown in Fig. 8(d). t_W is estimated to be 12 nm at $t_P = 2$ nm and the magnitude increases to 19 nm (58% rise) for an optimum t_P of 8 nm. The larger width reduces the tunneling generation rate and provides lower I_{Amb}. The comparison of the BTBT generation rate and the electric field is shown in Fig. 8(e). The magnitude of both the parameters reduces with the increase in t_P. The proposed device provides lower BTBT rate of 1.43×10^{24} $cm^{-3}s^{-1}$ and lateral electric field of 1.0×10^{6} Vcm^{-1} for $t_P = 8$ nm. The performance evaluation of DDP-SiGe-TFET with the variation in the alloy fraction has been examined in further discussion.

The effect of change in the alloy fraction (x) on the drain current performance is shown in Fig. 9(a). Here, the mole fraction of the compound $Si_{1-x}Ge_x$ has been varied from 0.10 (10%) to 0.40 (40%). The reported device provides a noticeable change in I_{ON} with variation in x while maintaining constant I_{Amb}. For $x=0.1$, the device offers an I_{ON} of 1.06×10^{-4}A/μm and the magnitude is further increased to 4.30×10^{-4}A/μm for $x=0.4$. This leads to an improvement in the magnitude of the current ratio (I_{ON}/I_{Amb}) from 1.1×10^{10} to 4.7×10^{10} as shown in Fig. 9(b). The average SS for 40% alloy fraction is the least (24 mV/decade) and increases slowly with a drop in x value. The increase in I_{ON} is due to the narrowing of the tunneling width (t_W) across S/C interface, which is clearly depicted in Fig. 9(c). The magnitude at the respective interface sluggishly decreases with an increase in the alloy fraction

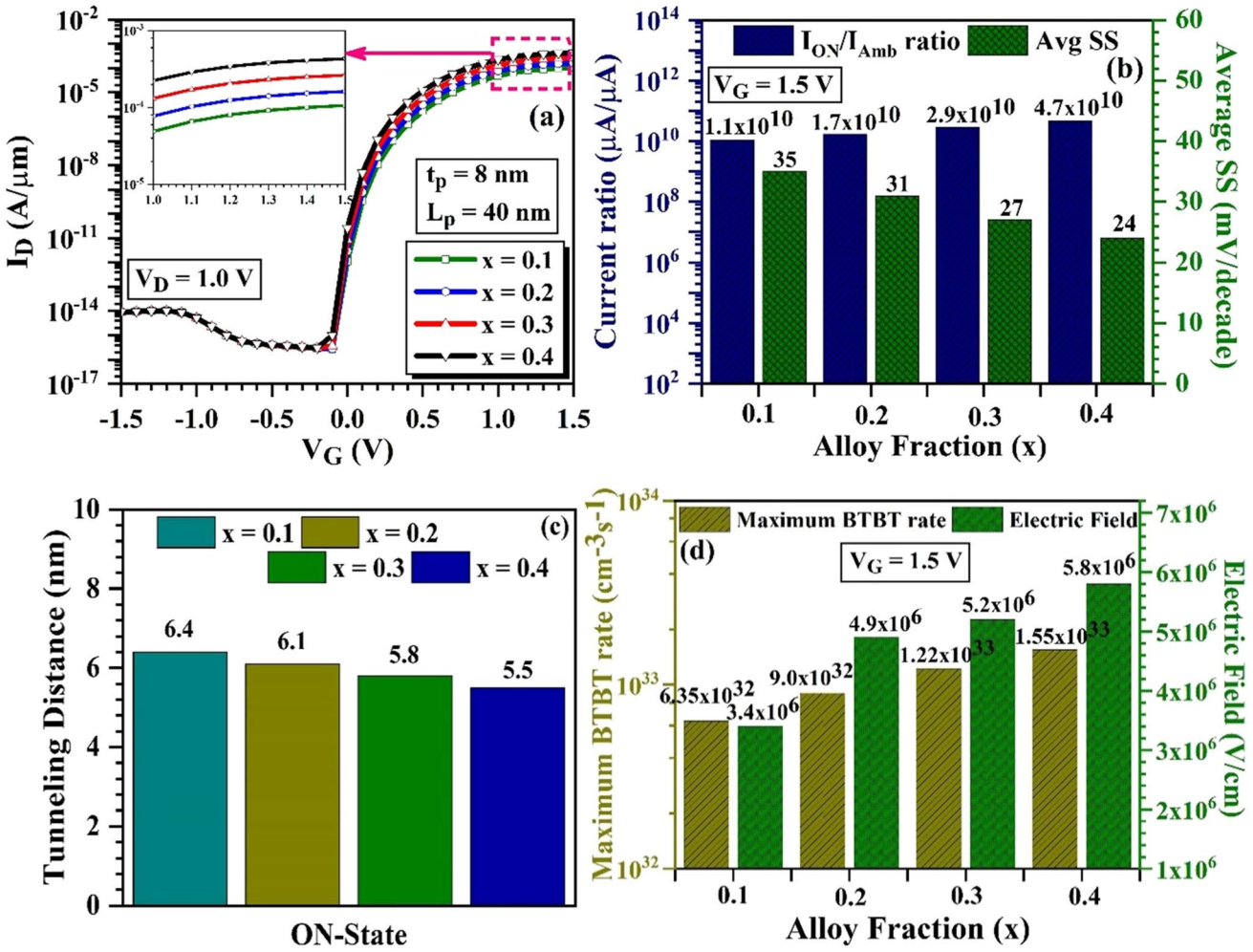

Fig. 9 (a) Transfer characteristics (b) average SS and current ratio (c) effective tunneling distance (d) electric field and BTBT generation rate at the S/C interface for different values of alloy fraction (x)

from 10% - 40%. This implies a higher probability of tunneling and thus improves drain current in the ON-state. The comparison of BTBT generation rate and electric field for $V_G = 1.5$ V is described in Fig. 9(d). The magnitude of both the factors follows the same increasing trend with the upsurge in x percentage. For the proposed device, the maximum value of e^- BTBT rate of 1.55×10^{33} $cm^{-3}s^{-1}$ and electric field of 5.8×10^6 Vcm^{-1} has been achieved with $x = 0.4$. This indicates higher tunneling of charge carriers in the ON-state and improves the drain current performance.

Here, the doping concentration of the drain region (N_D) has been varied from 1×10^{18} cm^{-3} to 2×10^{19} cm^{-3} for the performance comparison. Figure 10(a) depicts the drain current curve as a function of gate voltage with different magnitudes of N_D at a fixed drain bias of 1.0 V. The ambipolar current increases consistently with surge in N_D due to the narrowing of the tunneling barrier width at the C/D interface. On the other hand, it can be observed that the drain current at $V_G = 1.5$ V is unaffected. This is as a result of unchanged tunneling distance in the neighborhood of the primary tunneling junction. The device reports a much lower I_{Amb} of 2.67×10^{-17} A/μm for $N_D = 1 \times 10^{18}$ cm^{-3} and degrades to 3.45×10^{-11} A/μm (by ~6-decades) with higher drain doping of 2×10^{19} cm^{-3}. This reduced ambipolarity will certainly improve the current ratio in a big way. To support the reduction in I_{Amb}, we have also provided the maximum BTBT rate and tunneling distance comparison as shown in Fig. 10(b). For $V_G = -1.5$ V, DDP-SiGe-TFET exhibits much lower BTBT rate of 2.95×10^{19} cm^{-3} s^{-1} and larger tunneling width of 21 nm with $N_D = 1 \times 10^{18}$ cm^{-3}. Thus, both the parameters contribute lower ambipolarity for the proposed device, as they allow fewer charge carriers to tunnel along the C/D interface.

The influence of dielectric pocket material on the transfer characteristics of the proposed device is examined in Fig. 11(a). Here, we have considered Al_2O_3 ($k = 9.3$), SiO_2 ($k = 3.9$) and air ($k = 1$) as the dielectric pocket material and compared the results with that of HfO_2 ($k = 22$). The variation doesn't affect the drain current performance both in the ON-state and OFF-state as seen from the figure. However, there is a significant reduction in I_{Amb} with the upsurge in the *k* value. The device with Air DP gives a larger unwanted ambipolar current of 9.04×10^{-10}A/μm and reduces by 5-decades with high-*k* HfO_2. The presence of a high-*k* drain pocket increases the tunneling barrier at $V_G = -1.5$ V as depicted in Fig. 11(b) and reduces ambipolarity. Thus, the device can be able to suppress the ambipolarity significantly with a high-*k* dielectric pocket mounted in the drain region.

4.2 I_D-V_G Comparison with Other Ambipolarity Suppression Techniques

A comparative study of the transfer characteristics using different popular ambipolarity reduction techniques is provided in Fig. 12. The dimension of the device is kept identical for the accurate investigation of the ambipolarity performance. I_{Amb} reduces in all the methods discussed, due to the narrow tunneling barrier width in the vicinity of C/D interface. In the gate-to-drain overlap technique as shown in Fig. 12(b), the gate electrode has been extended towards the drain. The I_D-V_G curve has been plotted by considering the overlapping length (L_{over}) up to 35 nm ($L_D = 40$ nm). The device exhibits a reduced I_{Amb} of 7.44×10^{-10}A/μm for $L_{over} = 35$ nm, which is approximately 3-decades lower than the conventional TFET (2.64×10^{-7}A/μm). Similarly, Fig. 12(c) illustrates the gate-to-drain underlap engineering in double gate TFET with the same dimension. In this method, the

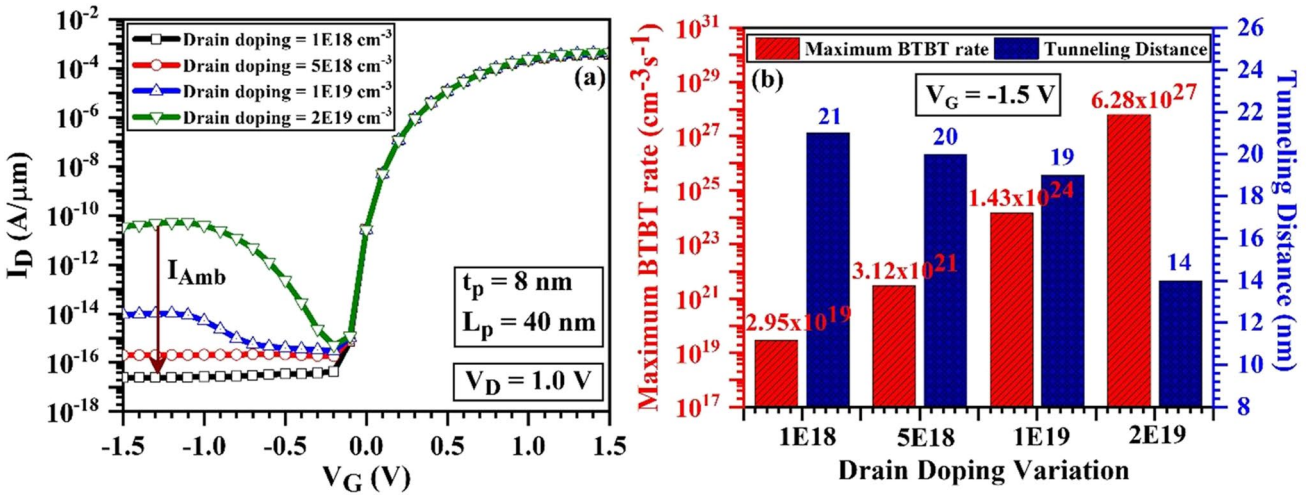

Fig. 10 Effect of drain doping on (a) transfer characteristics (b) BTBT rate, and tunneling distance of the reported device

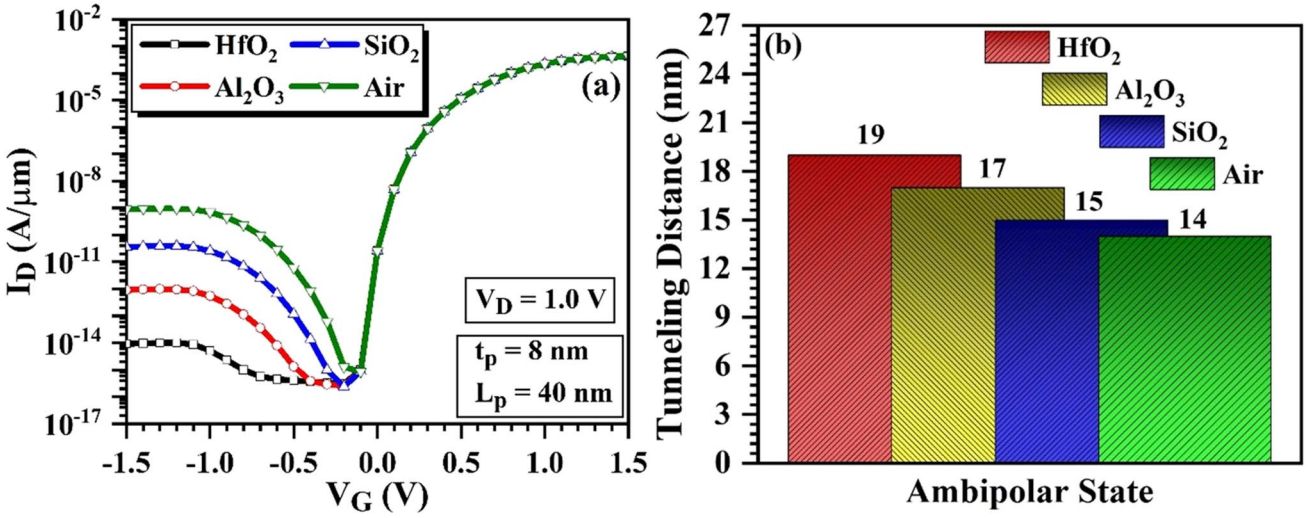

Fig. 11 (a) I_D vs V_G characteristics (b) tunneling distance at the C/D interface in presence of different dielectric materials

gate length (L_G) has been shortened up to 5 nm (underlap length of 25 nm) to provide much reduced I_{Amb}. DGTFET with $L_{und} = 25$ nm offers much lower ambipolar current of 2.06×10^{-14}A/μm, which is considerably lower compared to the overlap technique and at par with the DDP method discussed in this paper. However, the off state leakage current at $V_G = 0$ V is affected deeply with the increase in L_{und} compared to DDP. Thus, the SiGe/Si TFET with DDP will provide higher I_{ON}/I_{OFF} and I_{ON}/I_{Amb} current ratio compared to other techniques. Further, the underlap approach increases the resistance of the channel near the drain and fabrication cost [26].

4.3 RF Performance Analysis

Transconductance (g_m) is one of the significant parameters to consider during the estimation of the RF performance of a device. It can be derived by the first order differentiation of drain current w.r.t. gate bias at a constant drain voltage. Figure 13(a) displays g_m for the reported device as a function of V_G and the results are compared with conventional TFET. It increases exponentially with an increase in gate voltage due to the high current driving capacity of the charge carriers. DDP-SiGe-TFET provides a maximum g_m of 1.88×10^{-3} S/μm. As the high-*k* dielectric pocket is positioned in the drain region, it is most likely to affect the gate-to-drain capacitance (C_{gd}) as seen from Fig. 13(b). The device provides a C_{gd} of 3.09 fF/μm at $V_G = 1.5$ V, which is lesser compared to Si-TFET. This is due to the formation of the depletion region under the DP.

We also have investigated the influence of DDP upon the few key Figure of Merits (FOM) like cut-off frequency (f_t), and maximum oscillation frequency (f_{max}). These parameters are mathematically defined as [37]

$$f_t = g_m/2\pi C_{gg} = g_m/2\pi\left(C_{gs} + C_{gd}\right) \tag{1}$$

$$f_{max} = \sqrt{f_t/8\pi \times C_{gd} \times R_{gd}} \tag{2}$$

Here, C_{gs}, C_{gg} are the gate-to-source capacitance and total parasitic capacitance for the high frequency analysis. R_{gd} is known as gate-to-drain resistance.

The variation of the cut-off frequency (f_t) and maximum oscillation frequency (f_{max}) of the device in presence of DDP has been studied in Fig. 14. The reported device offers a maximum cut-off frequency of 516 GHz at $V_G = 1.0$ V. The increased f_t is due to the device's higher g_m and lower C_{gg} ($C_{gg} = C_{gd} + C_{gs}$). The presence of a narrow bandgap material (SiGe) in the source region leads to improvement in the interband tunneling, thus higher g_m is observed as seen from Fig. 13(a). The drain parasitic capacitance is also affected by the dielectric pocket (reduction in C_{gd}). The maximum oscillation frequency (f_{max}) is highly essential in the design of optimised amplifier and oscillator. DDP-SiGe-TFET also provides a higher value of f_{max} (725 GHz), as the parameter is dependent on f_t and C_{gg}.

5 Conclusion

This paper presents a comprehensive investigation of the impact of positioning a high-*k* dielectric pocket in the drain of an n-type SiGe-TFET. The performance superiority is established by comparing the results with heterostructure SiGe-TFET and conventional Si-TFET. The proposed DDP-SiGe-TFET with an optimized pocket length of 40 nm and thickness of 8 nm exhibits significantly

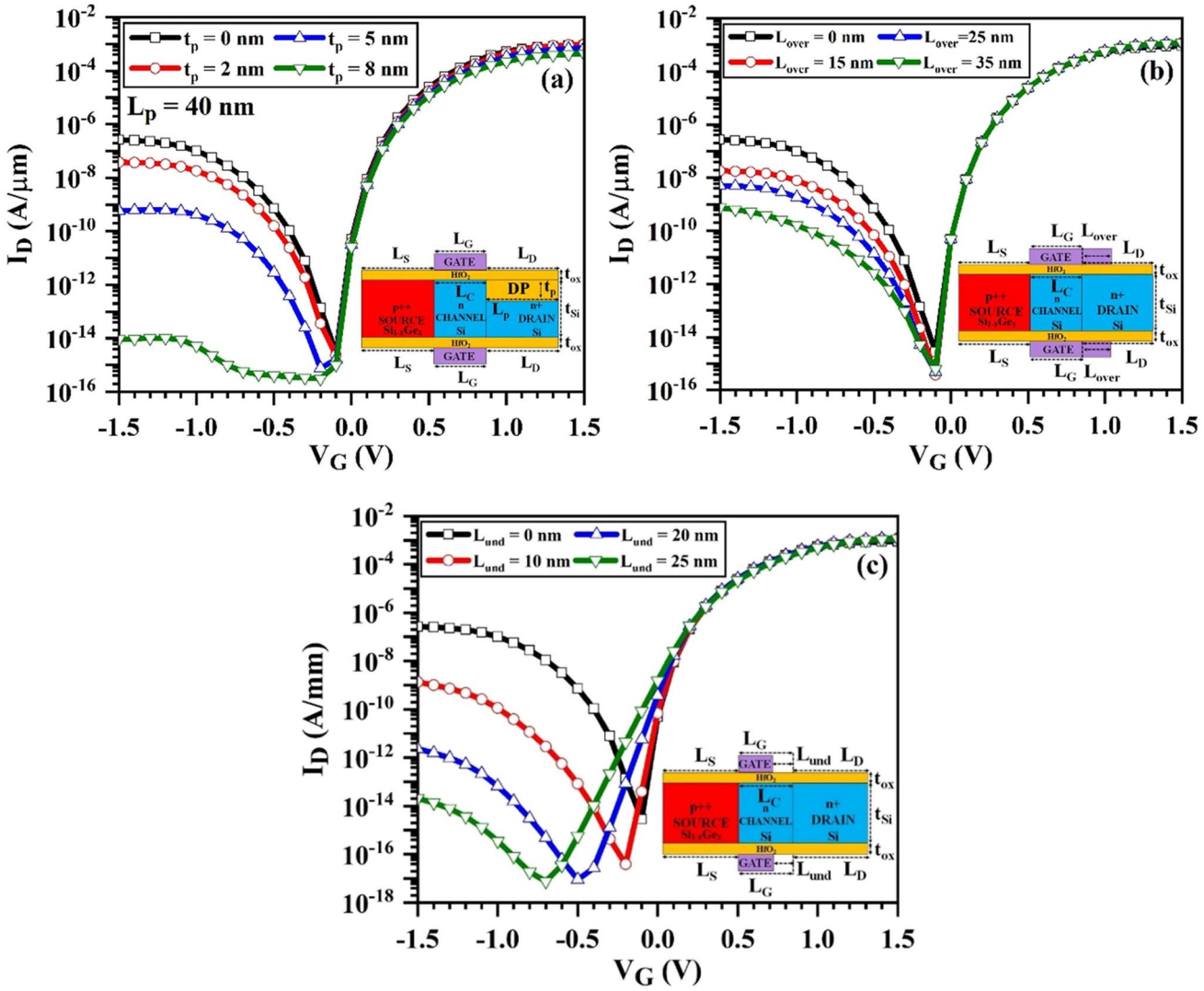

Fig. 12 Performance comparison between different ambipolarity reduction techniques: (a) dielectric pocket engineering (b) gate-to-drain overlapping (c) gate-to-drain underlap method

reduced ambipolarity ($I_{Amb} = 9.15 \times 10^{-15}$A/μm) at $V_G = -1.5$ V. The device also provides a higher current ratio ($I_{ON}/I_{Amb} = 4.7 \times 10^{10}$) with an average subthreshold swing of 24 mV/decade. The $Si_{0.6}Ge_{0.4}$/Si hetero-structure improves the drain current performance in the ON-state without degrading leakage current. The effect of dielectric constant variation for the pocket region on the analog performance is also examined. The suggested device with HfO_2 pocket in the drain proved to be effective in offering maximum current ratio and suppressed ambipolarity. Thus, the proposed device structure can be one of the potential candidates to be used in ultra-low power integrated circuits and SRAM digital circuits owing to its superior performance.

Availability of Data and Material Not Applicable.

Author Contributions Shwetapadma Panda has simulated the device and was a major contributor in writing the manuscript. Sidhartha Dash has theoretically developed the model and has contributed to the analysis of the results. Both the authors read and approved the final manuscript.

Declarations

Consent to Participate Not Applicable.

Consent for Publication Not Applicable.

Conflict of Interest The authors declare that they have no conflict of interests.

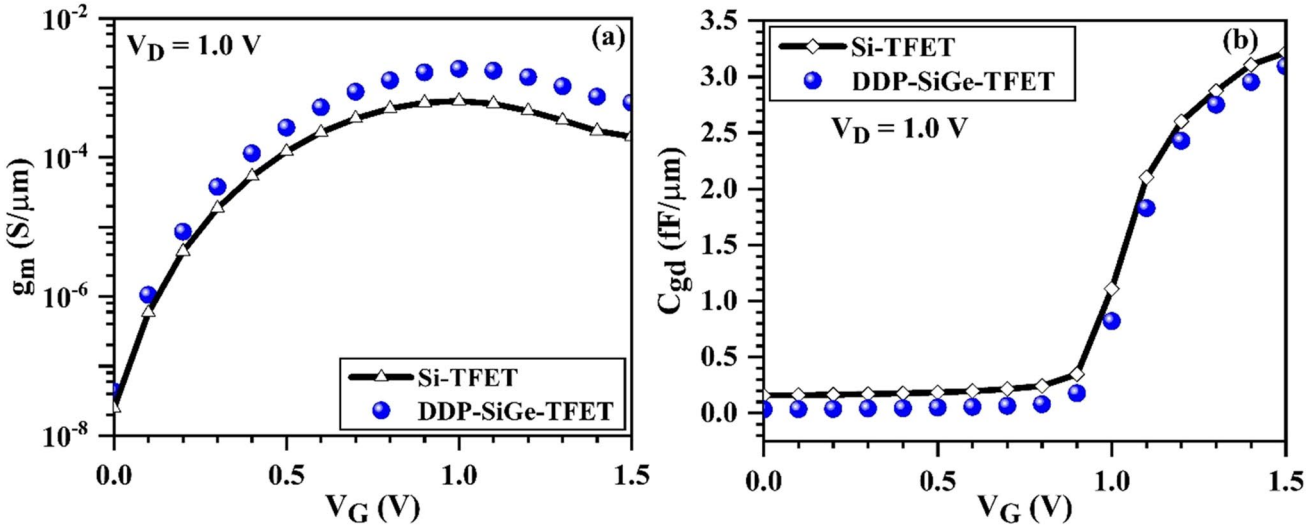

Fig. 13 (a) Transconductance (g_m) (b) gate-to-drain parasitic capacitance (C_{gd}) as a function of gate voltage (V_G)

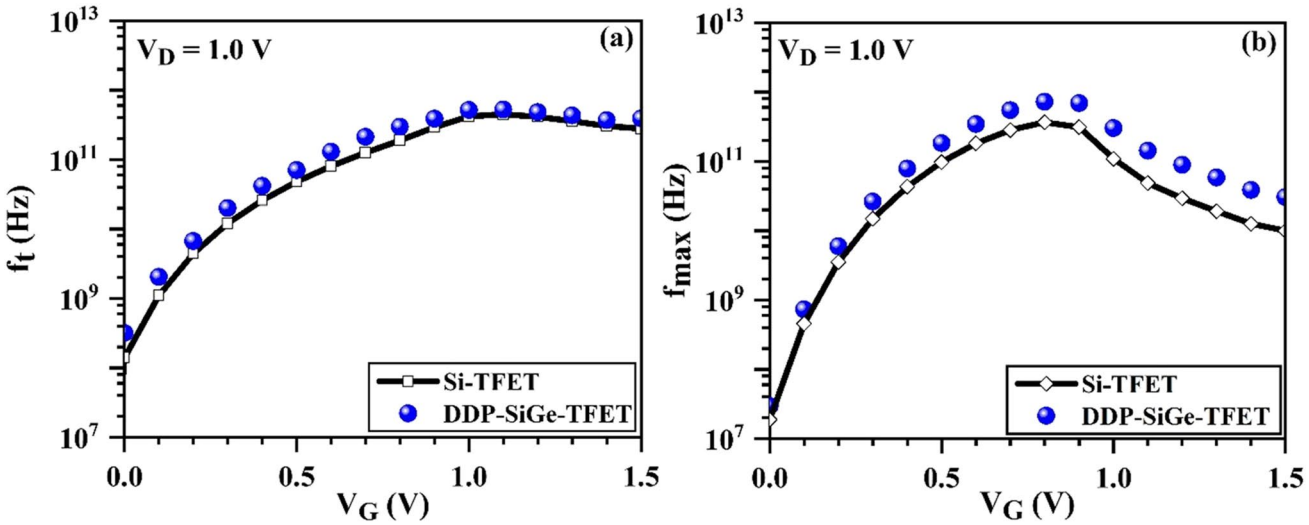

Fig. 14 (a) Unity gain cut-off frequency (f_t) (b) maximum oscillation frequency (f_{max}) as a function of gate voltage (V_G)

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