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REVIEW PAPER

Recent Trends in Novel Semiconductor Devices

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Abstract
The VLSI industry has grown a lot for several decades. The Packing density of integrated circuits has been increased without compromising the functionality. Scaling of semiconductor devices, improvements in process technology and the development of new device designs are the key to this. Starting from the planar MOSFETs to novel multigate transistors, semiconductor devices have a history of many decades. There is a need for extensive exploration in order to determine the best suited semiconductor device for a given technology node. A brief overview of the transition from the planar MOSFET to the novel semiconductor devices and a comparative study of various novel semiconductor devices viz. FinFET, Gate all around FET, Vertical Nanowire and Nanosheet FET are presented in this paper. Optimization of the device configuration and improvements in device design/technology are also reviewed. A review of the device comparison on the basis of various device performance parameters such as subthreshold slope, On-Off current ratio, ease of fabrication, process variations and impact of scaling on figure of merits is presented in this paper.

Keywords FinFET · MOSFET · Novel semiconductor devices · Nanosheet · Nanowire · Scaling

1 Introduction

The principal problem of VLSI domain is the incorporation of a growing count of devices with the requirement of high yield, low power operation, high performance and reliability [1]. Therefore, the reduction of the size of integrated circuits (ICs) and hence shrinking the transistor dimensions is required while not compromising the functionality and performance. Metal oxide semiconductor field effect transistor (MOSFET) has been used for many decades in VLSI industry [2–4] . Since 1970, MOSFET has been performing well. Over the years with continuing demand of higher packing density, the dimensions of MOSFET device have been scaled down from 10um in 1970 to 0.1um in 1998 [5]. To increase the integration density and performance of the (ICs), scaling of the MOSFETs has continued over the last decades. However, scaling beyond 0.1 nm node with traditional methods started degrading the device performance [5].

In the nanometer regime, increased short channel effects(SCEs) make it difficult to maintain the scaling trend predicted by Moore's law [2–4]. A deeply scaled MOSFET has a very narrow channel length because of which the electrostatics of the channel begin to be influenced by drain potential. Therefore, the gate relinquishes sufficient control over the channel. Consequently, the gate is incapable of closing up the channel entirely in the off-mode of working resulting in a higher leakage current between the drain and the source. To overcome these scaling issues, technology advancements like scaling of gate oxide, alternative high dielectric constant (K) materials, metal gate, and usage of strained silicon were adopted [5]. The scaling of gate oxide thickness (T_{ox}) and the use of high-k dielectrics increased the gate-channel coupling which in turn helped to reduce this problem. However, T_{ox} is essentially constrained by the worsening of the gate leakage and gate-induced drain leakage (GIDL) [6–8].

High-K gate materials, used to continue the scaling trend beyond 0.1 μm gate dimensions, allow the use of thick layers of dielectric without compromising the carrier density in the inversion layer. The result is, a reduced tunneling of carriers, and thus allowing further scaling of the T_{ox} [9]. The impact of high-K gate dielectrics on SCEs and device characteristics were studied in [10].

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Further, for better circuit performance, optimization of the doping profile is required. The overlap length should be minimized [11]. Transistors with smaller gate length and shallow source/drain junctions have been reported to have small gate overlap [12]. The source/drain extension length scaling and gate overlapping for MOSFETs of 0.1 μm and beyond was investigated in [9].

To allow scaling further, uniaxial mechanical stress was used which increased drive current. With technology scaling it becomes difficult to maintain a value of device threshold voltage which results in an acceptable I_{ON}/I_{OFF}. Using a metal gate allows the tuning of work-function and thus adjusting the threshold voltage [9, 13]. This allowed scaling up to 32 nm technology node [14]. Even with advanced fabrication techniques and the use of high-k gate dielectric materials, strained Si, and metal gate being used, scaling of device dimensions was believed to be difficult [9, 13]. However, further scaling down the devices introduced issues like leakage current, and variability which in turn reduced yield.

An ultra-thin body SOI nMOSFET was proposed to be a promising structure for deep-sub-tenth micron CMOS technology [15]. Later, a fully depleted thin-channel transistor named as DELTA was reported. Simulation and experimental based investigation of device characteristics found DELTA to be consistent with conventional MOSETs and scalable as a 3-D device. Therefore, DELTA provided a good solution for the MOSFET device in sub-tenth micron technology [16].

Furthermore, in deep-sub-100 nm region a folded channel structure termed as FinFET, appropriate for terabit-scale integration was reported. This 30-nm gate length quasi-planar device was supposed to suppress SCEs due to the special features viz., vertical thin Si fin wrapped by self aligned double-gate and gates aligned to the source/drain. Its raised source/drain architecture reduced the parasitic resistance. Deposition of gate at low temperature and fabrication of thinner gate dielectric materials became possible as deposition was done after the source/drain. Despite its double-gate structure, fabrication process and layout of FinFET is compatible to the conventional MOSFET in terms of layout and fabrication. Experimental device characteristics of a 30 nm gate device were reported [17]. Improvement in the FinFET device design and process to circumvent the challenges due to further shrinking technology node continued for decades. Also, the invention of new device structures to consider the challenges faced at deep sub nano dimensions is still going on.

We organize the rest of our paper as follows: In Section II, we describe FinFET device, advancements in its design and technology, challenges faced by FinFET device with scaling such as process variations. In Section III we discuss brief overview of next generation novel semiconductor devices such as Gate all around FET, Vertical nanowire and nanosheet FET. In section V we demonstrate a comparative study of these devices. Section VI concludes the paper.

2 FinFET

Multiple-gate field-effect transistors (MGFETs) are considered as a substitute to the planar MOSFETs because they suppress SCEs because of higher gate control of the multiple gates over the channel and thus the influence of the the drain potential over the channel is reduced (i.e., higher gate-channel capacitance) [12, 18]. FinFET has a self-aligned triple gate structure (Fig. 1(a)) and can be fabricated with relatively planar-compatible fabrication process. Therefore, FinFETs have emerged as a promising solution to address scaling issues of planar devices and extend the CMOS scaling beyond the sub-22 nm node [19] due to their higher gate control and ease of manufacturing. Conventional devices and FinFET are described depending on their structural and characteristic differences as shown in Fig. 1 [20]. The characteristics of FinFETs are qualitatively similar to planar devices, making it easy to realize circuits using FinFETs [20]. 22 nm gate Si-FinFET has been in the industry since 2012. It has overcome the SCEs faced by conventional planar devices and enabled further scaling [21].

2.1 Advancements in FinFET Device Design and Technology

To improve circuit performance further, the researchers have suggested several improvements in FinFET device structure, process technology, and the use of high mobility channels (SiGe PFETs).

2.1.1 Fin Doping

Low-doped fin extensions are a solution to improve device performance due to better short channel immunity and lower parasitic capacitances [22]. Optimization of underlap/overlap length in a 7 nm-node FinFET is done in [22]. Long fin extensions with low doping reduce the band-to-band tunneling currents, total gate capacitance and parasitic capacitance, thus providing a smaller RC delay at the expense of reduced current drivability [22]. Junction dopant placement and S/D silicide engineering is used in order to achieve high I_{ON}/I_{OFF} ratios by eliminating GIDL (Gate induced drain leakage) in aggressively scaled FinFET devices [23]. In sub-10 nm technology regime, the source/drain extension doping profile is an important factor for performance enhancement [24, 25]. Device design can be optimized by controlling the vertical source/drain extension doping precisely. A 7% (10%) improvement in I_{ON} is achieved in 3-nm node N(P)

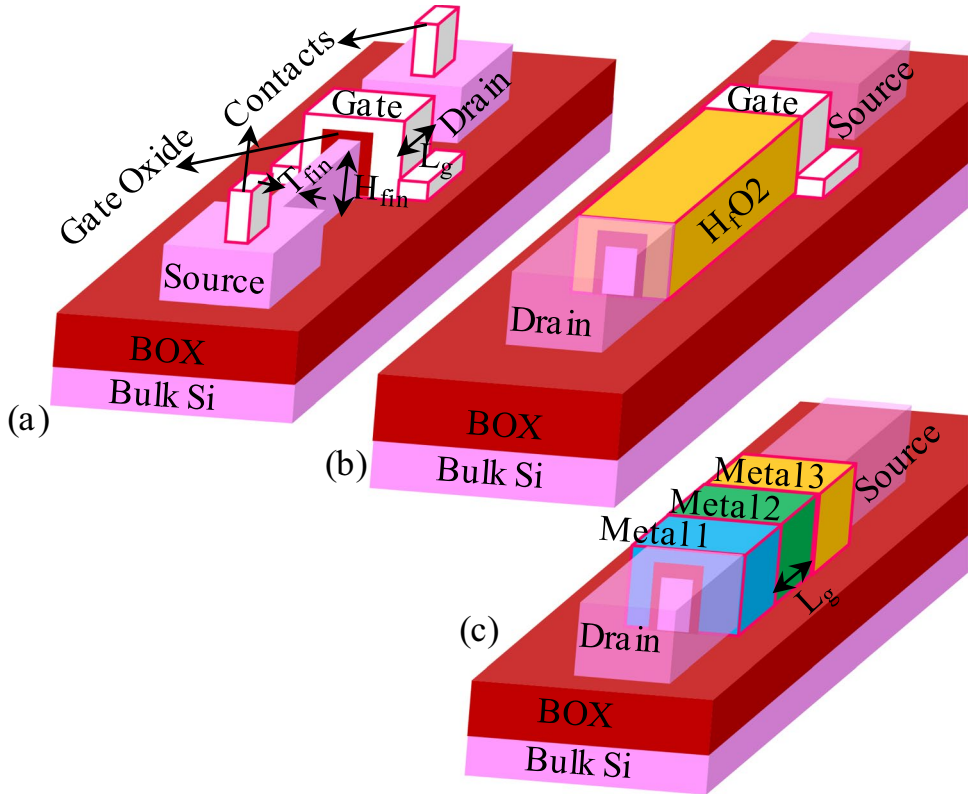

Fig. 1 Schematic of a (a) 3D FinFET structure (b) De-FinFET with high-K (HfO_2) over DE (c) Tri-material gate FinFET

FinFETs by using an optimal method for the 3-dimensional source-drain extension doping [26].

2.1.2 Use of High-K Gate Dielectric Materials

The use of high-K gate dielectric materials instead of conventional silicon dioxide is beneficial due to a drop in the gate to channel capacitance, parasitic outer fringe capacitance and a rise in internal fringe capacitance. The reduced parasitic outer fringe capacitance is useful in decreasing the circuit delay, whereas a decreased gate to channel capacitance and an increased internal fringe capacitance will deteriorate the power dissipation, and circuit's noise margin [27].

Recently, a drain-extended FinFET (De-FinFET) with an additional layer of High-k dielectric material was introduced for 10-nm gate length as shown in Fig. 1 (b). De-FinFET with additional high-k layer showed highly improved high voltage performance, improved I_{ON}/I_{OFF}, and smaller subthreshold swing as compared to the traditional De-FinFETs without the dielectric field layer. This reported device design De-FinFET with high-k dielectric material layer is expected to be replacing the conventional FinFET designs for high voltage system on chip applications [28]. Traditional De-FinFETs suffer from the high On resistance, hot carrier injection, and junction breakdown owing to the thin drain extended region [29–31]. Introducing the additional HfO_2 layer in DeFinFET shows improved breakdown voltage owing to the reduced electric field peak and optimally uniform distribution of electric field. Also, the On resistance is reduced because of high electron concentration in the drain extension originated due to the HfO_2 layer. Therefore, higher gate control over the drain extension by the high-k dielectric field layer alleviates the tradeoff between breakdown voltage and On resistance as compared to the traditional De-FinFET. The fabrication of this device design is possible with the improved FinFET process technology [32, 33]. Thus, De-FinFET with high-k dielectric field layer is a promising device design for high voltage applications in system on chip technology [28]. Nonetheless, De-FinFETs are extremely prone to electrostatic discharge than the stacked FinFET counterpart. In planar devices this issue was resolved by using a silicon-controlled rectifier (SCR) path in intrinsic De-MOS device [34]. In High Voltage De-FinFETs, missing SCR action is thoroughly studied, and as a result, a modified device is proposed, which offered a 3.5x improvement in failure threshold [35].

2.1.3 Strain

An improvement in the performance of pMGFET devices using strained SiGe in the source/drain regions is demonstrated in [36], It is demonstrated in [31] that introducing the recessed, strained $Si_{0.8}Ge_{0.2}$ in the source/drain of pMOS Multigate devices, I_{ON} is improved by 25% while keeping

I_{OFF} constant. Which results due to a smaller source/drain resistance and the resulting compressive channel stress [36]. Stress-induced fin dislocation results in defects which is critical if fins are narrow and tall. Detection and quantification of the fin dislocation defect has been reported [37].

2.1.4 Gate Engineering

Gate engineering allows the tuning of threshold voltage and off current (I_{OFF}) by adjusting the work function. Furthermore, the drive currents of FinFET devices can be improved further by using the raised source/drain (S/D) design to reduce the source-drain resistance significantly to its original one-eighth [38]. Use of tri-material gate in FinFETs i.e. different gate material over source extension, channel and drain extension (as shown in Fig. 1 (c)) showed that the surface potential, electric field and carrier velocity distribution is better as compared to the dual or single material gate [39].

High-k, metal-gate engineering and work function metal stacks have been used to achieve N/P FinFETs with multi-threshold voltages. This offers N/P devices to realize high performance and low power designs in integrated circuit design [40].

2.1.5 Optimizing the Geometrical Parameters

The effect of geometrical parameters such as fin thickness (T_{fin}) [41], T_{ox} [41] and fin height [42] on the properties of FinFET was discussed in [41, 42]. Dependence of the figure of merits of FinFET on T_{fin} is explained further in this paragraph. The I_{ON}/I_{OFF} current of the device increases with T_{fin}. The On current (I_{ON}) increases with T_{fin} because of the larger charge carriers and lesser series resistance of the source/drain extensions. However, thicker fin has poor control over SCEs [43] than that of thin Fin, as in former case channel barrier is reduced owing to the reduced source/drain-fin capacitances. In other words, DIBL is increased with increasing T_{fin} and hence the SCEs are increased. Consequently, the threshold voltage is reduced with a thicker fin due to the reduced quantum-mechanical confinement and increased SCEs, thereby increasing the I_{Off}. In general, a T_{fin} lying in the range of $L_g/4$ to $L_g/2$ is considered as optimum for immunity to parameter variability [41]. Dependence of the figure of merits of FinFET on the gate oxide is explained further in this paragraph. Reducing the T_{ox} increases the gate capacitance and hence the I_{ON} but at the expense of exponentially increased gate tunneling current.

Hence, because of this trade off, to maximize the I_{ON} while minimizing the leakage currents is not possible by tuning the T_{fin} and T_{ox} individually. Therefore, to design an optimized FinFET, T_{fin} and T_{ox} are simultaneously tuned and a combination of these values is obtained which provides the high I_{ON} while minimizing the leakage current. For 32 nm Lg, optimized device design has $T_{fin} = 8$ nm and $T_{ox} = 1.6$ nm [42].

Height of fin is another crucial geometric parameter tuned to minimize SCEs [44]. Driving strength of FinFET is mainly controlled by Fin height [45], therefore, increasing the Fin height increases off-state leakage current. Though, taller fins may reduce layout area, yet compromising the design flexibility. The fin aspect ratio Fin height/ Fin thickness = 3 as per the guideline by Si dry etch process, Fin height = 3 × Fin thickness = 2 × Gate length. Therefore, device width would be constrained to be an integer number of 4 × gate length [42].

3D FinFETs with a very high aspect ratio of fins ($H_{fin}/W_{fin} = 82.9$ nm/8.6 nm) are reported with30 nm gate length and gate dielectric nitrided oxide of 14 Å, using an advanced CMOS logic platform. TCAD simulations show that improved device performance is attained.

As the device dimensions are shrinking down with scaling, there are some challenges for maintaining the device performance. The self-heating effect in sub-14 nm regime affects the device characteristics significantly. It has been reported that the source/drain extension dimensions, doping concentration, fin width and fin height affect the heat dissipation and hence the thermal resistance [46]. Larger H_{fin} and W_{fin} result in increased I_{ON} and larger heat dissipation area. However, temperature is influenced more by the increased current than the heat dissipation area. Therefore, temperature increases and thermal resistance decreases with H_{fin} and W_{fin} [46].

In sub-10 nm technology regime, it becomes difficult to improve the device's figure of merits with scaling. Optimization of the geometrical parameters and minimizing the device parasitic allows the FinFET scaling to 7 nm technology node. Increasing the fin height improves the performance and area utilization [47]. However, device parasitic remain the challenging issue at 7 nm node. Also, reducing the number of fins decreases the dynamic power without compromising the speed [48]. Another limiting factor is the contact resistance because I_{ON} considerably degrades for aggressively scaled contacted gate pitch. However, for sub 7 nm technology regime, optimum dimension of the Contacted Gate pitch (CGP)/Metal Pitch (MP) are less than 45 nm/35 nm [48]. Therefore, to maintain the performance while scaling the CGP and MP beyond 30 nm, resistivity of the contact material/fully ohmic contacts should be upgraded to $\sim 8 \times 10^{-10}$ Ω-cm^2/ $\sim 1 \times 10^{-10}$ Ω-cm^2. Hence, the limits of material properties lead to the transition to alternative device structures, where, contact area is independent of CGP and scaling of CGP/MP is not required with device scaling [49].

With continuous improvements in process technology and deep analysis of the device physics, the scaling of FinFET is continued to 5 nm technology node. A 5 nm FINFET device based on classic 5 nm logic design rules

has been reported [50]. Considering the recent process technology with optimized process parameters the challenges of device performance, i.e. ~ 15% speed gain or 25% power reduction against the 7 nm device, were accomplished. Using ring oscillator simulations the performance per unit area was found to be similar to the industry reference results [50].

With recent advancements in the device architecture and technology, FinFETs have found applications in numerous fields like biosensors [15], neuromorphic applications [51], wireless communication [52], low power High performance computing applications [53] and many others. Biosensors based on Under-gate-dielectric-modulated (UG-DM) Junctionless FinFET detect the biomolecules using dielectric modulation approach. Threshold voltage of UG-DM Junctionless FinFETs is highly sensitive to channel dopping and volume of biomolecules filled in nanogap cavity. This makes it suitable to design biosensors [54]. Researchers have reported hafnium zirconium oxide based ultra-thin ferroelectric films that allows Fe-FinFET to be used for computing in memory applications [1–5]. However, deeply scaled Fe-FinFETs have problems of device variability [6, 7]. Truncated-fin (TF) FinFETs show higher linearity, lesser noise and high bandwidth down to 3 nm technology, which makes them suitable for wireless communication. A 7 nm node TF-FinFET with carbon nanotube based recessed channel has been reported to show better performance as compared to TF-FinFET [52].

For low-power High-performance computing applications air-trench-isolation between fins has been demonstrated in [53]. It has been shown that air space between the fins in the active region can be scaled, and this allows technology scaling down to 3 nm.

2.2 Impact of Process Variations on the Performance of FinFET

With continued scaling in sub-16 nm regime, dimensions of the device have turned very small and susceptiple to process induced variations [55–57]. Researchers have shown the dependence of the device characteristics on gate work function fluctuation [58], random dopant fluctuation [59, 60], line-edge roughness [61, 62], interface trap fluctuation [63], oxide thickness fluctuation [64] and some unidentified factors originating from the 3D FinFET structure. For instance, the contracted source/drain pads and the vertical construction of high-κ metal gate in bulk FinFETs causes large deviations in source/drain series resistance and capacitance [65–67] This is because the source/drain closeness and epitaxial shape and depth affects the electron mobility [67–69] and hence the device characteristics.

3 Next Generation Novel Semi-Conductor Devices

Technological advancements are continued to fulfill the challenge of scaling down the devices beyond 14 nm technology node. Figure 2 shows the technology roadmap for next generation transistors. Table 1 summarizes the challenges faced by the semiconductor devices at various technology nodes and solutions to overcome these issues. Characteristically, to facilitate the compensation for weak gate control due to SCEs, multi-gate devices; for instance, FinFET has been used extensively. In sub 14 nm technology regime, fin bridge defect becomes evident. Moreover, its impact increases with the scaling of the device dimensions. Researchers have given physical insights to the occurance of fin bridge defect and presented the possible solutions [70].

FinFET technology has been improving constantly down to 7-nm node. Fin/contact pitch has been decreased and aspect ratio has been increased to achieve the same [47, 71, 72]. However, this is restricted by fabrication limits of fin aspect ratio and fin pitch [73]. This leads to the development of new structures. Latest novel semiconductor devices suitable for sub 10-nm technology are described below.

Gate all around FET (GAA FET).

Vertical Nanowire.

Nanosheet FETs.

Schematic views of latest novel semiconductor devices are shown in Fig. 3 (a) GAA lateral NWFET (b) Lateral NSFET (c) GAA vertical NWFET structure (d) Vertical NSFET.

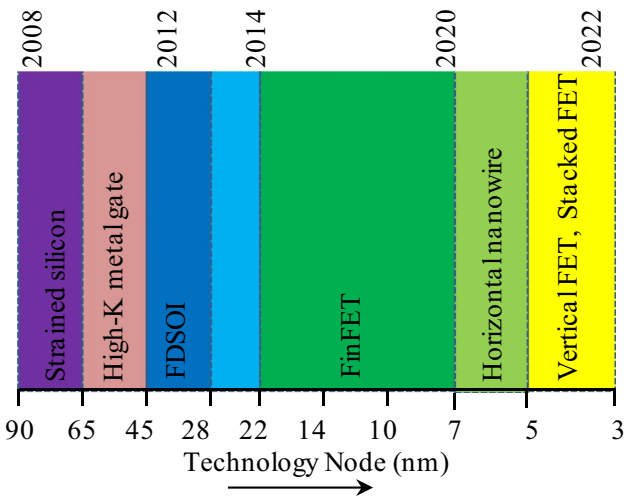

Fig. 2 Technology roadmap for semiconductor transistors

Table 1 Challenges faced by the semiconductor devices at various technology nodes and solutions to overcome these issues

Technology Node	Best Candidate	Challenges	solution
Sub-0.1 um	Planar MOSFET	Short channel effects limiting further scale down	High-K gate dielectrics, metal gate, and usage of strained silicon in planar MOSFET
Sub-32 nm	UTB SOI MOSFET	Leakage current, and variability	Ultra-thin body SOI nMOSFET
22 nm to 7 nm	Si-FinFETs	Further scaling required transition to new device	Multi gate transistors are used for better gate control
		FinFETs scaled below CGP of 40 nm	The contact resistivity (ρ_c) of ~8 $\times 10^{-10}$ $\Omega-$cm2 is required
		If FinFETs are to extend performance below CGP of 30 nm	Fully ohmic contacts i.e., ρ_c of ~1 $\times 10^{-10}$ $\Omega-$cm2 is requiredd
10 nm to 7 nm	Nanowire FET	Challenges to continue performance, power, area and cost improvement	Drain extended FinFET with high K field layer, Transition to lateral nanowires (NW), or to high mobility channels (SiGe PFETs)
Sub-7 nm	Nanosheet FET	Very high fin aspect ratio is required scaling is constrained by fin pitch, self heating effects, device parasitics	Vertically stacked Si-Gate-All-Around (GAA) nanosheet FETs (NSFETs)

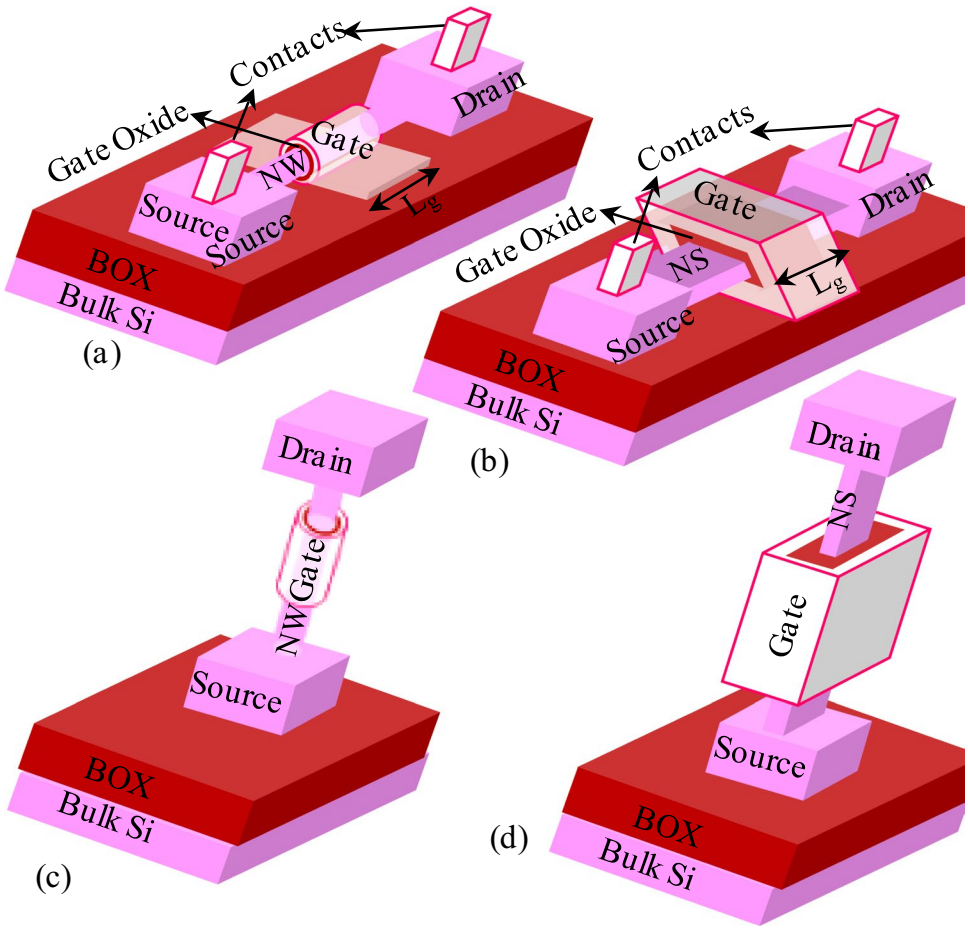

Fig. 3 Schematic of a (a) GAA lateral NWFET (b) Lateral NSFET (c) GAA vertical NWFET structure (d) Vertical NSFET

3.1 Gate all around FET

Device structure has further reformed in various ways to continue scaling in the sub-10 nm regime, while maintaining the performance and functionality, One implementation is Gate all around FET. Schematic view of GAA lateral NWFET is shown in Fig. 3 (a). It has gate wrapped all around the channel. The Gate All Around (GAA) structure provides for the greatest capacitive coupling between the gate and the channel. Aggressive scaling in sub-10 nm

regime is possible with the transition to this alternate device [49]. However, contact resistance remains the limiting factor for all horizontal transport transistors [49]. This constraint is resolved in a modified device architecture termed as vertical GAAFETs. Orientation of the channel and spacer is vertical, therefore, contact length and hence the contact resistance are not constrained by the scaled gate and spacer dimensions. Thus, it is assumed that contact resistance is not a limiting factor for scaling in vertical GAAFET unlike the conventional horizontal transport transistors [49, 74]. However, beyond 10 nm technology, resistance of source/drain extension and contact resistance have a major contribution of around 80–90% of the total resistance of middle of line [75–77]. Therefore, minimizing the parasitic resistance remains the challenge for device performance. A new metallization method using Co contact plug and the amorphous $CoTi_x$ barrier layer was proposed [77]. Small values of contact resistivity of 2.4e-9 Ω cm^2 and Schottky barrier height of 2 eV is reported with this method. The reported contact configuration is suitable beyond 10 nm technology [77]. GAAFET has improved electrostatic characteristics as compared to FinFET. However, the transition from FinFET to GAAFET can be accomplished with increased complications of fabrication. For extremely scaled transistor structures, satisfying the technical requirements viz., good gap filling, low Contact resistance, diffusion barrier property, and precise control of silicide thickness is a challenge [77]. Researchers have demonstrated that stacked Gate-All-Around structure shows improved device characteristics requirements for appropriate channel length [49, 78–80].

3.2 GAA Vertical Nanowire

Schematic view of GAA vertical NWFET structure is shown in Fig. 3 (c). Basic NWFETs were demonstrated using nanowire two decades back [81–83]. Though, the performance characteristics obtained were far from optimal, such as, less carrier mobility and variability issues. Since then, extensive research has underwent to improve the process, material and design of the structure. 22/10 nm gate length Si GAA NWFETs were studied in [83]. As compared to FinFET, a reduction in subthreshold slope andI_{OFF}, increment in I_{ON} and thus improvement of an order of magnitude in I_{ON}/I_{OFF} values was observed for 10 nm gate length. However, in the context of scalability, as compared to FinFET, GAA nanowire showed higher degradation in I_{ON}/I_{OFF} while scaling from 22 nm to 10 nm technology node. Furthermore, as compared to FinFET, GAA NWFET is considered more susceptible to variability.

Vertical nanowire FETs (VNWFETs), when compared to FinFETs and stacked lateral nanowire FETs, have the potential to reduce the contacted gate pitch induced parasitics due to the vertical orientation of the channel w.r.t the circuit wiring topology [84]. However, the fabrication process of VNFETS is more complex, series resistance is more challenging and thermal performance is poorer than that in FinFETs [85].

The NWFET delivers the highest I_{ON}/I_{OFF} ratio. These NWFET characteristics, together with the possibility of stacking them vertically [86–89], suggest that the NW architecture makes an excellent candidate for low power applications [89].

3.3 Vertical Nanosheet FETs

FinFET has scaling limits beyond sub-10 nm technology, thus, Nanoplate/Nanosheet FET structure was supposed to replace FinFET as a future device beyond this node [78, 90–92]. For technology nodes below 7 nm, this device structure named as GAA nanosheet FETs is being considered as a promising alternative. Schematic view of Vertical Nanosheet FET is shown in Fig. 3 (d). Vertical stacking makes the device capable of replacing Si-FinFETs owing to the better electrostatics below 7-nm node [89, 91, 93–95]. Impact of geometrical parameters on the dc performance of sub-7 nm node stacked NSFET has been studied in [96]. Level of channel stacking and reduced vertical pitch improves the circuit performance [96].. Impact of the nanosheet thickness/width on DC characteristics of the vertically stacked NSFET has been done. Though, I_{ON} and I_{OFF} increase with width and thickness values, the switching ratio, DIBL, and subthreshold slope are degraded. Device performance of NSFET has been analysed with channel scaling to ensure the device viability at smaller technology nodes. [97]

In ultra scaled regime, NSFET offers higher I_{ON} and improved sub-threshold characteristics, yet using a compatible fabrication process [89]. However, leakage current is the limiting factor in deep sub nano regime due to the parasitic channels beneath the intrinsic channels which in turn increase the leakage current [98]. NSFET suffers more owing to the broader parasitic channels as compared to FinFET. Furthermore, in deeply scaled regime, impact of process variation on AC/DC performance is an unavoidable issue. Source/drain process variation has a high impact as it impacts source/drain leakage current and the drive current. Researchers have reported the impact of the source/drain process variation such as source/drain epitaxial shape, depth [67, 99, 100], source/drain length [101, 102] and source/drain doping concentration [103] on FinFET. However, research on process induced variability on the vertically stacked NSFETs is yet to be done [73].

As a concluding remark, subthreshold performance of the devices (NSFET and FinFET) degrade more than the NWFET in ultra-scaled regime, therefore, transition to NWFET is required at this point. The NWFET provides lesser I_{OFF}, better subthreshold slope, and improved $I_{ON}/$

I_{OFF} ratio as compared to NS FET/ FinFET. This improvement in performance has been reported for gate length of 12 nm/8 nm. Though, NWFETs suffer from the earlier saturation of On current with the increasing gate voltage. Reducing the interface roughness and optimizing the doping profile, this issue can be handled. On the other hand, NSFET and NWFETs are stackable and hence offer the better packing density of transistors as compared to the alongside placed arrangement of FinFETs. [89]. NSFETs give an I_{ON}/I_{OFF} ratio 37% lesser as compared to the NWFET (Here, while comparing two different device architectures NWFET and NSFET, gate length is kept constant as 12 nm). However, in subthreshold regime, performance advantage is obtained to some extent as compared to FinFETs. NSFET offers largest I_{ON}, this makes NSFET a feasible substitute for the FinFET in high performance applications. The FinFET has an I_{ON}/I_{OFF} ratio 27% lesser than NSFET and 54% lesser than NWFETs. Though FinFET is more flexible to intrinsic variability than the NW FET [83], however, FinFET gives larger subthreshold slope and I_{OFF} because of the weaker control by the gate as compared to NSFET and NWFET. Even though NSFET provides the largest I_{ON}, NWFET offers highest I_{ON}/I_{OFF} ratio among FinFET, NWFET and NSFET at a cost of increased n-type source/drain doping. Increased n-type source/drain doping impacts the performance of the FinFET the most, which leads to the degraded sub-threshold performance and lowest I_{ON} [89]. Table 2 presents a comparative study of the figure of merits of FinFET, Nanosheet FET and Nanowire FET at 12 nm gate length. Table 2(a),(b) and (c) are for various values of source/drain doping as shown in Table 2(d).

Scaling the device further, researchers have presented a simulation based study of a 3 nm gate length NSFET. Using calibrated simulation set up, optimized device dimensions were obtained and device characteristics were studied. Contacted gate pitch is also scaled down according to the 3 nm technology node [104]. It is observed that for such ultra scaled dimensions, self heating effect becomes critical and affects the device performance [86, 105] Furthermore, extremely narrow channel has small heat dissipation, and hence self heating affects the device performance in an opposite manner [92].

Performance enhancement of stacked NSFET with source/drain contact engineering has been compared with conventional source/drain epi-based NSFET. Electrical/thermal characteristics of the device are improved by 10% using optimal M0-wrap and M0-trench-based NSFETs. Thus, for improved heat alleviation and improved I_{ON} the M0-trench-based NSHFET is a promising candidate [106].

A simulation based comprehensive investigation of RF/analog performance of vertically stacked NSFET have been done in [107]. It has been shown that vertically stacked

Table 2 Comparison of the figure of merits of FinFET, Nanosheet FET and Nanowire FET at 12 nm gate length. Table (a),(b) and (c) are for various values of source/drain doping as shown in (d)

		(a)	
Figure of Merit	FinFET	Nanosheet	Nanowire
Threshold Voltage (V_{th})	x	x	x
Threshold Voltage (Vt h)	1.13y	1.09y	y
Off- current (I_{off})	2.33z	1.9z	z
I_{on}/I_{off}	0.45w	0.63w	w
		(b)	
Threshold Voltage (V_{th})	0.89x’	0.93x’	x’
Sub-threshold slope (SS)	1.16y’	1.12y’	y’
Off- current (I_{off})	4.13z’	2.89z’	z’
On current (I_{on})	0.99 t’	1.13 t’	t’
I_{on}/I_{off}	0.23w’	0.39w’	w’
		(b)	
Threshold Voltage (V_{th})	0.83x”	0.88x”	x”
Sub-threshold slope (SS)	1.19y”	1.13y”	y”
Off- current (I_{off})	5.82z”	3.79z”	z”
On current (I_{on})	0.94 t”	1.09 t”	t”
I_{on}/I_{off}	0.16w”	0.29w”	w”
Figure of Merit	$N_{S/D}$ 5×10^{19} cm^{-3}	$N_{S/D}$ 1×10^{20} cm^{-3}	$N_{S/D}$ 1.5×10^{20} cm^{-3}
Threshold Voltage (V_{th})	x	x’ = 0.95x	x” = 0.91x
Sub-threshold slope (SS)	y	y’ = 1.01y	y” = 1.03y
Off- current (I_{off})	z	z’ = 1.53z	z” = 2.06z
On current (I_{on})	t	t’ = 1.28 t	t” = 1.44 t
I_{on}/I_{off}	w	w’ = 0.84w	w” = 0.68w

NSFET having smaller gate length and larger nanosheet width can be a promising candidate for high speed memory applications due to their better RF performance [107].

GAA NWFETs are one of the strongest contenders to replace the FinFETs because of their superior gate control but, their adoption implies a substantial change in the fabrication processes [108]. NSFETs have been proposed as an intermediate step while reusing, with minimal changes, its fabrication process. Between both architectures due to a slightly better performance than the FinFETs [89] while reusing, with minimal changes [78], its fabrication process [109].

4 Conclusion

With regress scaling in traditional CMOS technologies, the planar MOSFET device is restricted by the SCEs. In the 30-40 nm CGP region (contacted gate pitch region. a new scaling scheme needs to be where the contact length is independent of CGP to continue the power and performance benefits of CMOS scaling. Multiple gate transistors such as FinFET, Nanowire FET and Nanosheet FET have come out as the alternative devices in sub-22 nm technology regime. A detailed comparative study of the aforementioned devices shows that FinFET, Nanosheet FET and Nanowire FET are the preferred choices at current technology nodes. These semiconductor devices offer best performance characteristics when the optimized device configuration suitable for a given application is used.

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Declaration

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