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ORIGINAL PAPER

Double Metal Double Gate Hetero-oxide Tunnel FET: An Analytical Model

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Abstract
A 2-D compact analytical model for the device potential of double metal double gate hetero-oxide Tunnel FET (DM DG Hetero-oxide TFET) has been developed in this work. The hetero-oxide ($HfO_2 + SiO_2$) and the double metal double gate allows improvement in current in the ON state of TFET as well as suppresses the ambipolar current in TFET curtailing both the limitations of TFET. Parabolic approximation method with required boundary conditions has been utilized to solve Poisson's equation. Depletion region plays vital role in altering the potential of device in its proximity. Therefore, the depletion regions at drain and source are also considered for the modeling of the device. For this the effect of fringing field has been considered using the technique of conformal mapping in the depletion regions. The incorporation of the depletion region in potential modeling allows a precise modeling of the potential near channel-drain and source-channel junctions. The model results considering source and drain depletion region shows better match with simulation results. Validation of proposed model has done against simulation data using ATLAS TCAD SILVACO software. The compact analytical model developed here is found to have good agreement with the simulation framework.

Keywords Ambipolar suppression · Analytical modeling · Hetero-oxide · Potential · Tunnel FET

1 Introduction

With the advancement in the CMOS technology the size of chip is getting reduced due to the ultra-scaling of the transistor dimensions leading to a surge in the number of transistors. This causes an exponential rise in the density of the power in the chip. To limit the consumption of dynamic power to make it more suitable for the ultra low-power applications supply voltage scaling is done. However, to maintain the I_{ON} with the scaled supply voltage (V_{DD}), V_{TH} also need to be scaled down with respect to V_{DD} but the decrease in V_{TH} causes leakage current to rise exponentially. This then escalates the consumption of the static power. This surge in the leakage current/OFF state current is due to Boltzmann's tyranny, i.e. the limitation of subthreshold slope (SS) due to fermi distribution of charge carriers, at room temperature the minimum value of SS that can be achieved is 60 mV/decade . This requires exploration of new devices that consumes lesser power and can operate at low voltage and should also have low SS [1–4]. Tunnel field effect transistor (TFET) comes up as an optimistic candidate for the ultra low power applications. It has the ability to operate at very low supply voltage [5, 6] and it can also achieve better subthreshold characteristics [7], thus outperformes MOSFET [8]. This variation among the two is because of difference in their operating mechanisms. Band-to-band tunneling (BTBT) is the dominant mechanism for current conduction in TFET [9] whereas, for MOSFET current conduction is due to drift-diffusion. Meanwhile, TFET faces certain limitations such as low ON state current [8] and conduction at negative gate bias (ambipolar conduction) [8]. To utilize TFET for circuit designing, it is needed to improve the ON state current and to suppress the ambipolar current.

Researchers have explored numerous potential techniques like band gap engineering (replacing traditional Si channel with low band gap material like InAs, Ge, InGaAs, and SiGe) [10–12], gate work-function engineering (use of the gate contact metal of the suitable work-function) [13], source/drain material engineering (source/drain regions are made of the material with low band gap) [14, 15], channel

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strain engineering (strains are induced in channel region to increase the conductivity because of the increased mobility due to strain) [16], engineering in gate dielectric (high-κ gate dielectric) [17, 18], and multiple gate technique (introduction of double gate or triple gate to increase gate control) [12, 19] in order to boost the ON state current in TFETs. Further, the use of gate/drain underlap [20, 21], decreasing the concentration of doping on drain side [22], use of high band gap hetero-structure in drain side, increase in gap between gate and drain, and use of hetero-oxide to suppress the ambipolar current [23, 24].

Further, the mathematical modeling of the channel potential, electric field, threshold voltage and drain current of TFETs has granered huge research interest of the researchers. The model for the surface potential of DG TFET along with the effects of depletion regions at the source-channel and drain-channel junctions with high-k gate dielectric using pseudo-2-D model has been reported by Bardon et al. [25]. Model for DG TFET for its drain current has been reported by Pan and Chui [26] using quasi-analytical model. The model and comparison of the single gate (SG), double gate (DG), and gate all aroung (GAA) TFETs drain current characteristics have been reported by Verhulst et al. [27]. A compact analytical model for dual-material SG TFETs surface potential and drain current is reported by Vishnoi and Kumar [28]. The compact analytical model for SG TFETs drain current is also reported by Vishnoi and Kumar [29]. A set of generalized equation for DG and GAA TFETs electrostatics study is reported by Pan et al. [30]. Various compact models [31, 32] DG TFETs has been reported. A compact model for DG TFETs channel potential has been reported by Kumar et al. [31]. A compact analytical model for DG TFETs surface potential, electric field and drain current has been reported by Sarkhel et al. [32]. An analytical model for electrical characteristic of TFET with localized interface charge is reported by Kumar et al. [33]. An analytical model for triple metal double gate heterodielectric gate stack oxide is reported by Gupta et al. [34] without considering the depletion region. Further, performance improvement of TMDG TFET has been reported by [35]. However, no work has been done for mathematical modeling of double metal double gate hetero oxide TFET (DM-DG Hetero oxide TFET). This structure has the advantage that it achieves higher ON state current along with the ambipolar current suppression curtailing both the limitation of TFETs.

In this paper, mathematical expression for device potential has been developed using analytical modeling for DM DG hetero-oxide TFET. The double metal double gate structure improves the ON state current whereas hetero-oxide suppresses the ambipolar current. The solution of Poisson's equation has been found using parabolic approximation method and boundary conditions. The device potential is altered due to presence of depletion region at junction, in its nearby region. We have also considered source-drain depletion regions while modeling device potential. The fringing field in the depletion region is considered by the conformal mapping technique. The incorporation of these depletion region while potential modeling allows the precise modeling of the potential near the channel-drain and source-channel junctions. Further, the use of HfO_2 ($\varepsilon = 21$) oxide under the tunneling gate, i.e oxide near source region improves the ON state current. Whereas, use of SiO_2 ($\varepsilon = 3.9$) oxide under auxiliary gate, i.e oxide near drain region suppresses the ambipolar current. The results of analytical model has been compared with the simulation framework developed by deploying the ATLAS TCAD 2D device simulator [36] for claiming the model validity.

The organisation of remaining part of the paper is as follows: Section 2 contains the mathematical expressions for device potential modeling. Section 3 contains the result and discussion to validate the model with the simulation data and Section 4 finally concludes the work.

2 Potential Modeling

Figure 1 depicts the 2-D schematic view of the DM DG hetero-oxide TFET considered here to develop device potential model and its simulation. L is the channel length, L_1 and L_4 are depletion length at source and depletion length at drain, L_2 and L_3 are tunneling gate length and auxiliary gate length, t_{si} and t_{ox} is thickness of channel and the thickness of gate oxide. The device consists of double gate and each gate is composed of two different metals M_1 and M_2. The gate metal at source is termed as tunneling gate and gate metal at drain is termed as auxiliary gate. The origin of co-ordinate system is taken in the middle of channel thickness at the starting point of region 1, x-axis is across the length of channel and y-axis is across the thickness of channel as depicted in Fig. 1. Further, the potentials at x_0, x_1, x_2, x_3, and x_4 are ψ_0, ψ_1, ψ_2, ψ_3 and ψ_4, respectively.

Assuming $\psi_i(x, y)$ as the function for 2-D distribution of potential in the channel of device R_i (i = 1,2,3,4) with reference to the Fermi-potential. The Poisson equation in 2-D for different region is expressed as,

$$\frac{\delta^2\psi_i(x,y)}{\delta x^2} + \frac{\delta^2\psi_i(x,y)}{\delta y^2} = \pm\frac{qN_i}{\varepsilon_{si}} \qquad i = 1,2,3,4 \quad (1)$$

where, N_i is the concentration of doping in the region R_i. Here, plus sign is used for p-type doping concentration and minus sign is used for n-type doping concentration.

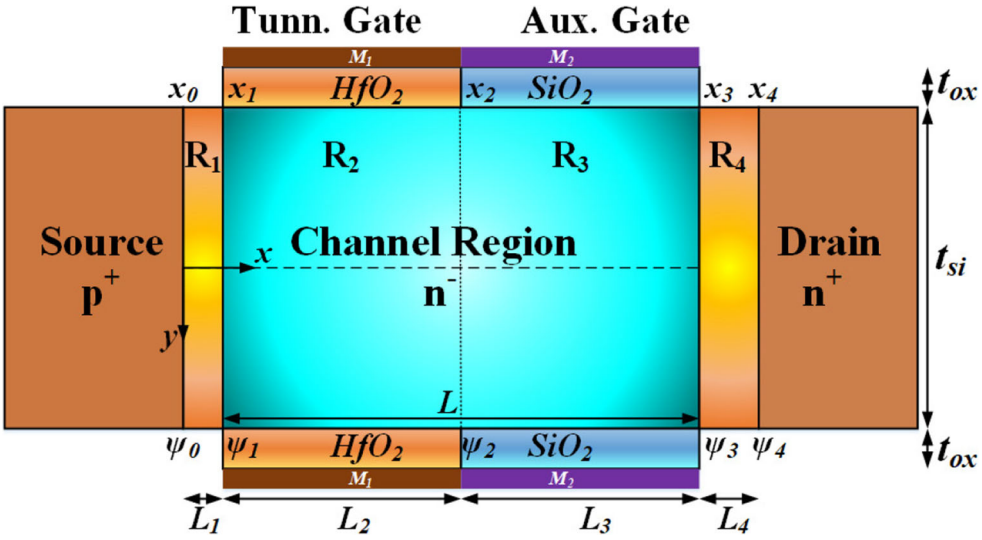

Fig. 1 2-D schematic of double metal double gate hetero-oxide Tunnel FET

Using parabolic approximation [17], $\psi_i(x, y)$ channel potential in 2-D in R_i (i = 1,2,3,4) is as

$$\delta\psi_i(x, y) = M_{0i}(x) + M_{1i}(x)y + M_{2i}(x)y^2 \tag{2}$$

Here, $M_{0i}(x)$, $M_{0i}(x)$ and $M_{0i}(x)$ are functions dependent on x which can be solved by using the given boundary conditions,

$$\left.\frac{\delta\psi_i(x, y)}{\delta y}\right|_{y=\pm t_{si}/2} = \pm\frac{C_{ri}}{t_{si}}[V_G{}_i^{ref} - \psi b/fs(x)] \tag{3}$$

Where, $\psi fs(x)$ and $\psi bs(x)$ is the front gate and the back gate surface potentials of the device, respectively. Further, $V_G{}_i^{ref} = V_{GS} - \phi_{msi} = V_{GS} - \phi_{mi} + \chi_{sub} + \frac{E_g}{2} + \phi_f$ represents the gate potential with reference to the Fermi potential. Here, ϕ_m is the work function of gate metal, χ_{sub} represents electron affinity for substrate semiconductor and C_{ri} is ratio of equivalent capacitance of gate oxide, say C_{oxi} in region R_i and capacitance of channel region $C_{ch} = \frac{\epsilon_{si}}{t_{si}}$.

Here, $C_{ox2} = \frac{\epsilon_{HfO_2}}{t_{ox}}$ in region 2 as gate oxide is HfO_2 and $C_{ox3} = \frac{\epsilon_{SiO_2}}{t_{ox}}$ in region 3 as gate oxide is SiO_2. Further, depletion region is considered by conformal mapping of fringing field in the depletion region R_1 and R_4 as $C_{ox1} = \frac{2}{\pi}C_{ox2}$ and $C_{ox4} = \frac{2}{\pi}C_{ox3}$ [37].

Using Eqs. 2 and 3, we obtain $M_{0i}(x) = \psi_{0i}(x)$, $M_{1i}(x) = 0$, $M_{2i}(x) = \left(V_G{}^{ref} - \psi_{0i}(x)\right)/\lambda_i{}^2$, where $\psi_{0i}(x)$ is the potential at y = 0 (in the middle of channel) in the region R_i and λ_i is given as,

$$\lambda_i = \sqrt{\frac{(4 + C_{ri})t_{si}^2}{4C_{ri}}} \tag{4}$$

It is the characteristic length of the device related to the potential in the middle of channel $\psi_{0i}(x)$.

The surface potential is represented by $\psi_{s,i}(x) = \psi_i(x, \pm t_{si}/2)$ in region R_i. The 2-D surface potential $\psi_{s,i}(x)$ and potential in channel $\psi_i(x, y)$ can be expressed as,

$$\psi_i(x, y) = \psi_{0i}(x) + [V_G{}^{ref} - \psi_{0i}(x)]\left(\frac{y}{\lambda_i}\right)^2 \tag{5}$$

$$\psi_{s,i}(x) = \psi_{0i}(x) + [V_G{}^{ref} - \psi_{0i}(x)]\left(\frac{t_{si}}{2\lambda_i}\right)^2 \tag{6}$$

At the middle of channel (y = 0), Poisson's Eq. 1 can be expressed as

$$\left.\frac{\delta^2\psi_i(x, y)}{\delta x^2}\right|_{y=0} + \left.\frac{\delta^2\psi_i(x, y)}{\delta y^2}\right|_{y=0} = \left.\frac{-qN_i}{\varepsilon_{si}}\right|_{y=0} \tag{7}$$

Using Eqs. 2 and 7, we can get the 1-D differential equation in terms of the middle channel potential/center potential $\psi_{0i}(x)$ as

$$\frac{\delta^2\psi_{oi}(x, y)}{\delta x^2} - \beta_i{}^2\psi_{oi}(x) = -\beta_i{}_i^2 \tag{8}$$

where

$$\beta_i{}^2 = \frac{2}{\lambda_i{}^2} \quad ; \quad P_i = V_G{}^{ref} + \frac{qN_i}{\varepsilon_{si}\beta_i{}^2} \tag{9}$$

The solution of Eq. 8 gives middle channel potential $\psi_{0i}(x)$ in the region R_i (i = 1,2,3), it can be written as

$$\begin{aligned}\psi_{oi}(x) = {} & A_i \exp\left(\beta_i\,(x - x_{i-1})\right) \\ & + B_i \exp\left(-\beta_i\,(x - x_{i-1})\right) + P_i\end{aligned} \tag{10}$$

Where, A_i and B_i are constants and can be solved using the following boundary conditions [37, 38]:

$$\psi_0 = \psi_1(0, y) = -V_T \ln N_1/n_i \quad (11)$$
$$\psi_1 = \psi_1(L_1, y) = \psi_2(L_1, y) \quad (12)$$
$$\psi_2 = \psi_2(L_1 + L_2, y) = \psi_3(L_1 + L_2, y) \quad (13)$$
$$\psi_3 = \psi_3(L_1 + L_2 + L_3, y) = \psi_4(L_1 + L_2 + L_3, y) \quad (14)$$
$$\psi_4 = \psi_4(L_1 + L_2 + L_3 + L_4, y) = V_T \ln N_3/n_i + V_{DS} \quad (15)$$
$$A_i = \frac{-1}{2sinh(\beta_i L_i)} (\psi_{i-1} exp(-\beta_i L_i) + P_i (1 - exp(-\beta_i L_i)) - \psi_i) \quad (16)$$
$$B_i = \frac{1}{2sinh(\beta_i L_i)} (\psi_{i-1} exp(\beta_i L_i) + P_i (1 - exp(\beta_i L_i)) - \psi_i) \quad (17)$$

where, $L_i = x_i - x_{i-1}$ is the length of the region R_i (i = 1,2,3,4) and $\psi_i = \psi_{s,i}(x)$ is the junction potential at the surface at $x = x_i$, as shown in Fig. 1.

The continuity property of electric field can be utilized at the interface at $x = x_i$ (i = 1,2,3), to write

$$\left.\frac{\delta\psi_{0i}(x)}{\delta x}\right|_{x=x_i} = \left.\frac{\delta\psi_{0i+1}(x)}{\delta x}\right|_{x=x_i} \quad at\, x = x_i \quad (i = 1, 2, 3). \quad (18)$$

The potential at surface $\psi_{s,i}(x)$ in R_i (for i = 1,2,3) of Fig. 1 is solved using Eqs. 6 and 10. Using the resultant $\psi_{s,1}$, $\psi_{s,2}$, $\psi_{s,3}$ and $\psi_{s,4}$ in Eq. 18 and solving the equations for i = 1,2, and 3, the junction potentials ψ_1, ψ_2, and ψ_3 can be expressed as

$$\psi_1 = \frac{1}{\rho_1} [\gamma_2\psi_2 - \gamma_1\alpha_1 - \gamma_2\alpha_2 + \gamma_1\psi_0] \quad (19)$$

$$\psi_2 = \frac{1}{\eta} [\gamma_3\alpha_3(\rho_1\rho_3 + \rho_1\gamma_3) + \rho_1\gamma_3\gamma_4(\alpha_4 - \psi_4) + \gamma_2\rho_3(\gamma_1\alpha_1 + \gamma_2\alpha_2) + \gamma_2\rho_3(\alpha_2\rho_1 - \gamma_1\psi_0)] \quad (20)$$

$$\psi_3 = \frac{1}{\rho_3} [\gamma_4\psi_4 - \gamma_3\alpha_3 - \gamma_4\alpha_4 + \gamma_3\psi_2] \quad (21)$$

where

$$\alpha_i = [1 - \cosh\beta_i L_i] P_i; \quad i = 1, 2, 3, 4 \quad (22)$$

$$\gamma_i = \frac{beta_i}{\sinh\beta_i L_i}; \quad i = 1, 2, 3, 4 \quad (23)$$

$$\rho_i = \beta_i \coth\beta_i L_i + \beta_{i+1} \coth\beta_{i+1} L_{i+1}; \quad i = 1, 2, 3 \quad (24)$$

$$\eta = \left(\rho_1\gamma_3^2 - \rho_3\gamma_2^2 - \rho_1\rho_2\rho_3\right) \quad (25)$$

The source-drain depletion lengths L_1 and L_4 can be given by [37, 38]

$$L_1 = f_1\sqrt{2\varepsilon_{si}(P_2 - \psi_0)/(qN_1)} \quad (26)$$

$$L_3 = f_2\sqrt{2\varepsilon_{si}(\psi_4 - P_3)/(qN_3)} \quad (27)$$

where f_1 and f_2 are the fitting parameters. Here, L_1 and L_4 are V_{GS} dependent due to V_{GS} dependence of P_2 and P_3.

3 Result and Discussion

In this section the comparison of the analytical model results with TCAD simulation data has been done for double metal double gate hetero-oxide tunnel FET (DM DG Hetero-oxide TFET). The models used for TCAD simulation are non-local band-to-band tunneling model along with SRH and auger recombination model. Further, band gap narrowing model, concentration and field dependent lombardi model has also been considered for precise modeling. The device physical dimensions taken for simulation have been listed in Table 1.

Figure 2 depicts the comparison of the potential of device across channel considering source and drain depletion region and without considering source and drain depletion region in analytical modeling with simulation results. It is observed that the model results considering source and drain depletion region shows better match with TCAD simulation results. Thus, the source drain depletion region have significant effect on device performance characteristics.

Figure 3 (a), (b), (c) and (d) compare the device potential along the channel for DM DG TFET with SiO_2, HfO_2+SiO_2 (HfO_2 under tunneling gate and SiO_2 under auxiliary gate because of its added advantage of high ON state current as well as ambipolar current suppression) and HfO_2 as gate dielectric for V_{GS} = 0 V and V_{DS} = 0 V (thermal equilibrium), V_{GS} = 0 V and V_{DS} = 1 V (OFF state), V_{GS} = 1 V and V_{DS} = 1 V (ON state), and V_{GS} = -1 V and V_{DS} = 1 V (ambipolar), respectively. The SiO_2 as gate dielectric suppresses the ambipolar current and HfO_2 as gate dielectric increases the ON state current but also allows ambipolar conduction, thus $HfO_2 + SiO_2$ (HfO_2 under tunneling gate and SiO_2 under auxiliary gate) utilizes the advantage of both i.e, increase in the ON state current and decrease in the ambipolar current. The model shows good match with device potential in the thermal equilibrium, OFF state, ON state and ambipolar conduction with SiO_2,

Table 1 DM DG hetero-oxide TFET device parameter

SYMBOL	PARAMETER	VALUE
N_1	Source doping	$1 \times 10^{20} cm^{-3}$
$N_{2,3}$	Channel doping	$1 \times 10^{16} cm^{-3}$
N_4	Drain doping	$1 \times 10^{18} cm^{-3}$
L	Channel length	50 nm
L_2	Tunneling gate length	25 nm
L_3	Auxiliary gate length	25 nm
t_{si}	Channel thickness	10 nm
t_{ox}	Gate oxide thickness	3 nm
$M_1 = \phi_t$	Tunneling gate work-function	4.2 eV
$M_2 = \phi_a$	Auxiliary gate work-function	3.9 eV

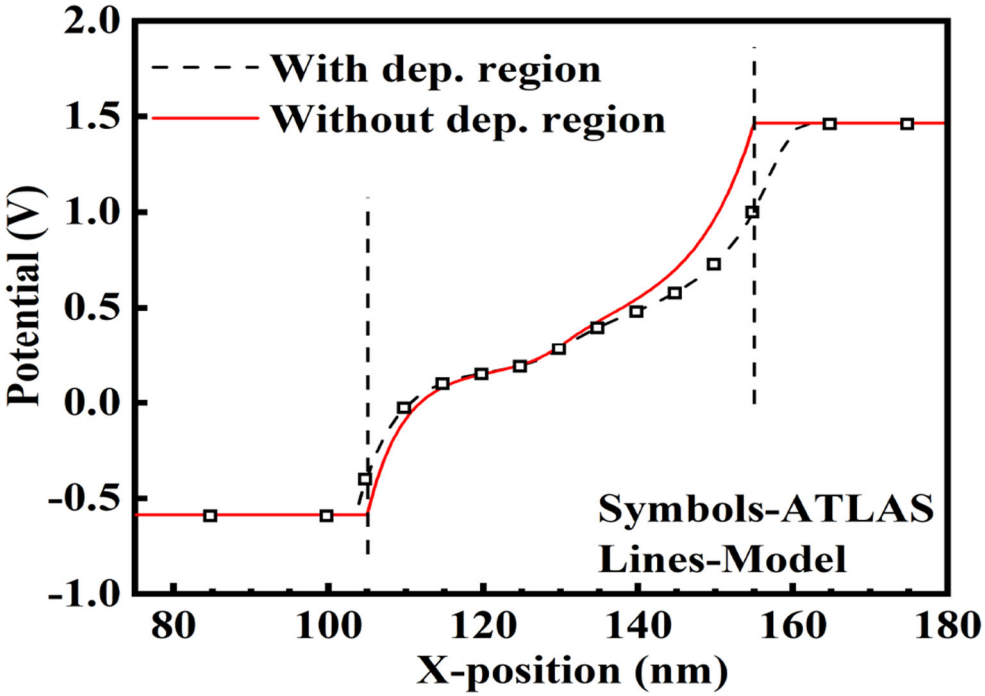

Fig. 2 Device potential along channel for different model (with source-drain depletion region and without source-drain depletion region) with hetero-oxide ($Hf O_2 + Si O_2$) at $V_{DS} = 1$ V and $V_{GS} = 0$ V

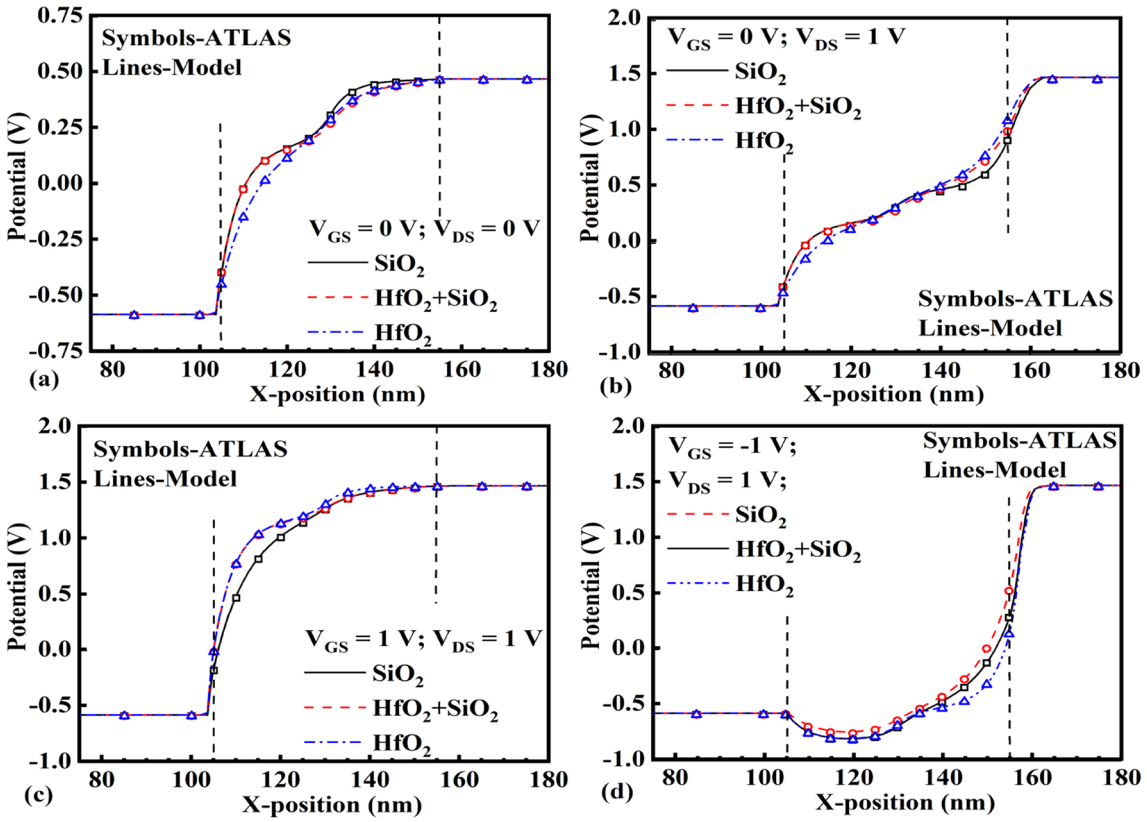

Fig. 3 Device potential along channel of DM DG TFET for $Si O_2$ as gate oxide, $Hf O_2$ as gate oxide and hetero-oxide ($Hf O_2 + Si O_2$) at (a) $V_{GS} = 0$ V and $V_{DS} = 0$ V (thermal equilibrium), (b) $V_{GS} = 0$ V and $V_{DS} = 1$ V (OFF state), (c) $V_{GS} = 1$ V and $V_{DS} = 1$ V (ON state), and (d) $V_{GS} = -1$ V and $V_{DS} = 1$ V (ambipolar)

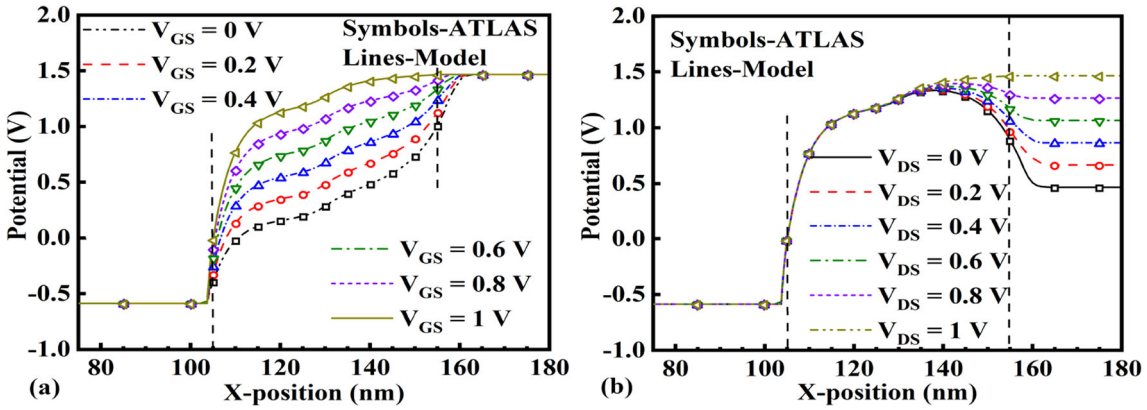

Fig. 4 Device potential along channel of DM DG hetero-oxide TFET with (a) V_{GS} variation at $V_{DS} = 1$ V, and (b) V_{DS} variation at $V_{GS} = 1$ V

$Hf\,O_2 + Si\,O_2$ ($Hf\,O_2$ under tunneling gate and $Si\,O_2$ under auxiliary gate) and $Hf\,O_2$ as gate dielectric with TCAD simulation framework.

Figure 4 (a) and (b) depict the comparison of the device potential across the channel for DM DG hetero-oxide TFET with control voltage (gate voltage) variation and supply voltage (drain voltage) variation, respectively. The increase in control voltage shows an increase in the device potential in channel region and an increase in supply voltage shows an increase in the device potential in drain region. This variation validates our model with respect to control and supply voltage. The model shows good match with TCAD simulation data for change in control voltage and supply voltage.

Figure 5 (a) and (b) depict the comparison of the device potential across the channel for DM DG hetero-oxide TFET with tunneling gate metal work-function (Φ_t) variation and auxiliary gate metal work-function (Φ_a) variation, respectively. The increase in Φ_t shows a decrease in device potential in tunneling gate region and increase in Φ_a shows a decrease in the device potential in the auxiliary gate region. The increase in the gate metal work-function increases the flat band voltage and decreases the effective gate voltage leading to a decrease in the device potential. Variation in (Φ_t) and (Φ_a) allows optimization of device potential and its performance. The model shows good match with TCAD simulation model for the change in Φ_t and Φ_a. This variation in Φ_t and Φ_a allows the optimization of the device performance.

4 Conclusion

In this work, a physics based 2-D compact analytical model of the device potential for double metal double gate hetero-oxide Tunnel FET (DM DG hetero-oxide TFET) has been developed. The double metal double gate and hetero oxide ($Hf\,O_2$ + $Si\,O_2$) curtails both the limitation of TFET by improving the current in ON state of the TFET and it suppresses the ambipolar current as well. Device potential is modeled by solving Poisson's equation with the help of parabolic approximation method with suitable boundary

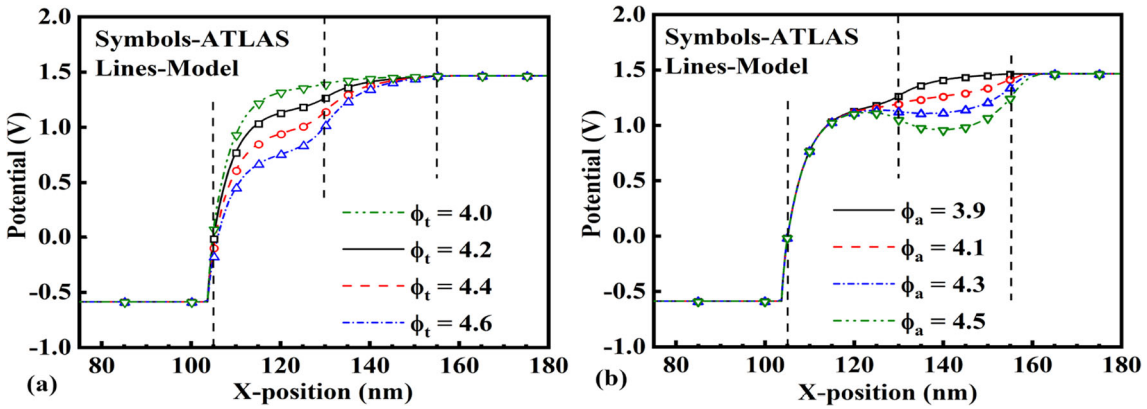

Fig. 5 Device potential along channel of DM DG hetero-oxide TFET at $V_{GS} = 1$ V and $V_{DS} = 1$ V with (a) Φ_t variation with $\Phi_a = 3.9$ eV, and (b) Φ_a variation with $\Phi_t = 4.2$ eV

conditions. The device potential is altered due to presence of depletion region at junction, in its nearby region. Source and drain depletion regions are also taken into account for device potential modeling. For this the effect of fringing field in the depletion region is considered by the method of conformal mapping. The incorporation of depletion region while potential modeling allows the precise modeling of the potential at the channel-drain and source-channel junctions. The validation of the proposed model is done against the simulation framework using ATLAS TCAD SILVACO tool.

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Author Contributions Kumari Nibha Priyadarshani has developed the model and the computational framework. Sangeeta Singh has devised the idea, helped while preparing the final draft and supervised.

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Availability of data and material No associated data.

Declarations

Ethics approval and consent to participate We comply to the ethical standards. We provide our consent to take part.

Consent for Publication All the authors are giving consent to publish.

Conflict of Interests No conflict of interest to disclose.

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