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ORIGINAL PAPER

Effects of Linearity and Reliability Analysis for HGO-DW-SCTFET with Temperature Variation for High Frequency Application

Manshi Kamal[1] · **Dharmendra Singh Yadav**[1]

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Abstract

This paper examines the effects of temperature variation on Hetero Gate Oxide Dual Work Function Step Channel Tunnel Field-Effect Transistor (HGO-DW-SCTFET). For different temperatures, the proposed device performs better in comparison with conventional Step Channel Tunnel Field-Effect Transistor (SCTFET). This study includes a temperature-based analysis on DC and Analog parameters like drain current, threshold voltage (V_{th}), Sub-threshold Slope (SS), I_{ON}–I_{OFF} ratio, trans-conductance, gate drain capacitance (C_{gd}), cut off frequency (f_T), Trans-conductance-frequency product (TFP), Trans-conductance generation factor (TGF), Gain Bandwidth Product (GBP), Transit Time (TT) to analyze its performance at various temperatures and various models named BT-BT, SRH, and TAT, along with the linearity analysis, and the reliability of the device. The variation in DC and Analog parameters shows that the proposed device can be used for the applications of high temperature. To examine the performance of the device, a wide range of temperatures of 250K to 400K has been taken in the TCAD simulator.

Keywords Temperature · Reliability · Linearity · BTBT · SRH · TAT · Hetero-gate-oxide · Dual work function

1 Introduction

Metal Oxide Semiconductor Field-Effect Transistors (MOS-FETs) played a very important role in the establishment of electronic industries. Development of the devices in the nano range raises convenience for users in terms of better functionality, higher speed, reduced power consumption, and reduced power supply voltage. However, dissipation of static and dynamic power, high gate leakage current, overheating, and Sub-threshold Slope limitation are the considerable problems to replace MOSFET with another field-effect transistor [1]. A Tunnel Field-Effect Transistor (TFET) has been used as a vigorous replacement for MOSFET with high leakage and high SS but they have some major concerns like low ON current and high ambipolar conduction [2–6]. These restrictions can be minimized by using structural variations with various methods and concepts [7–13]. Temperature analysis has been done on the HGO-DW-SCTFET to see its effect on device performance.

Semiconductors are temperature sensitive, whenever there is a change in temperature, the semiconductor changes its state of conductivity. At absolute zero temperature, tightly bound electrons by valence band are not able to cross the forbidden energy gap resulting in no free electron and no conduction. At room temperature, very fewer electrons cross the energy band-gap to reach the conduction band due to some heat and cause a very small current in the device. High-temperature breaks down some covalent bonds in the valence band and electrons become free to reach the conduction-band by leaving holes behind in the valence-band, called the generation of electron-hole pair to improve the current range. As temperature increases and decreases below room temperature some parameters are adversely affected so we have taken a varied temperature range from 250K to 400K to find its behavior in DC and Analog (RF) analysis [14–18]. In ON-state, drain current is influenced by the band/band tunneling (BTBT) mechanism for the transportation and this mechanism does not show many dependencies on temperature, however, temperature dependencies and OFF current are dominated by Trap Assisted Tunneling (TAT) [19, 20] and SRH mechanism

✉ Manshi Kamal
alpanakamal.555@gmail.com

Dharmendra Singh Yadav
dsyadav@nith.ac.in

[1] Electronics and Communication Engineering Department, National Institute of Technology, NIT Hamirpur, Himachal Pradesh, 177005, India

in the OFF-state of device. The release of electrons to a state (Trap-state) through the interaction of electron and phonon, following that tunneling into the conduction-band happens, is known as TAT. A hole emission and tunneling from a trap is also a possibility [21]. TCAD tool has been used to study the temperature-based analysis of the newly proposed HGO-DW-SCTFET. Further, the paper has been categorized as follows: Section 2 contains the structure of the device on which temperature analysis has been done and its simulation parameters. DC characteristics, Analog parameters, linearity analysis at various temperatures, and finally reliability issues of the device have been examined in Section 3. In the end, in Section 4, the dominant findings of the study are outlined.

2 Device Structure

In the silicon body, p+ doping (10^{20} $/cm^3$) and n+ doping (10^{18} / cm^3) are used to add the source region and the drain region respectively, while the intrinsic channel is doped with doping (10^{17} $/cm^3$), as shown in Fig. 1. Insulation of the device has been done using two different dielectric constant (high-k, low-k) materials where HfO_2 (ε= 22.0) has been included at the side of the channel-source junction to increase the tunneling of electrons from the valence-band of the source to the conduction band of the channel region by allowing more electric field permeation. Low-k dielectric (SiO_2 (ε =3.9)) is included at the drain-channel side for reducing bipolar conduction at the negative voltage.

Work function engineering has been implemented to enhance the Analog and DC performance of the device with Tunneling Gate (TG) having work function (Φ_2) of 4.3 eV and Auxiliary Gate (AG) having work function (Φ_1) of 4.5 eV. Lower gate work function is used to decrease Sub-threshold Slope (SS) and OFF current of the device. However, higher gate work function is used to boost ON current of the device. Design parameters of the device HGO-DW-SCTFET has been listed in Table 1.

The structure of the presented device and its simulations have been designed and performed by a TCAD simulator. Different models like bbt. nonlocal, bgn, conmob, consrh have been used to analyze the physical effects of the device.

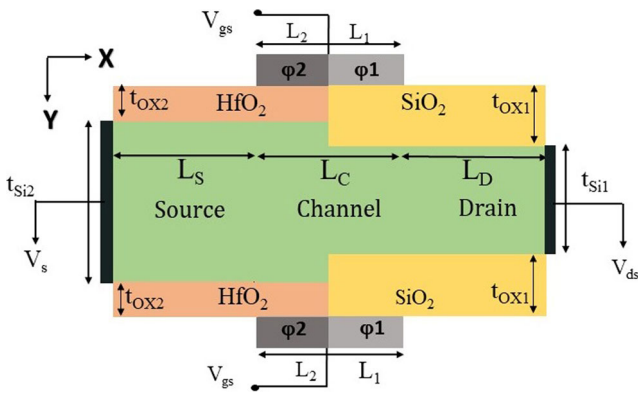

Fig. 1 Schematic of the proposed device HGO-DW-SCTFET

3 Results and Parameter Analysis

3.1 DC Characteristics

The drain current variation in log scale with gate voltage has been shown in Fig.2 which is also called transfer characteristics of the device. As V_{gs} increases energy bands of the channel region start coming down to match the level of the source region and this helps the movement of the electron from the valence-band of the source to the conduction-band of the channel which results in increasing drain current. In Fig.3, energy band diagrams of the device at different temperatures ranging from 250K to 400K with a difference of 50K have been shown to analyze device behavior at various temperatures. The conduction-band and the valence-band energies of the device, increase with increasing temperature. In contrast to the conduction band, the valence band shifts more with temperature. As a result, the energy band gaps of HGO-DW-SCTFET shrink as the temperature rises [22–24]. This can be explained with help of the energy band gap equation for the different temperatures, given by the Eq. 1

$$E_g(T) = E_g(0) - \frac{\alpha T^2}{T + \beta} \tag{1}$$

Table 1 Design parameters of HGO-DW-SCTFET

Parameters	HGO-DW-SCTFET
Source Length (L_S)	20 nm
Channel Length (L_C)	10 nm
Channel Length (L_D)	20 nm
Source doping (p-type)(N_S)	10^{20} $/cm^3$
Channel doping (n-type)(N_{CH})	10^{17} $/cm^3$
Drain doping (n-type)(N_D)	10^{18} / cm^3
Oxide thickness at DC-junction (t_{OX1})	2 nm
Oxide thickness at SC-junction (t_{OX2})	1 nm
Drain thickness (t_{Si1})	6 nm
Source thickness (t_{Si2})	8 nm
Gate length (L_1)	5 nm
Gate length (L_2)	5 nm
Gate work function (AG=Φ1)	4.5 eV
Gate work function (TG=Φ2)	4.3 eV

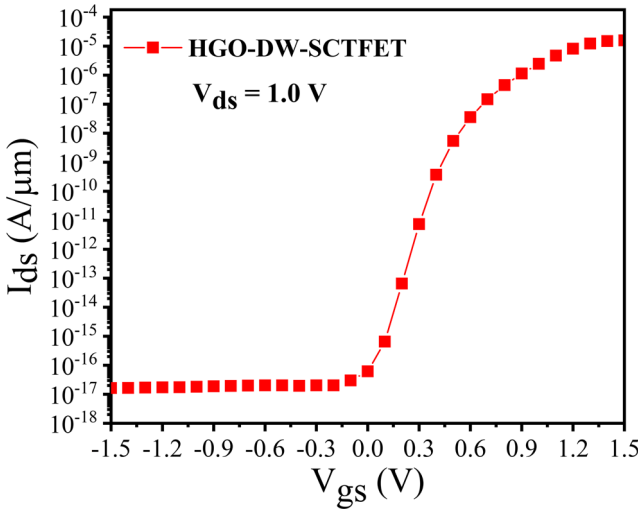

Fig. 2 Transfer characteristics of HGO-DW-SCTFET

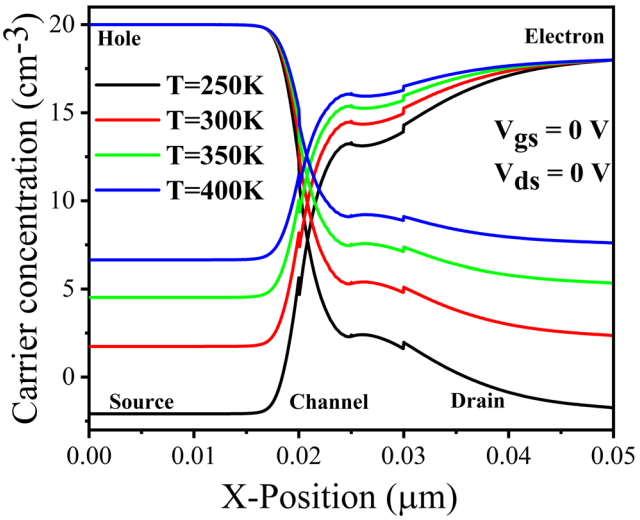

Fig. 4 Electron - hole concentration of HGO-DW-SCTFET at various temperatures

In this equation, α, β = fitting parameters of the material, $E_g(0)$ = energy band gap (EBG) at 0K, $E_g(T)$ =EBG at different temperatures, T = absolute temperature.

The carrier concentration of the device at different temperatures has been depicted in Fig. 4. There are no inherent electron-hole pairs at very low temperatures because the donor atoms have donor electrons bound to them which is called the ionization region. At 400K temperature, electrons number is comparatively higher than other temperatures on the source side which result in a high current in the condition of ON-state [25]. Higher temperature provides the thermal energy which helps in breaking the covalent bonds, when it happens, more donor electrons become free from the donor state to go to the conduction band where they help in more conduction. In Fig. 5, linear characteristics show that for lower temperature, the current is low and for higher temperature, the current has increased. The movement of electrons from one energy level to different energy levels is not much affected by the temperature, in the case of TFET, the current will be significantly less temperature-dependent. High temperature increases the diffusion component of ON-state current, but as temperature increases, the charge carrier's mobility increases and this incremented mobility assists charge carriers to collide with each other. This collision degrades their mobility which results in the degradation of the drift component of drain current which is why slight variation happens for the drain current in ON-state. In OFF-state, a large variation in currents can be seen at different temperatures.

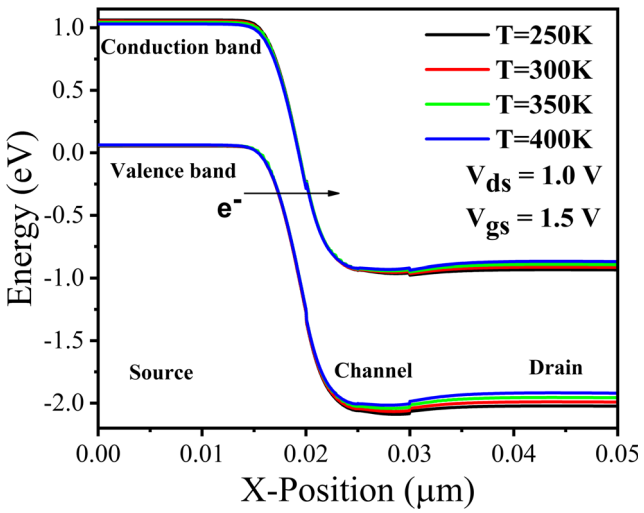

Fig. 3 Energy band profile of HGO-DW-SCTFET at different temperatures

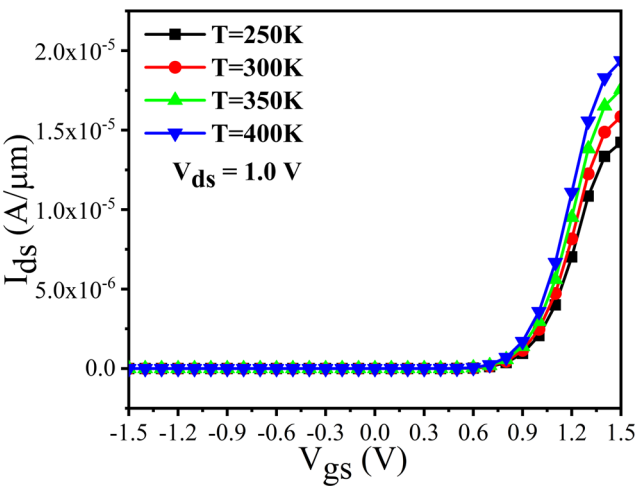

Fig. 5 Transfer characteristics of HGO-DW-SCTFET at different temperatures in linear scale

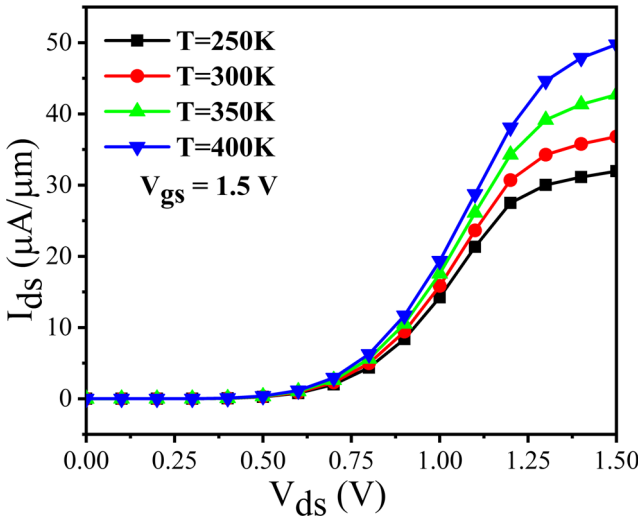

Fig. 6 Output characteristics of HGO-DW-SCTFET at various temperatures

Figure 6 shows drain current variation with drain voltage. At a lower value of V_{ds}, drain current increases linearly but at a certain value of V_{ds}, they start being saturated and no further current increment happens. Temperature variation shows that the highest saturation point gained by I_{ds} at 400K and the lowest saturation point is gained by the I_{ds} at 250K. The high temperature helps to break more bonds to create a large number of electrons and electron tunneling happens when V_{gs} is applied. Increased V_{ds}, increases the depletion width which stops the drain current to increase further, called the saturation point where more increment in V_{ds} does not affect the current.

3.2 Off-State Analysis

OFF-state current has a significant effect on the device performance, because the I_{ON}–I_{OFF} ratio is extremely affected. Less OFF current improves the I_{ON}–I_{OFF} ratio which directly enhances device performance. We have explored DC characteristics at various temperatures, EBG, electron-hole concentration in the previous section to examine its consequences on the proposed device. In this section, we have investigated the impact of temperature on drain current, SS, V_{th}, I_{ON}–I_{OFF} ratio, and OFF-state behavior of the device at different temperatures and different models such as TAT, SRH, and BTBT [26].

$$T(E) = \exp\left[-\frac{4\sqrt{2m^*}E_g^{*3/2}}{3h|e|(E_g^* + \Delta\varphi)}\sqrt{\frac{\epsilon_{\mathrm{si}}t_{\mathrm{ox}}t_{\mathrm{si}}}{\epsilon_{\mathrm{ox}}}}\right]\Delta\varphi \tag{2}$$

$$R_{\mathrm{SRH}} = \frac{pn - n_{ie}^2}{TAUP0\left[n + n_{\mathrm{ie}}\exp\left(\frac{ETRAP}{kT_{\mathrm{L}}}\right)\right] + TAUN0\left[p + n_{\mathrm{ie}}exp\left(\frac{-ETRAP}{kT_{\mathrm{L}}}\right)\right]} \tag{3}$$

$$R_{\mathrm{TAT}} = \frac{pn - n_{ie}^2}{\frac{TAUP0}{1+\Gamma_p^{DIRAC}}\left[n + n_{\mathrm{ie}}\exp\left(\frac{ETRAP}{kT_{\mathrm{L}}}\right)\right] + \frac{TAUN0}{1+\Gamma_n^{\mathrm{DIRAC}}}\left[p + n_{\mathrm{ie}}\exp\left(\frac{-ETRAP}{kT_{\mathrm{L}}}\right)\right]} \tag{4}$$

The effect of BTBT, SRH and TAT can be analyzed from Eqs. 2, 3, and 4 respectively. So from the Eq. 2 it can be explained that electron tunneling depends upon various factors like silicon body dielectric constant (ε_{Si}), oxide dielectric constant (ε_{OX}), oxide thickness (t_{OX}), silicon body thickness (t_{Si}), work function of gate electrode ($\triangle\Phi$), material's energy band gap (E_g^*), carrier's effective mass (m^*), reduced plank constant (h), and charge of electron (e). The rate of SRH recombination has been depicted in the Eq. 3, where k is Boltzmann constant, T_L is the temperature, n_i is intrinsic concentration, E_{TRAP} is trap energy level, p is hole concentration, n is electron concentration, TAU_{P0} is hole lifetime, and TAU_{N0} is electron lifetime. The rate of recombination for TAT shown in the Eq. 4 and it is dependent on all of the factors that influence SRH, as well as field-effect functions (Γ_p^{DIRAC}, Γ_n^{DIRAC}).

From Fig. 7, it is noticeable that high temperature reduces the V_{th} and increases the drain current because at the drain-channel junction the tunneling width is reduced due to high temperature which helps more tunneling of holes from the conduction-band of the drain to the valence-band of the channel region in the OFF-state which results in a low I_{ON}–I_{OFF} ratio. Figure 8 depicts the behavior of SS and V_{th} towards different temperatures. The temperature is directly proportional to the Sub-threshold Slope which results in SS increment as the temperature increases, while V_{th} decreases. I_{ON}–I_{OFF} ratio variation with temperature is depicted in the Fig. 9, where the I_{ON}–I_{OFF} ratio for

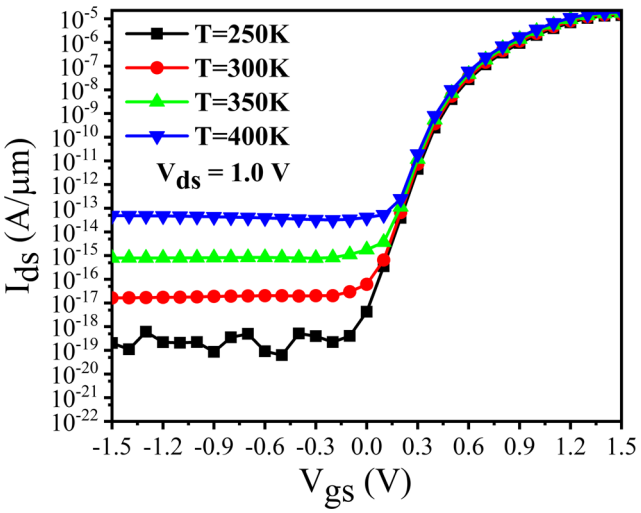

Fig. 7 Transfer characteristics of HGO-DW-SCTFET at various temperatures in logarithmic scale

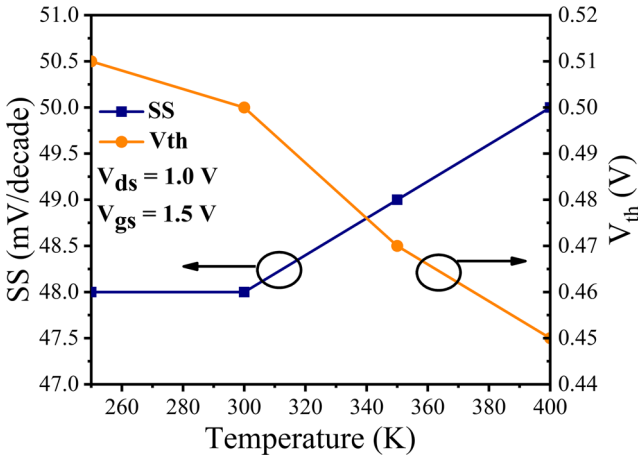

Fig. 8 Variations of SS and V_{th} with temperature

lower temperatures is very large due to very low off current, while the I_{ON}–I_{OFF} ratio for higher temperatures is very low due to very high OFF current.

Figure 10 demonstrates how the Trap Assisted Tunneling (TAT) mechanism along with a formalism of Shockley-Read- Hall contribute a significant path of the leakage current before the BTBT is initiated in HGO-DW-SCTFET. The rate generation of electron and hole pairs in the existence of traps is described by the classical SRH formalism. A phonon can be absorbed by an electron in the valence-band (VB) to enter a state (Trap state) before moving to the conduction-band (CB) through another phonon interaction. Traps greatly increase carrier capture rates, allowing the leakage current to outnumber the desired current because TAT is so reliant on the electric-field, any attempt to boost the BTBT current by strengthening the local electric-field also enhances the leakage current.

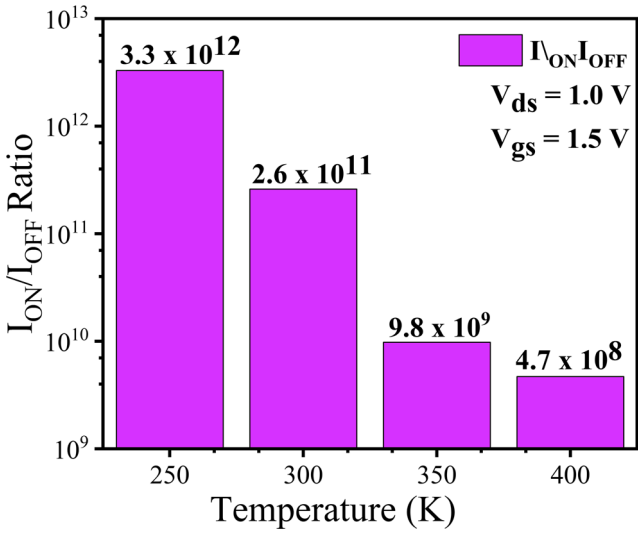

Fig. 9 Variations of I_{ON}–I_{OFF} ratio with temperature

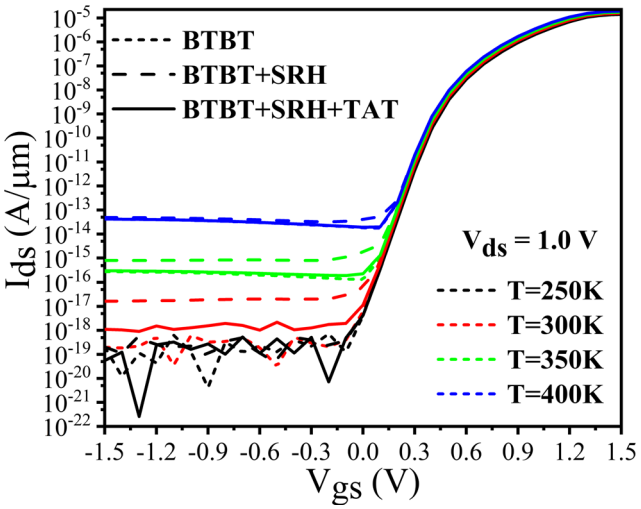

Fig. 10 Variations of I_{ds} with gate voltage at various temperatures and at different models

TAT has an impact on the I_{ON}–I_{OFF} ratio as well as the SS. The total current comes primarily from BTBT when the threshold voltage is exceeded. The generation rate of electrons and holes is reduced at lower temperatures, resulting in a shorter TAT. Temperature has a weak effect on I_{ON} above the threshold voltage, but it has a strong effect on I_{ON} below the threshold. The BTBT mechanism is not enabled at negative V_{gs} because the distance from the valence to conduction bands is too great. SRH is the most common phenomenon in a negative voltage range. Trap-assisted tunneling is triggered by raising the gate voltage, and when V_{gs} = 0 V, TAT and BTBT, both are operating together. TAT (Trap-Assisted-Tunneling) and SRH (Shockley–Read–Hall) recombination components become primarily responsible for the off-state current [19–21]. So, it can also be stated that these models do not have any vital effect on drain current in ON-state condition, however, OFF-state current is extremely affected by these models and temperature variations. The Off-state value of SRH and TAT currents becomes very high for high temperatures.

3.3 Analog/ RF Characteristics

In Fig. 11, trans-conductance variation with V_{gs} and temperature can be seen. The reason behind the increment of the g_{m1} depends on the variation in drain current. The relationship between drain current and g_{m1} is shown by the Eq. 5.

$$g_{m1} = \frac{\partial I_d}{\partial V_{gs}} \tag{5}$$

As drain current is enhanced with the gate voltage, g_{m1} increases with the same proportion. Whenever the saturation

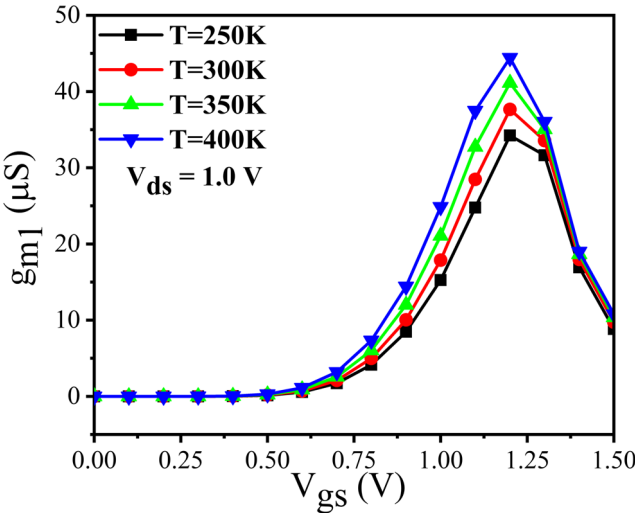

Fig. 11 Trans-conductance (g_{m1}) variations with gate voltage at different temperatures

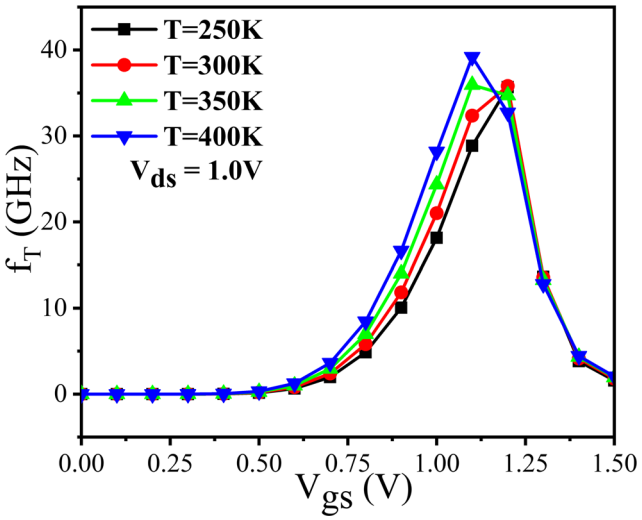

Fig. 13 Cut-off frequency variations with V_{gs} at various temperatures

point of drain current starts, the decrement of g_{m1} starts taking place with the increased value of V_{gs}. Like the behavior of drain current, at higher temperature, g_{m1} shows its higher peak. The effect of the C_{gd} at the output of the device can be analyzed from the graph in Fig. 12. Initially, it does not show much effect but with increment of V_{gs}, it starts increasing. Furthermore, unlike MOSFETs, which have a significant reverse bias, TFETs have a very small potential drop at the drain–channel junction. In TFETs, this results in a higher gate-to-drain capacitance (C_{gd}) than in conventional transistors. Cut off frequency is a frequency level above or below where a device fails to operate. Its variation with V_{gs} and temperature has been shown in Fig. 13, where it achieves a peak value at some gate voltage and after that it starts decreasing showing a relationship with

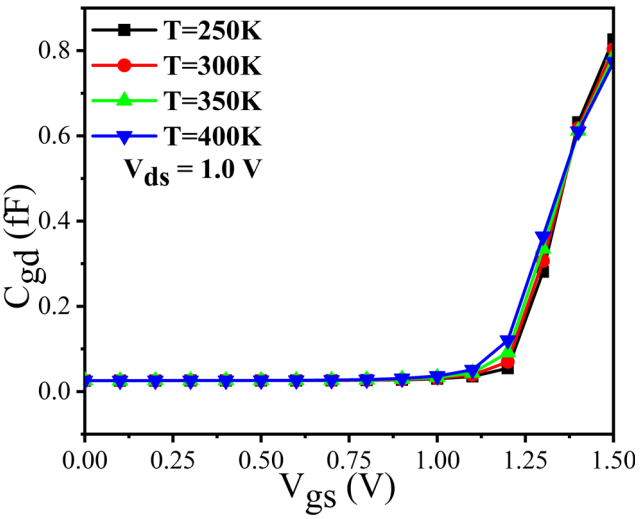

Fig. 12 Gate-drain capacitance (C_{gd}) variations with gate voltage at different temperature

g_{m1} and drain current that can be described from the Eq. 6 given below.

$$f_t = \frac{g_{\mathrm{m1}}}{2\pi(C_{gs} + C_{gd})} \tag{6}$$

Temperature sensitivity analysis in Fig. 13 shows that at higher temperature, f_T depicts higher peak. Gain bandwidth product defines the product of bandwidth and gain at which bandwidth is measured. GBP can be defined by the Eq. 7.

$$GBP = \frac{g_{\mathrm{m1}}}{2\pi C_{gd}} \tag{7}$$

Equation 7 shows direct proportionality between GBP and g_{m1}. It achieves the highest peak as g_{m1} achieves with the increment of the gate voltage and further increment in V_{gs} makes a fall in GBP value. The reason behind this event is that the proportionality of g_{m1} and I_{ds} increases the GBP due to increment in itself but at the saturation point of current g_{m1} starts decreasing which affects the GBP. Inversely proportional C_{gd} also affects the GBP, increasing the value of C_{gd} decreases the GBP. In Fig. 14, the GBP of the device gets higher value as the temperature increases. Trans-conductance-frequency product (TFP) is a device parameter that describes the performance of the device at the operating frequency. The TFP reflects a trade-off between power and bandwidth and is used in moderate-to-high speed designs. The relationship of TFP with g_{m1}, f_T and I_{ds} has been shown in the Eq. 8. This equation tells that TFP is highly dependent upon g_{m1}, f_T and I_{ds}, so increase in the value of g_{m1} and f_T concerning V_{gs}, enhance the value of TFP but after the saturation, current stops increasing and stops affecting the TFP, while the decrement of g_{m1} and f_T make the fall in the value of TFP.

$$TFP = \frac{g_{\mathrm{m1}} f_T}{I_d} \tag{8}$$

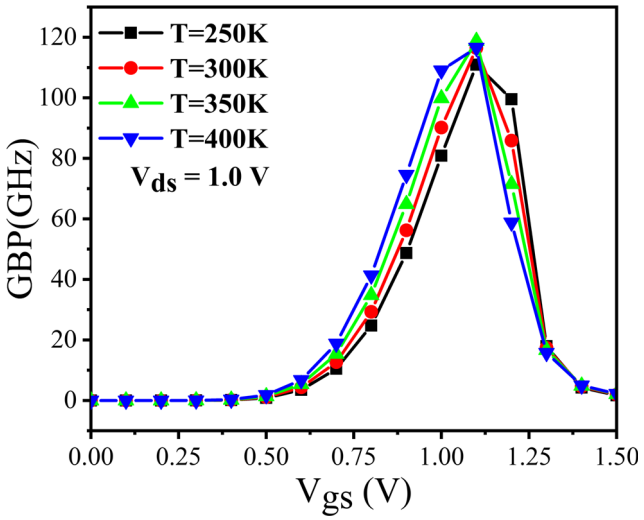

Fig. 14 Gain-bandwidth product variations with gate voltage at various temperatures

High temperature boosts the value of the TFP parameter of the device that is shown in Fig. 15. Trans-conductance generation factor (TGF) is a parameter of performance for devices that depicts device efficiency. The graph in Fig.16 shows the relationship of TGF with V_{gs} and varied temperatures.

$$TGF = \frac{g_{\mathrm{m1}}}{I_d} \tag{9}$$

Direct proportionality of g_{m1} and indirect proportionality of I_{ds} with TGF are shown in the Eq. 9. From the transfer characteristics it has been concluded that for 400K drain current achieves high value and here TGF is indirectly proportional with I_{ds} that tells that TGF achieves lesser value for 400K and higher value for 250K. In Fig. 17 transit

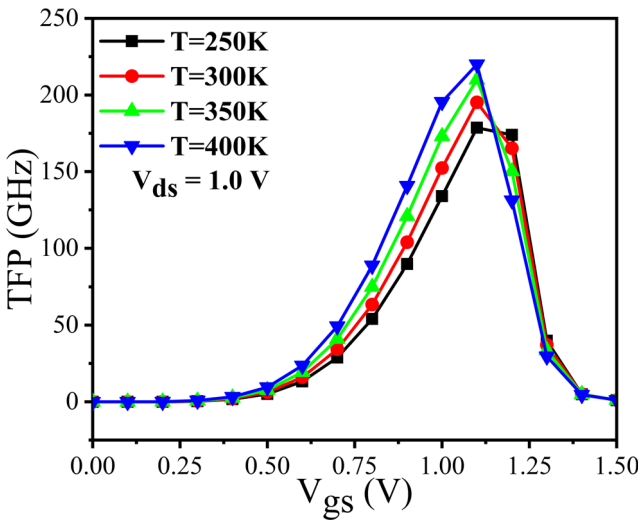

Fig. 15 TFP variations with gate voltage at different temperatures

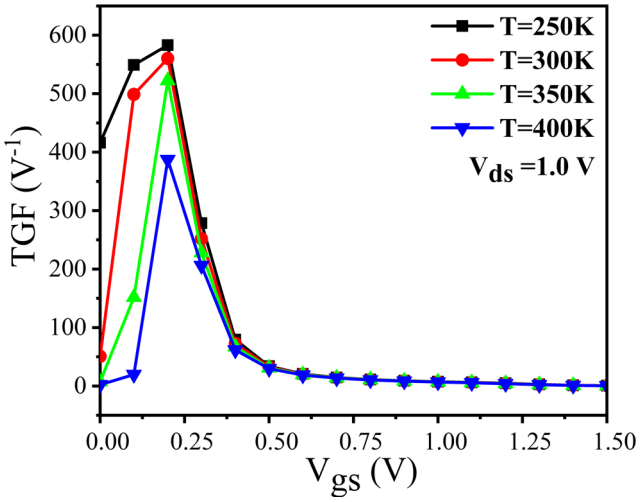

Fig. 16 TGF variations with V_{gs} at different temperatures

time of HGO-DW-SCTFET has been graphed concerning V_{gs}.

$$\tau = \frac{1}{2\pi f_t} \tag{10}$$

Transit time (TT) examines the device's performance in terms of speed. TT can be calculated from the Eq. 10. Initially, when V_{gs} is applied an increased transit time of device for different temperatures starts to decrease and this decreased transit time lessens the delay of the device which improves the device's speed.

3.4 Linearity Analysis

Linearity analysis ensures that the signal in the system is distorted as little as possible, making it suitable for low-noise applications [27]. Trans-conductance coefficients

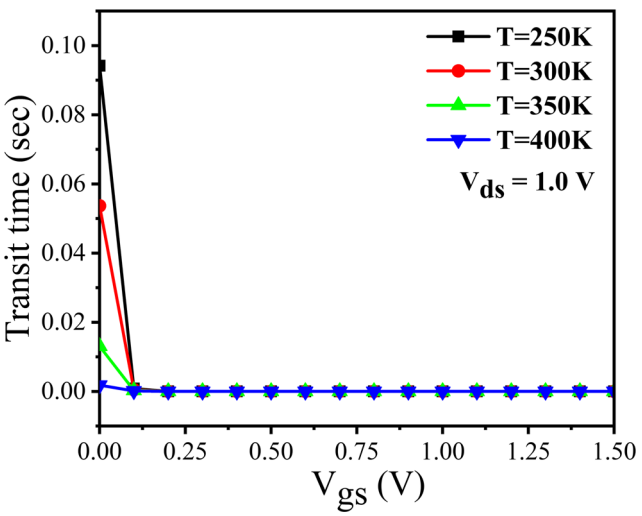

Fig. 17 Transit time variation with V_{gs} at various temperatures

(g_{m1}, g_{m2}, g_{m3}), Voltage-Intercept-Points (VIP_2, VIP_3), Input-Intercept-Point (IIP_3), Inter-Modulation Distortion (IMD_3) control linearity. Trans-conductance coefficients (g_{m1}, g_{m2}, g_{m3}) are the dominant parameters to define the linearity of the device. All other parameters for linearity are totally dependent upon trans-conductance coefficients. In the section of Analog analysis, g_{m1} has been described in Fig. 11 and in this section g_{m2} and g_{m3} are defined. Lower limit of distortion is governed by g_{m2} and g_{m3}, which explains that the value of g_{m2} and g_{m3} should be small. g_{m2} is basically known as the second derivative of drain current which can be described by the Eq. 11. The low value of g_{m2} provides better linearity by reducing distortion. Variation of g_{m2} with gate voltage can be analyzed by the graph portrayed in Fig. 18. Initially, the value of g_{m2} is increasing but after achieving a high peak it starts decreasing. This happens because after some point drain current saturates and its effect starts disappearing from g_{m2} and then gate voltage becomes a dominant factor and further increment in gate voltage makes g_{m2} decrease.

$$g_{m2} = \frac{\partial^2 I_d}{\partial V_{gs}^2} \tag{11}$$

$$g_{m3} = \frac{\partial^3 I_d}{\partial V_{gs}^3} \tag{12}$$

The third derivative of drain current is called g_{m3} and for better performance of the device in linearity analysis, its value should be small. g_{m3} can be calculated from the Eq. 12 and its variation with gate voltage has been shown in Fig. 19. For this device, g_{m3} increases a little initially then starts decreasing rapidly and achieves very low value, which helps the device to provide better linearity performance. 1st and 2nd harmonic voltages are equal at input gate voltage (V_{gs})

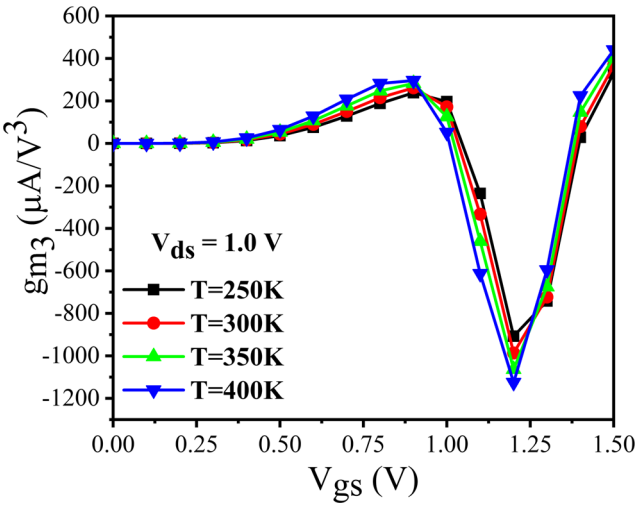

Fig. 19 g_{m3} variation with V_{gs} at various temperatures

which is represented by Voltage-Intercept-Point (VIP_2). According to the Eq. 13, VIP_2 should have a high peak for distortion-less device [28]. In Fig. 20, VIP_2 has been varied with respect to the gate voltage. From Fig. 18, a negative value is shown by the g_{m2} for V_{gs} ranging from 1.125 V to 1.50 V at 400K temperature that leads to a negative peak for VIP_2 at 400K temperature.

$$VIP_2 = 4\left(\frac{g_{m1}}{g_{m2}}\right) \tag{13}$$

Third-order Voltage Interception Point (VIP_3) is a gate voltage (V_{gs}) at which both 1st and 3rd harmonic voltages are equal [29]. This intercept point inversely depends upon g_{m3} which is shown in the Eq. 14. The relationship between VIP_3 and input gate voltage has been shown in Fig. 21 where VIP_3 achieves a high peak for the high temperature in the range from 0.875 V to 1.125 V due to rapid increase

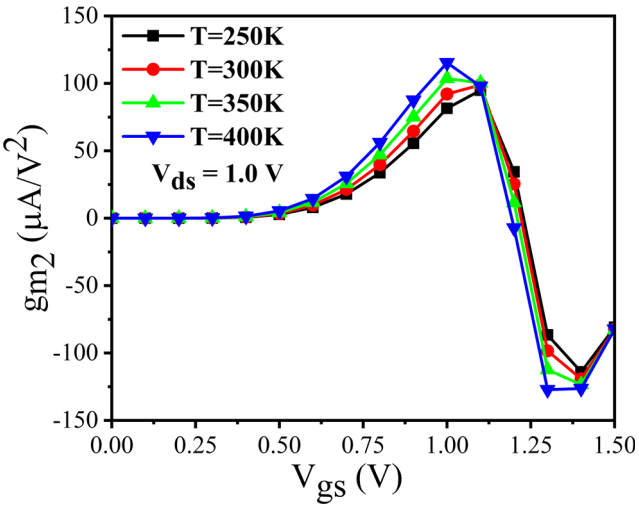

Fig. 18 g_{m2} variation with V_{gs} at various temperatures

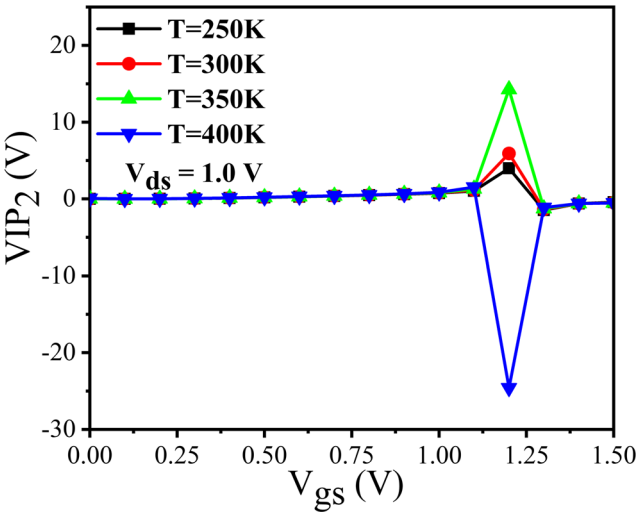

Fig. 20 VIP_2 variation with V_{gs} at various temperatures

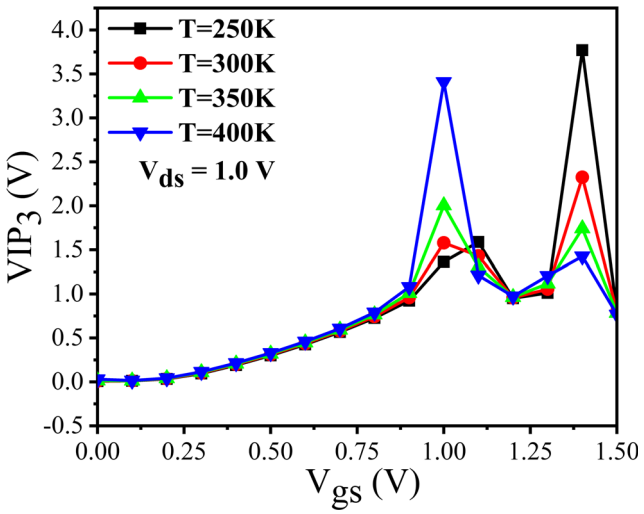

Fig. 21 VIP3 variation with V_{gs} at various temperatures

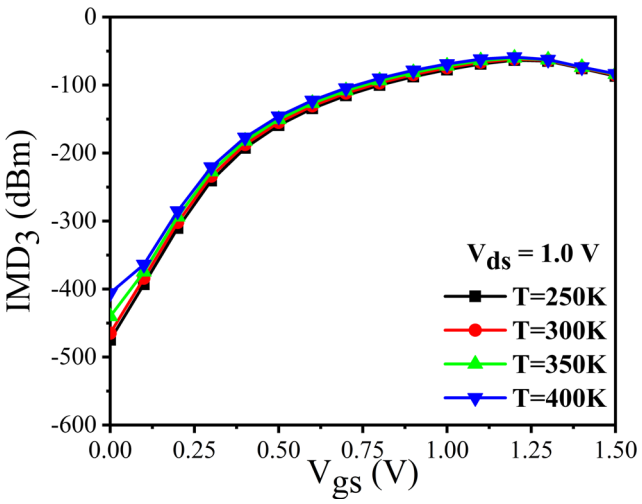

Fig. 23 IMD3 variation with V_{gs} at various temperatures

of g_{m1}, at this range of V_{gs}, g_{m3} shows very less impact on VIP_3. The second high peak is achieved by the VIP_3 for the low temperature in the range from 1.25 V to 1.50 V because here g_{m3} shows a low value for low temperature.

$$VIP_3 = \sqrt{24\left(\frac{g_{m1}}{g_{m3}}\right)} \tag{14}$$

Input power where first and second-order harmonic power are equal is examined by 3rd order Input- Intercept-Point (IIP_3) [30]. It is noticed that low value of g_{m3} decides better performance of the device. According to the Eq. 15, decreased g_{m3} improves IIP_3. IIP_3 (log) variation has been shown in the Fig. 22.

$$IIP_3 = \frac{2}{3}\left(\frac{g_{m1}}{g_{m3}R_s}\right) \tag{15}$$

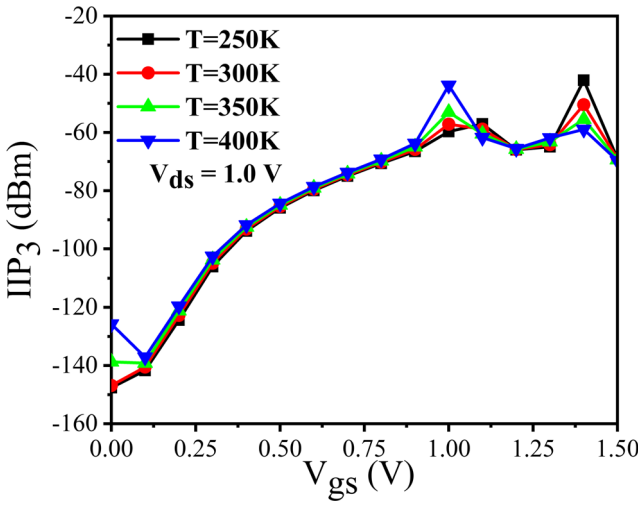

Fig. 22 IIP3 (log) variation with V_{gs} at various temperatures

IMD_3 occurs when two or more signals of different frequencies are mixed. Inter-modulation distortion is calculated by IMD_3 and its value should be as minimal as possible [31]. For smaller V_{gs}, IMD_3 is very low, and when V_{gs} starts increasing, IMD_3 also starts achieving high values. Temperature also affects the distortion parameter as we can see in Fig. 23. This parameter can be evaluated from the Eq. 16.

$$IMD_3 = \left[\frac{9}{2}(VIP_3)^2 g_{m3}\right]^2 R_s \tag{16}$$

The level of output power at which the gain reduces by 1 decibel from its constant value is known as the 1 decibel compression point (P1dB). When an amplifier reaches its point of 1 decibel compression, it enters into compression and transforms into a non-linear device,

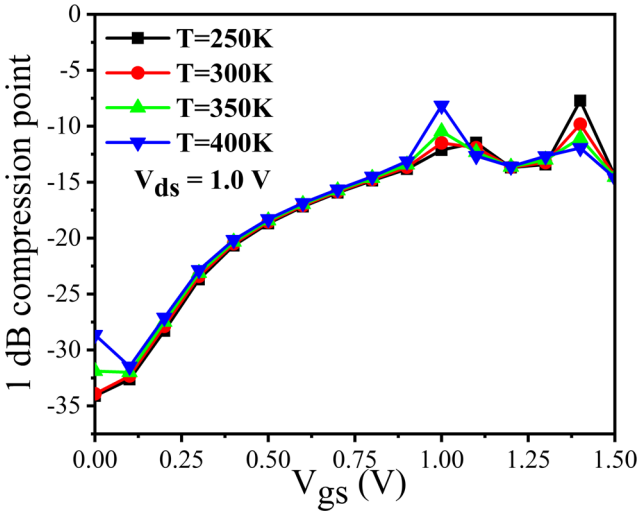

Fig. 24 Variation of 1 decibel Compression Point with V_{gs} at various temperatures

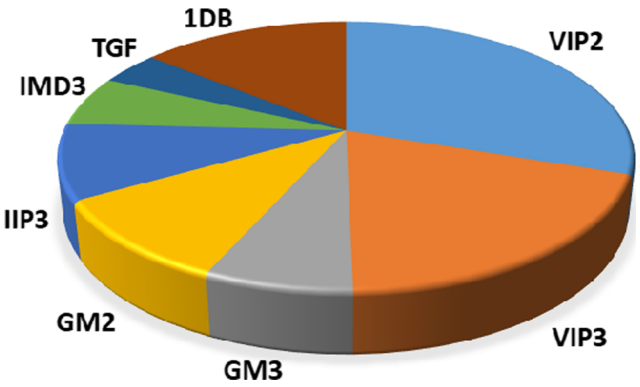

Fig. 25 Variation of 1 dB Compression Point with V_{gs} at various temperatures

resulting in harmonics, distortion, and inter-modulation products. It gives an indication of how much power the amplifier can store. 1 dB compression point is defined by the Eq. 17.

$$1dB\,compression\,point = 0.22\sqrt{\frac{g_{\mathrm{m1}}}{g_{\mathrm{m3}}}} \tag{17}$$

1 dB compression point value should be large enough, for more linearity of the device [32]. Log variation of 1 dB compression point is shown in Fig. 24 and conveys that high value is achieved when the value of g_{m3} is small.

3.5 Reliability of Device

Device reliability related issues are illustrated in this part of the research work for a temperature range of 250K to 400K. The study of ON-state current in this work shows that for a high temperature, drain current improves slightly but off current also degrades with a large value which impacts the I_{ON}–I_{OFF} ratio extremely. The reason behind this is that TAT and SRH provide a large dependency in OFF-state, however BTBT shows its dependency in ON-state mainly. Ambipolarity and SS start degrading with the temperature increment. The evaluation of DC, Analog, and Linearity parameters determines the satisfactory reliability performance of HGO-DW-SCTFET. The deviation in linearity parameters of HGO-DW-SCTFET for temperature fluctuation has been shown in Fig. 25.

4 Conclusion

A temperature based study has been done in this paper for DC, Analog characteristics, linearity analysis and reliability analysis of the device. From the study, it is concluded that our proposed device (HGO-DW-SCTFET) shows high sensitivity towards temperature. For 250K to 400K range of temperature, ON-state current increases but for high temperature, OFF current also increases, which reduces the quality of I_{ON}–I_{OFF} ratio. Along with this, OFF-state current for different temperatures at different models has been analyzed. The current in the OFF-state is increasing due to TAT and SRH modeling for high temperatures. We have also examined the behavior of the SS, V_{th} and I_{ON}–I_{OFF} ratio concerning temperature. Analog parameters are also highly sensitive to the temperature and provide better results at high temperature. Trans-conductance, f_T, GBP, TFP attains high peak for high temperature and TGF achieves the lowest peak for 400K. A device performs in a better way if transit time of the device shows the lowest value. For 400K, transit time of the device is very less in comparison to other devices. We have also examined linearity metrics in terms of g_{m2}, g_{m3}, VIP_2, VIP_3, IIP_3, and IMD_3, and 1 dB compression point to analyze non-linearity issues of the device. Along with these reliability issues also has been determined for the device. So according to the impactful study in this research work, it shows small distortion for small V_{gs} and better current driving capability of HGO-DW-SCTFET which portrays itself a reliable device in linearity analysis, DC analysis, Analog analysis and for high frequency applications.

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Author Contributions

- Manshi Kamal: Conceptualization, data curation, formal analysis, methodology, investigation, writing – original draft.
- Dharmendra Singh Yadav: Supervision, validation, visualization, writing – review & editing

Data Availability The data and material concerned to the manuscript may be made available on request.

Declarations

The manuscript follows all the ethical standards, including plagiarism.

Consent to participate Yes.

Consent for Publication Yes.

Conflict of Interests No conflicts of interest.

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