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ORIGINAL PAPER

Impactful Study of F-shaped Tunnel FET

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Abstract
In this proposed work, a novel single gate F-shaped channel tunnel field effect transistor (SG-FC-TFET) is proposed and investigated. The impact of thickness of the source region and lateral tunneling length between the gate oxide and edge of the source region on analog and radio frequency parameters are investigated with appropriate source and drain lateral length through the 2D-TCAD tool. The slender shape of the source enhanced the electric field crowding effect at the corners of the source region which reflect in terms of high ON-current (I_{on}). The I_{on} of the proposed device is increased up to $10^{-4}\ A/\mu m$ with reduced sub-threshold swing (SS) is 7.3 mV/decade and minimum turn-ON voltage (V_{on} = 0.28 V). The analog/RF parameters of SG-FC-TFET are optimized.

Keywords Band-to-Band tunneling (BTBT) · Tunnel field effect transistor (TFET) · Energy band diagram (EBD) · Source/channel interface (SCi) · Drain/channel interface (DCi) · Tunneling length · F-shaped channel

1 Introduction

The steeper subthreshold slope devices are necessary to alter next generation low power device application in the field of electronics. The TFET is one of the most extensively investigated novel devices with their methodologies that can potentially surpass the 60 mV/decade limit of SS in MOSFET at room temperature [1–3]. The TFET working operation is based on BTBT mechanisms, and it is capable of attaining a smaller SS value. However, the ambipolar behavior (high ambipolar current ($I_{amb} \approx 10^{-7}\ A/\mu m$)) and low I_{on} ($\approx 10^{-6}\ A/\mu m$) for which TFET can be realized by a small tunneling junction with limiting SCi region. To overcome these leading limitations of TFET, many researchers investigated different structures and materials by using antithetic concepts and techniques [4–9]. In this simulation-based work, a novel SG-FC-TFET has been studied and optimized to obtain high I_{on}, suppressed I_{amb}, and minimum V_{on} with the steeper sub threshold slope of $I_{ds} - V_{gs}$ curve. Along with this, the analog and radio frequency performance parameters were analyzed through the 2D-TCAD tool, to optimize the device performance for high frequency applications with low power consumption.

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2 Designed Device Specifications

The 2D cross-sectional view of conventional double gate TFET (DG-TFET) and the proposed device structure under study is illustrated in Fig. 1a and b. The proposed device resembles a finger-like ultra-thin N-type source region (dark green color) which is completely enclosed by a lightly doped P-type channel region. Due to complete insertion of source in channel region, the tunneling area is increased. Along with this, electric field crowding effect came into existence at the corner of source region. A metal gate (gate work function (WF_{gate})= 4.6 eV) with a SiO_2 as gate oxide is used to improve the controllability over channel region. Along with different colors displayed in Fig. 1b defining various regions of simulated device like oxide, source, gate, channel, drain electrodes and their region, etc. The simulated device and DG-TFET are with drain doping $N_{DN} = 1 \times 10^{18} cm^{-3}$ (N+ type), source doping $N_{SP} = 1 \times 10^{20} cm^{-3}$ (P+ type), channel doping $N_{CP} = 1 \times 10^{15} cm^{-3}$ (P-type) and SiO_2 (k= 3.9) as gate oxide material.

Figure 2 depicts flawless fabrication process steps for SG-FC-TFET with ultra-thin finger like source region. A single silicon bulk wafer is used initially and ip+i epitaxial

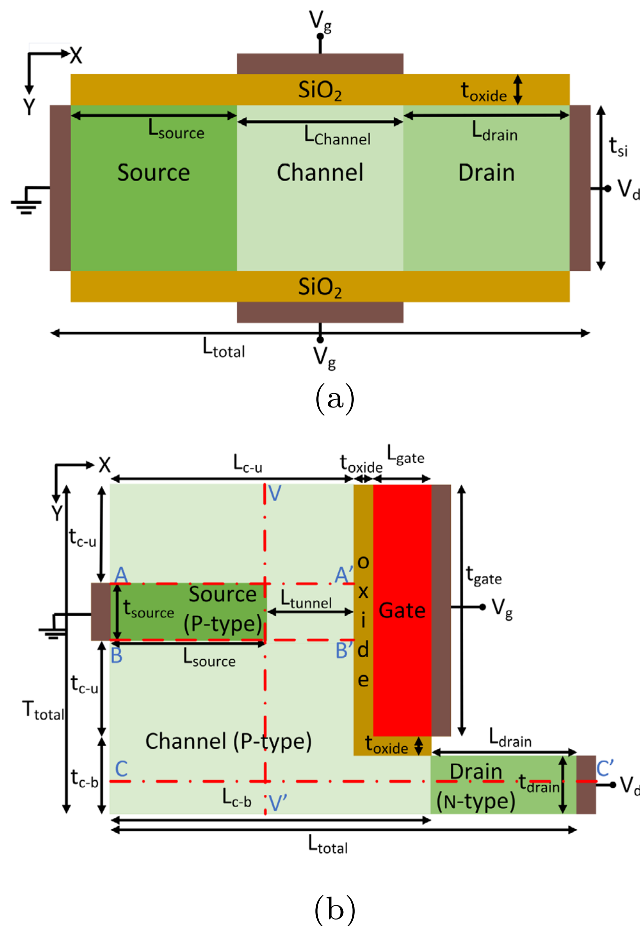


Fig. 1 2D cross sectional schematic of **(a)** DG-TFET: $L_{source} = 25nm, L_{channel} = 53nm, L_{drain} = 25nm, t_{si} = 10nm, t_{oxide} = 1nm\ and\ L_{total} = 103nm$ **(b)** SG-FC-TFET (Proposed device): $L_{drain} = 38nm, t_{drain} = 5nm, L_{gate} = 20nm, t_{gate} = (2t_{c-u} + T_{source}) = 35nm, t_{oxide} = 1nm, L_{c-u} = 44nm, L_{c-b} = 65nm, t_{c-b} = (t_{oxide} + t_{drain}) = 6nm, L_{source} = 40nm, t_{source} = 3nm, L_{tunnel} = 4nm, t_{c-u} = 16nm, T_{total} = 41nm\ and\ L_{total} = 103nm\ with\ SiO_2\ as\ gate\ oxide$

layers can be grow (active regions) with the help of in-situ doping process. After this, CVD (chemical vapor deposition) method is use to deposit SiO_2 hard-mask and this will cooperative to passivate active sidewall. SiO_2 sacrificial buffer layer deposited after performing mesa pattering process. Along with this, a dummy gate is formed and etch back process performed to remove the SiO_2 buffer layer. With the help of RTA (Rapid thermal annealing) and ion implantation process, arsenic impurity (VA group) is added to define the drain region and a thick layer of SiO_2 is deposited. To evince the dummy gate, CMP (chemical mechanical polishing) is used. For ultra-thin lateral tunnel region, selective epitaxial layer of silicon is grown after the selective removal of dummy gate and SiO_2 sacrificial buffer layer. After this, the stacking of gate and gate-oxide is performed by using atomic layer deposition processes. At the last, selective etch back process performed to obtain proposed device schematic [10–14].

3 Results and Observations

The DG-TFET and SG-FC-TFET are simulated in a 2D-TCAD simulator using nonlocal BTBT, SRH, FLDMOB, auger, FERMI, and CONMOB models. Along with, quantum tunneling region (qt region) for accurate lateral tunneling of electrons and holes at both interfaces (SCi and DCi). The comparative analysis between both devices is perform to ensure the performance advantages of proposed device over the conventional DG-TFET. From Fig. 3, the I_{amb} is suppressed by seven decade because the the BTBT rate is reduced as DCi decreases. However, I_{on} increased by 3 decade because of electric field crowding effect and increased tunneling area at SCi. The turn-ON voltage is reduced by 0.25V for the proposed device when compare to DG-TFET because very high charge accumulation takes place at the SCi junction and high ELF crowding effect helps to enable the BTBT phenomena earlier. Along with, the steepness of $I_{ds} - V_{gs}$ is improved and the SS value for proposed device is reduced (7.3 mV/decade).

The electric field (ELF) variation of proposed device along with different cut lines is illustrated in Fig. 4. The ELF plays an important role in the proposed device operations [15, 16], hence it can be analyzed in different regions by imposing cut lines. AA' (Black square) and BB' (Red circle) horizontal cut lines are used to compare ELF at the corners of source region where ELF crowding takes place. The ELF along cut lines AA' and BB', which run parallel to the upper and lower source junctions exhibit peak each at X ≈ 66 nm, which falls within the channel. Besides, the field is nearly uniform and rather small at the lateral source junction, shown in Fig. 4a. Next, The ELF at the CC' cut line, intersecting the drain junction, exhibits a first peak (≈ 4.5 × 10^5 V/cm) within the channel and second peak occurs at X ≈ 90 nm (≈ 1.5 × 10^5 V/cm) because the DCi junction at X = 91 nm, as depicted in Fig. 4b. For analysis of ELF crowding effect at corner and flat region of source, vertical VV' cut line used, it exhibits double peak at Y ≈ 15 nm and 20 nm, as portrayed in Fig. 4c. Therefore, we can conclude that at the corner of source region ELF is very high (E_{corner}=4 × 10^5 V/cm) compare to flat region (E_{flat}=2.3 × 10^5 V/cm). The high ELF at source corners (Fig. 4), causes higher drain current due to improved tunneling probability at SCi. From Fig. 5a, we can observe that the drain current (I_{ds}) increased rapidly w.r.t., V_{gs} at fixed V_{ds}= 0.7 V.

The slope of $I_{ds} - V_{gs}$ curve defines the amplification ability of the device, which is also known as g_m. The g_m of a device also depends on the I_{ds} [17, 18]. Hence, higher

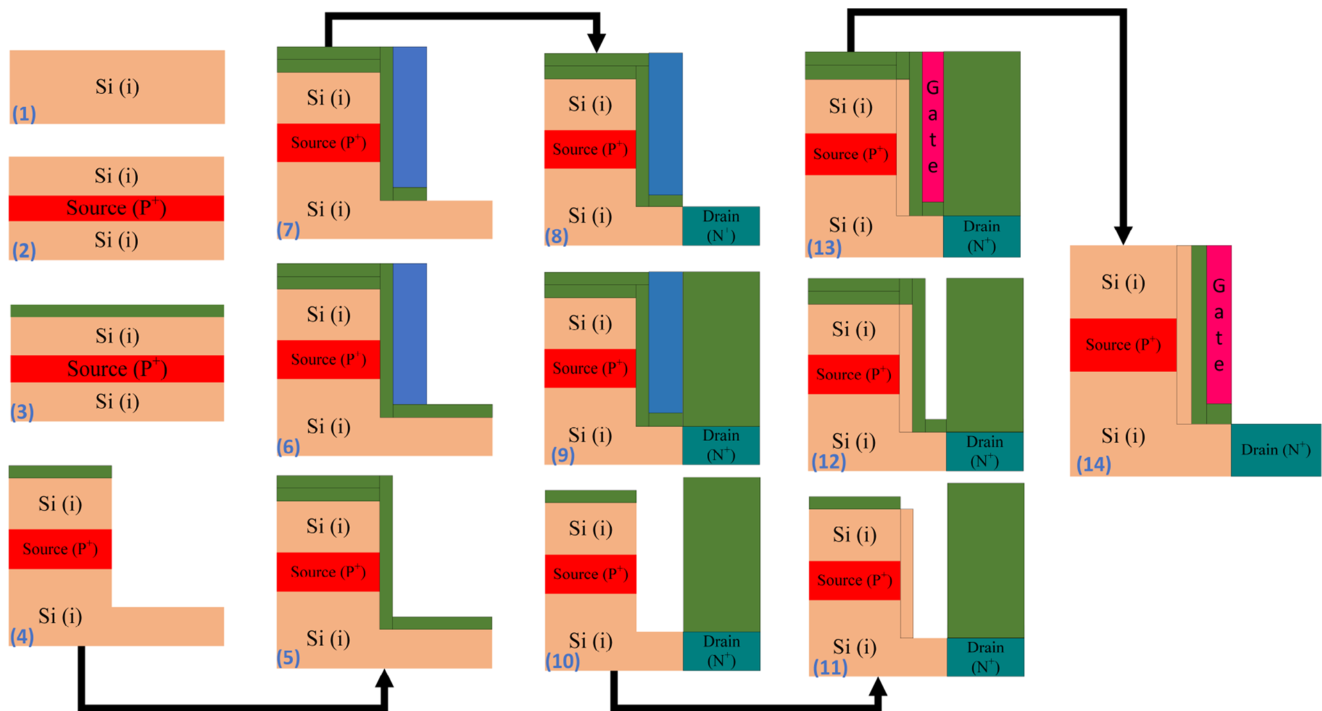


Fig. 2 Fabrication process flow of SG-FC-TFET device

I_{ds} reflect in terms of higher g_m in the range of 830 μS (Fig. 5b). On the other hand, g_{ds} of the device is required low for better device performance because output resistance (R_{out}) of device inversely proportional to g_{ds}. For better amplification property, we need a device with high R_{out} [19]. For the proposed device, the g_{ds} is obtained 23 μS, as displayed in Fig. 5c. The ratio of g_m to g_{ds} is known as intrinsic gain, it should be high for better amplification property of a device [20]. From Fig. 5d, the intrinsic gain of the proposed device is increasing with V_{gs} (up to 0.9 V) and

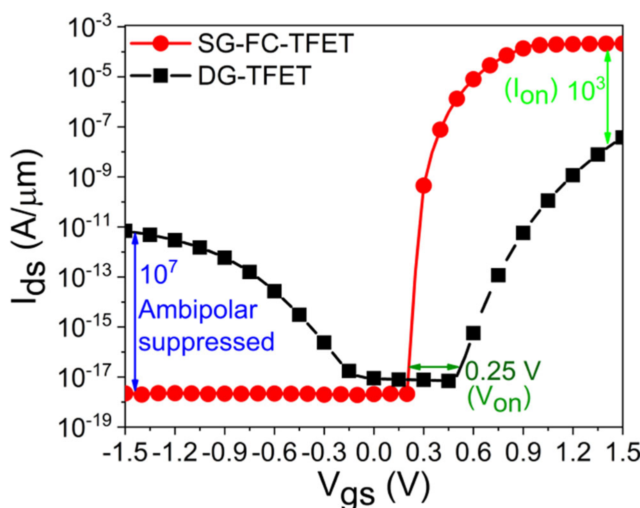
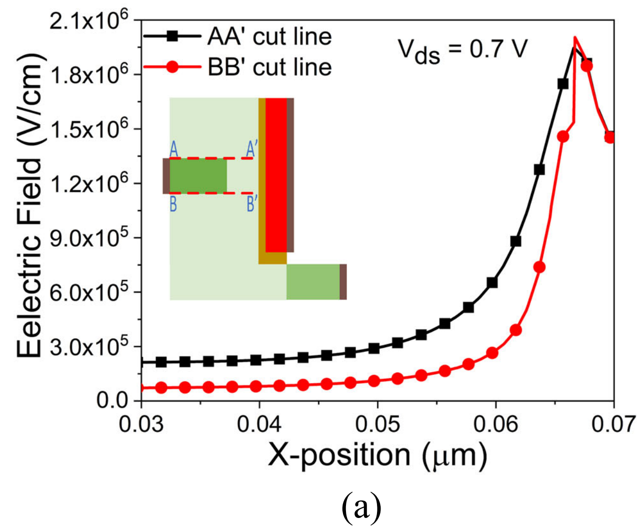


Fig. 3 Comparative Transfer characteristics of DG-TFET and SG-FC-TFET

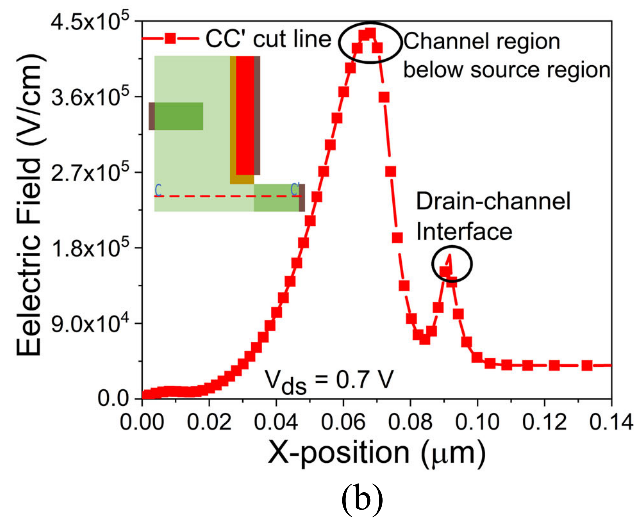
attain the peak value 68 obtained as an ratio. Furthermore, it starts decreasing due to mobility saturation of charge carriers a significant reduction been observed in g_m.

The radio frequency (RF) parameters play a very crucial role in the circuit level analysis of the device. Regarding this, the parasitic capacitances (C_{gd} and C_{gs}) are analyzed and depicted by Fig. 6a and b. The C_{gd} is a critical parameter that affects many other RF parameters (f_t, GBP, etc.) [19]. The lower value of capacitances are observed in this proposed device because of less accumulation of charge carriers at SCi and collected by drain region. The reduced value of C_{gd} helps to improve the gate controllability over the channel region with enhanced f_t and GBP values of proposed device [20], as illustrated in Fig. 6c and d. The f_t and GBP increased to achieve their apex, then with higher C_{gd} it starts decreasing.

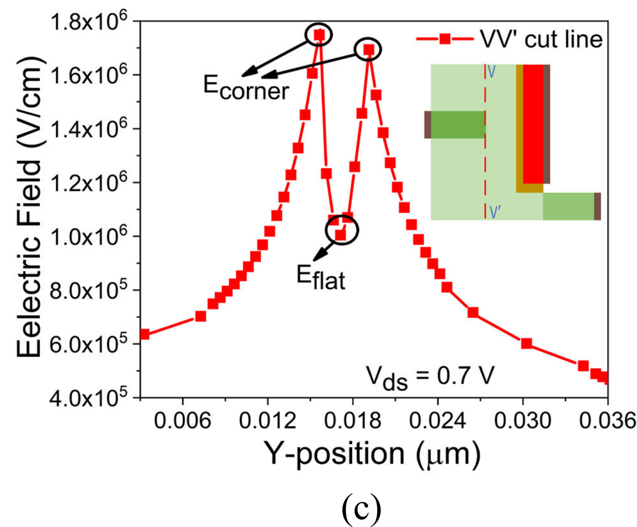
To explain the trade-off between intrinsic gain and cut-off frequency, another parameter is introduced named GFP. It is increasing with V_{gs} due to an increment in intrinsic gain and f_t (Fig. 7a). Its curves start decreasing due to mobility saturation of the charge carriers which are responsible for existence of parasitic capacitances. Along with, TFP and TGF are also examining to check the device efficiency and consumption of power. TFP defines the relation between power and bandwidth [20]. Therefore, a higher value of TFP = 0.31 GHz (Fig. 7b) indicates that the proposed device is suitable for low-power applications. On the other hand, TGF defines the device efficiency in terms of circuit operation. The higher value of TGF reflect in terms of high



(a)



(b)



(c)

Fig. 4 Schematic corresponds to Fig. 1b, Electric field strength analysis for (a) horizontal cut lines AA' and BB' (b) horizontal cut line CC' and (c) vertical cut lines VV'

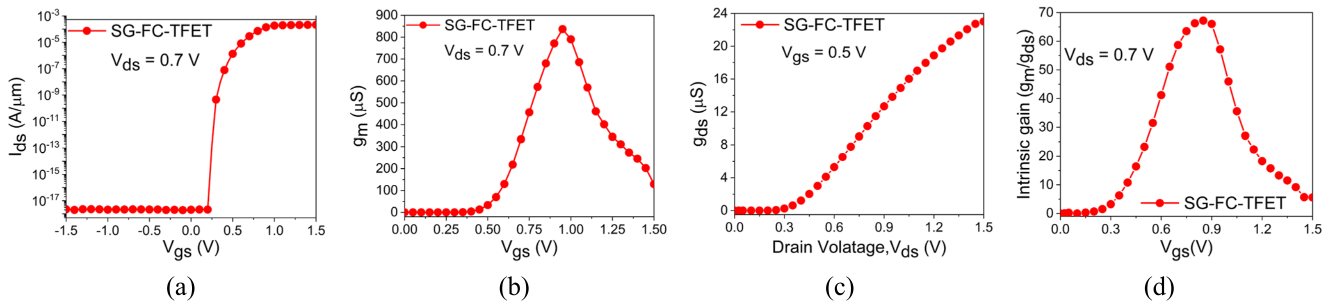


Fig. 5 **(a)** Transfer characteristics ($I_{ds} - V_{gs}$) **(b)** Transconductance (g_m) **(c)** Output Transconductance (g_{ds}) **(d)** Intrinsic gain

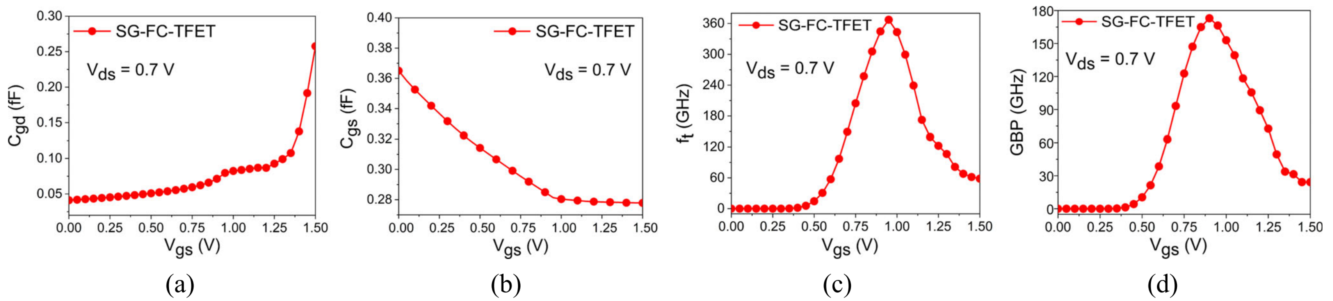


Fig. 6 **(a)** Gate to drain capacitance (C_{gd}) **(b)** Gate to source capacitance (C_{gs}) **(c)** Cut-off frequency (f_t) **(d)** Gain bandwidth product (GBP)

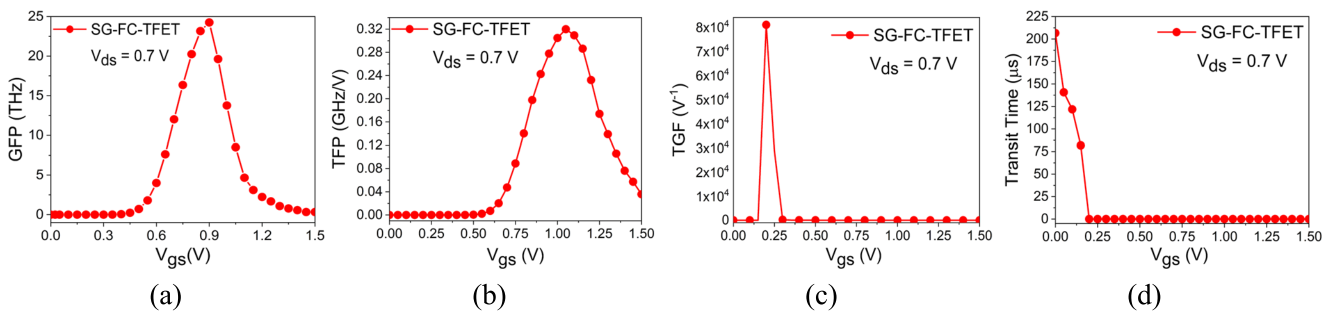


Fig. 7 **(a)** Gain frequency product (GFP) **(b)** Transconductance frequency product (TFP) **(c)** Transconductance generation factor (TGF) **(d)** Transit time

device efficiency [20]. From Fig. 7c, we can observe that TGF of $8 \times 10^4\ V^{-1}$ is achieved for the proposed device (SG-FC-TFET).

The transit time (τ) is inversely propositional to f_t. For higher f_t, transit time is less [10]. In other words, τ represents the delay of a device, so the speed of SG-FC-TFET is improved with a reduced value of τ. From Fig. 7d, we can analyze that τ is in the range of 210.5 μs, which indicates that the proposed device can be used in digital circuits with the advancement of high speed as well as low power consumption [21]. According to the above impactful studies carried out, the proposed device (SG-FC-TFET) is best suited for low power high speed with enhanced RF performance.

4 Conclusion

In this study, we have inspected the solitary characteristics of SG-FC-TFET with fabrication process flow. It is worth pointing of the effect of a finger-like shape of the source region on analog/RF parameters is investigated using a 2D-TCAD simulator in this analysis. The proposed device achieved $I_{on} = 4.35 \times 10^{-4}\ A/\mu m$, $I_{ambi} = 6.35 \times 10^{-18}\ A/\mu m$, $I_{on}/I_{off} = 6.85 \times 10^{13}$, $V_{on} = 0.28$ V and SS of 7.3 mV/decade. Along with these results, some important parameters were also examined to study the RF performance of the SG-FC-TFET device like g_m (830 μS), g_{ds} of (23 μS), C_{gd} of 0.23 fF, C_{gs} of 0.28 fF, f_t = 370 GHz, GBP = 176 GHz, and GFP of 24 THz. To achieve high performance, some additional parameters related to the speed and power of the device are also investigated that as TFP (0.31 GHz), TGF ($8 \times 10^4\ V^{-1}$), and transit time (210.5 μs). The promising results obtained for the proposed design demonstrate its applicability in both analog and digital technologies.

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Author Contributions

- Prabhat Singh: Conceptualization, data curation, formal analysis, methodology, investigation, writing – original draft.
- Dharmendra Singh Yadav: Supervision, validation, visualization, writing – review & editing

Availability of Data and Material All relevant data has been included in manuscript.

Declarations

The manuscript follows all the ethical standards, including plagiarism.

Consent to Participate We are giving consent to participate.

Consent for Publication We are giving consent to publish.

Conflict of Interests No conflicts of interest

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