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ORIGINAL PAPER

Investigation of the Device Electrical Parameters for Homo and Hetero Junction Based TFETs

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Abstract
This paper presents the analytical approximation of device physics of heterojunction based double gate (DG) Tunnel field effect transistors (TFETs) in terms of potential distribution, electron density and electron barrier tunneling. In order to improve the device performance with respect to ON current (I_{ON}), DG TFET with gate-drain overlap is developed. An asymmetric gate oxide is introduced in the gate - drain overlap region and is compared to DG TFET. The device physics and its performance characteristics are studied by using various materials, such as Si, SiGe, InAs and GaSb. The simulated results are validated against the model values. DG TFETs with gate-drain overlap offers higher tunneling probability compared to DG TFETs. Also GaSb/Si based DG TFETs with gate-drain overlap shows good performance improvement by offering higher tunneling probability which in turn offers a higher I_{ON} of 1.15 mA/μm.

Keywords DG TFETs · Asymmetric gate oxide · Gate-drain overlap · Electron density · Band to band tunneling

1 Introduction

With the downscaling of CMOS devices, the high static power consumption has paved a way for an imminent power crisis. Small swing switches are an attractive applicant to replace the current MOSFETs for low power applications [1–5]. TFETs being an alternate to CMOS devices have become increasingly important in micro and nano-electronic applications due to their significantly low OFF current (I_{OFF}) and low subthreshold swing (SS) [6–8]. While the TFET devices reported early suffered from low ON current (I_{ON}), it has been reported that the use of the lower band gap materials have improved the same. The use of various materials such as Silicon, Ge, SiGe and group III-V materials have made it better suited for analog applications.

Many literature have been reported on TFET from analytical perspective. In certain 1D analytical models, the tunneling current has been analytically derived [9]. It has also been reported that, analytical based pseudo 2D approaches were designed from the aspect of examining the electrostatic potential and tunneling current of a long channel device [10]. The effect of shortest tunneling path were studied to analyze the behavior of device tunneling current [11]. An analytical model including the effect of the channel mobile charge carriers was studied to analyze the impact of the interface trapped charges density, the length of damaged region on the surface potential, and drain current on the device performance of DG TFET [12].

A 2-D analytical model of triple-metal hetero-dielectric DG TFET was reported by combining the concepts of triple material gate engineering and hetero-dielectric engineering along with silicon-on- nothing technology to improve the device performances [13]. An analytical drain current model for the dual-material-gate heterojunction (DMG-H) TFET was studied to observe the effects of source depletion, drain depletion, ambipolar behavior, and mobile charge performance both in inversion and accumulation states [14]. It has also been reported that by exploiting the thermal injection method (TIM), an accurate analytical model for the TFET potential profile can be developed to improve the device accuracy with less computational cost [15].

This study focuses primarily on improving DG TFET performance with device structure modification. An asymmetrical gate

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oxide is developed in the gate - drain overlap region and its performance is compared to that of DG TFET by exploring the device parameters (electrostatic potential, electron density and electron barrier tunneling). The devices taken into consideration are homo (Silicon based TFETs) and hetero-structures (SiGe/Si, InAs/Si and GaSb/Si) based TFETs. Device description and parameter space are given in the next section. The analytical expressions, validation of simulation result and conclusion are provided in the subsequent sections.

2 Device Description and Parameter Space

2.1 Device Description

All the simulations are carried out using technology computer aided design (TCAD) simulator from Synopsys [16]. The simulated structure of Si and SiGe/Si based DG TFET and DG TFET with gate-drain overlap are shown in Fig. 1(a-d) respectively. For SiGe/Si based devices, optimized mole fraction (x) of 0.4 is used. Figure 2(a-d) shows the device structure of InAs/Si and GaSb/Si based DG TFET and DG TFET with gate-drain overlap respectively. This study is carried out for drain voltage (V_d) of 1 V and gate voltage (V_g) of 1.8 V. All the devices are calibrated against the published results [8].

2.2 Parameter Space

Table 1 lists the dimensions of the device carried out in this study. Doping dependence mobility, high and normal field effects on mobility and velocity saturation are used in the physics section of the simulator. Besides, the Fermi - Dirac statistics and SRH recombination, Hurkx tunneling model is also used in the simulator.

2.3 Band Diagram of DG TFETs

Figure 3(a-d) depicts the band diagram of Si, SiGe/Si, InAs/Si and GaSb/Si based DG TFETs during ON state. A lower bandgap material can increase the tunneling probability in TFET which in turn improves I_{ON} of the device. When a smaller bandgap in the entire TFET region is used, both I_{ON} and I_{OFF} increases simultaneously. The material property at the source tunneling junction determines I_{ON} value of the device.

Various methods were used to establish a heterojunction in the device through the use of the smaller band gap material in the tunnel region and higher band gap material in the other regions of the device. It is evident from Fig. 3 that a reduced tunneling width of DG TFETs with gate-drain overlap offers higher tunneling probability which in turn results in higher I_{ON}. Also GaSb/Si based DG TFETs provides higher I_{ON}

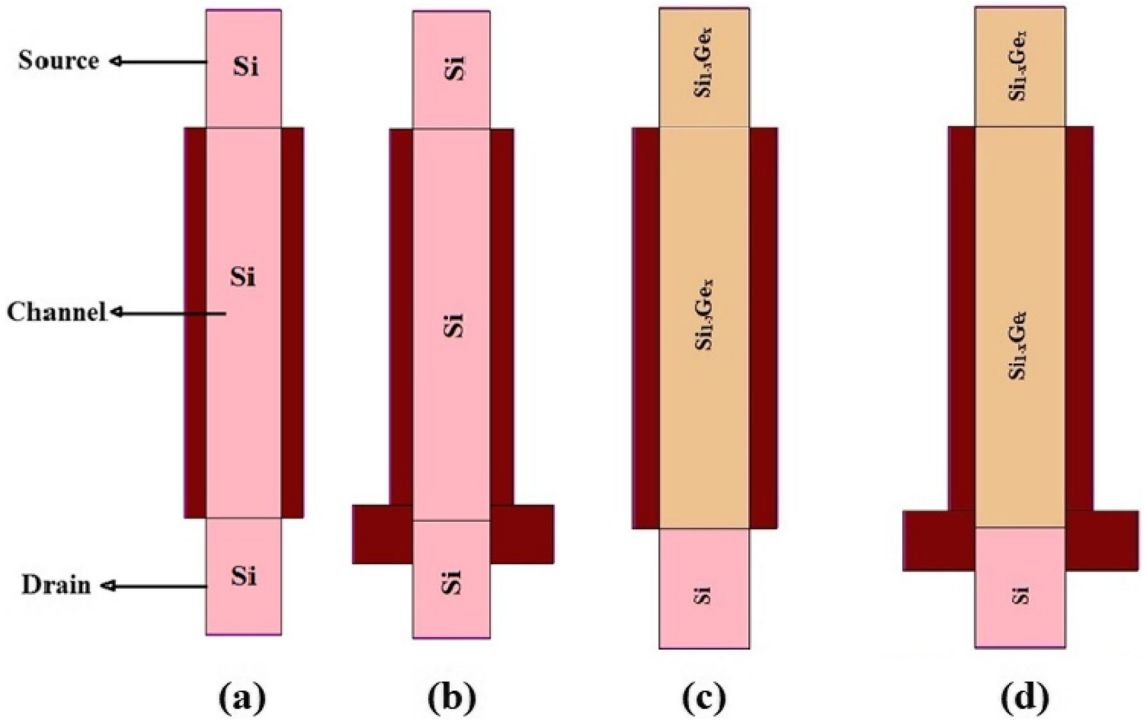

Fig. 1 Device structure of (**a**) Si based DG TFET (**b**) Si based DG TFET with gate-drain overlap (**c**) SiGe/Si based DG TFET (**d**) SiGe/Si based DG TFET with gate-drain overlap

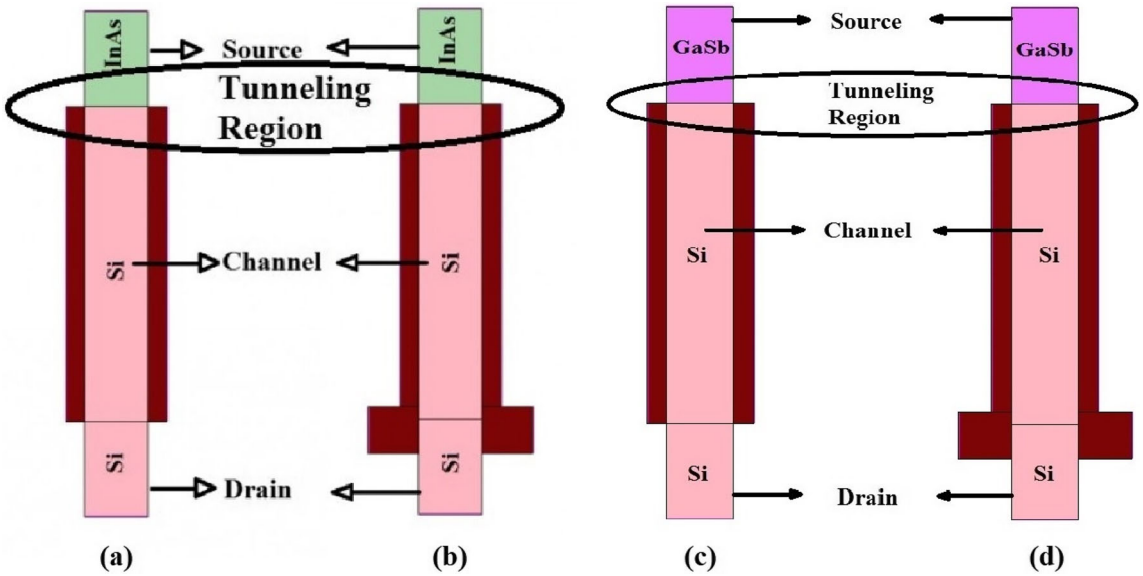

Fig. 2 Device structure of (**a**) InAs/Si based DG TFET (**b**) InAs/Si based DG TFET with gate-drain overlap (**c**) GaSb/Si based DG TFET (**d**) GaSb/Si based DG TFET with gate-drain overlap

compared with other devices due to higher tunneling rate of electrons at the source channel junction. Though InAs has a lower band gap, the material property of GaSb like electron affinity plays an important role in obtaining the higher tunneling rate of electrons at the source channel junction which in turn enhances the tunneling propability of the device [17].

Table 2 shows the I_{ON} value extracted for all the devices with I_{OFF} matching which can be done by proper gate work function tuning. It can be seen from Table 2 that, all DG TFETs with gate-drain overlap devices offers higher I_{ON} compared to DG TFETs without overlap. In addition, GaSb/Si based devices offers more I_{ON} compared to other materials and this is because of its material property, electron affinity [17].

Table 1 Parameter space for DG TFETs

Parameters	Si and SiGe/Si based DG TFETs	InAs/Si and GaSb/Si based DG TFETs
Gate length (L_g)	50 nm	50 nm
Gate oxide thickness (t_{ox})	3 nm	3 nm
Channel thickness (t_{ch})	10 nm	10 nm
Channel doping concentration (N_{ch})	1e17 cm^{-3}	1e16 cm^{-3}
Drain doping concentration (N_d)	5e18 cm^{-3}	1e19 cm^{-3}
Source doping concentration (N_s)	1e20 cm^{-3}	2e19 cm^{-3}

3 Analytical Expressions

In this section, the analytical expressions to obtain the electrical parameters, electrostatic potential, electron density and electron barrier tunneling are discussed as in the literature.

3.1 Potential Distribution

Potential distribution in the channel is obtained by solving the 2D Poisson equation,

$$\frac{\partial^2\Psi(x,y)}{\partial x^2}+\frac{\partial^2\Psi(x,y)}{\partial y^2}=\frac{qN_{ch}}{\varepsilon_s},(0\le x\le l_d) \tag{1}$$

where $\Psi(x,y)$ is the potential distribution, q is the charge and ε_s is the permittivity of semiconductor. The channel region can be split into two regions such as tunneling and transport regions. Figure 4 shows the electrostatic potential of a heterojunction DG TFET where l_d represents the length of the tunneling region and Ψ_{ch} represents the channel potential [18].

The parabolic approximation and vertical boundary conditions to solve 1D second order differential equation of Eq. (1) are as follows:

$$\begin{cases}\Psi(x,y)=a_0(x)+a_1(x)y+a_2(x)y^2\\ \Psi(x,0)=\Psi(x,t_{ch})=\Psi(x)\\ \varepsilon_s E_y(x,0)=C_{ox}\left(V_g-V_{fb}-\Psi(x)\right)\\ \varepsilon_s E_y(x,t_{ch})=-C_{ox}\left(V_g-V_{fb}-\Psi(x)\right)\end{cases} \tag{2}$$

From the above boundary conditions, 1D second order differential equation can be given as,

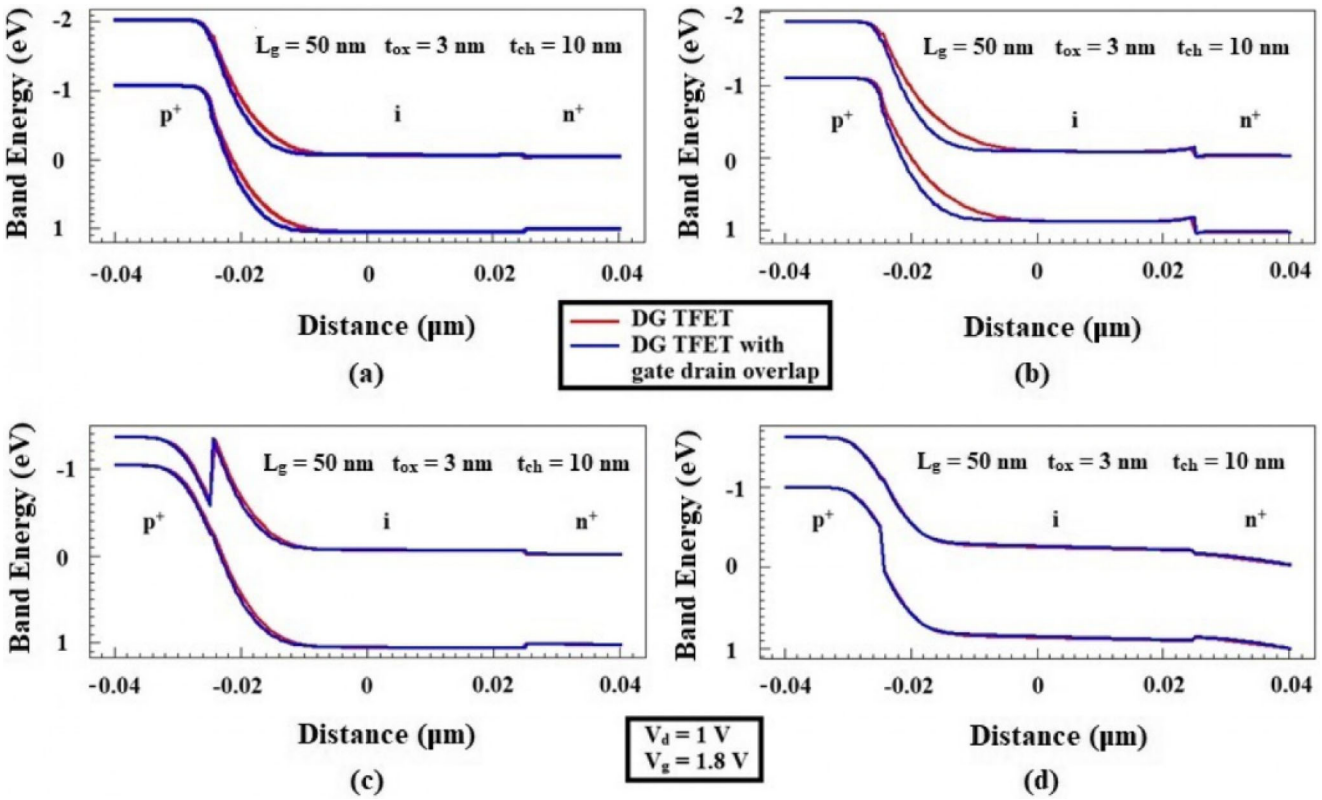

Fig. 3 Band diagram of Si, SiGe/Si, InAs/Si and GaSb/Si based DG TFETs during ON state

$$\frac{d^2\Psi(x,y)}{dx^2}-\frac{2C_{ox}}{t_{ch}\varepsilon_s}\Psi(x)=\frac{qN_{ch}}{\varepsilon_s}-\frac{2C_{ox}}{t_{ch}\varepsilon_s}\left(V_g-V_{fb}\right) \tag{3}$$

where $\Psi(x)$ is the electrostatic potential, V_{fb} is the flat band voltage which mainly depends on the material properties such as electron affinity, bandgap and intrinsic carrier concentration. C_{ox} is the effective oxide capacitance and can be given as ε_{ox}/t_{ox}, where ε_{ox} is oxide permittivity.

The general solution of the electrostatic potential can be obtained as below,

$$\Psi(x)=A\exp\left(\frac{x-l_d}{\lambda}\right)+B\exp\left(-\frac{x-l_d}{\lambda}\right)+\left(V_g-V_{fb}\right)-\frac{qN_{ch}}{\varepsilon_s}\lambda^2 \tag{4}$$

where λ is the characteristic length and it can be expressed as,

$$\lambda=\sqrt{\frac{t_{ch}\varepsilon_S}{2C_{OX}}} \tag{5}$$

A, B and l_d are the coefficients that can be obtained from below three boundary conditions. The electrostatic potential equals built in potential (V_{bi}) at the source/channel interface.

$$\Psi(0)=V_{bi} \tag{6}$$

The electric field equals zero at $x=l_d$,

$$\frac{d\Psi(x)}{dx}=0 \tag{7}$$

The electrostatic potential equals the channel potential at $x=l_d$,

$$\Psi(l_d)=\Psi_{ch} \tag{8}$$

Table 2 Comparison of DG TFETs with and without gate-drain overlap

Parameters	DG TFETs with gate-drain overlap				DG TFETs without gate-drain overlap			
	Si	SiGe/Si	InAs/Si	GaSb/Si	Si	SiGe/Si	InAs/Si	GaSb/Si
I_{ON} (μA/μm)	57	116	80	1150	15	15	45	900
I_{OFF} (fA/μm)	14.5	14.5	0.5	0.5	14.5	14.5	0.5	0.5

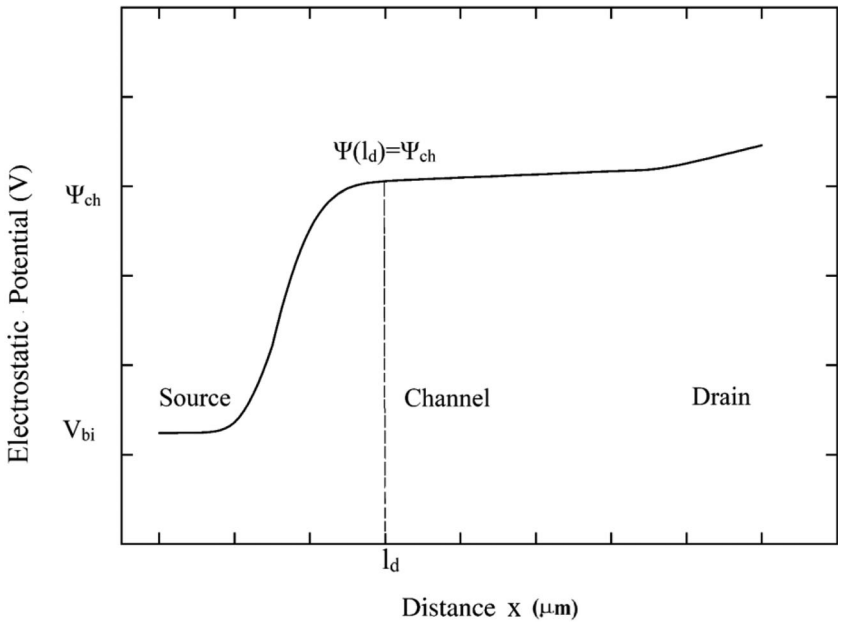

Fig. 4 Electrostatic Potential of a heterojunction DG TFET

The channel potential can be obtained from the solution of 1D Poisson's equation involving the inversion charge,

$$\frac{d^2\Psi(y)}{dy^2} = \frac{q}{\varepsilon_s\left(n_i e^{(\Psi(y)-V_d)/V_t}\right)}, \tag{9}$$

where n_i is the intrinsic carrier concentration, V_t is the thermal voltage,

$$\Psi_{ch} = \Psi(y)|_{y=t_{ch}} = V_d - \frac{2kT}{q}\ln\left[\frac{t_{ch}}{2\beta}\sqrt{\frac{q^2 n_i}{2\varepsilon_s kT}}\cos\beta\right] \tag{10}$$

where β can be obtained from the below expression,

$$\frac{q\left(V_g - V_{fb} - V_d\right)}{2kT} - \ln\left[\frac{2}{t_{ch}}\sqrt{\frac{2\varepsilon_s kT}{q^2 n_i}}\right] = \ln\beta - \ln(\cos\beta) + \frac{2\varepsilon_s}{t_{ch}C_{ox}}\beta\tan\beta \tag{11}$$

The coefficients A, B and l_d can be obtained from Eqs. (6)–(8),

$$A = B = \frac{\Psi_{ch} - \left(V_g - V_{fb}\right) + \frac{qN_{ch}}{\varepsilon_s}\lambda^2}{2} \tag{12}$$

$$l_d = \lambda\cosh^{-1}\left(\frac{V_{bi} - V_g + V_{fb} + \frac{qN_{ch}}{\varepsilon_s}\lambda^2}{\Psi_{ch} - V_g + V_{fb} + \frac{qN_{ch}}{\varepsilon_s}\lambda^2}\right) \tag{13}$$

After substituting A, B and l_d in Eq. (4), the electrostatic potential can be given as,

$$\Psi(x) = \left(\Psi_{ch} - V_g + V_{fb} + \frac{qN_{ch}}{\varepsilon_s}\lambda^2\right)\cosh\left(\frac{x - l_d}{\lambda}\right) + V_g - V_{fb} - \frac{qN_{ch}}{\varepsilon_s}\lambda^2 . (0 \le x \le l_d) \tag{14}$$

3.2 Electron Density Profile

Fermi-Dirac statistics and 2D density of states are used to obtain the density of electrons for weak and strong inversions.

$$n = \frac{g m_d kT}{\pi\hbar^2}\ln\left[1 + \exp\left\{\frac{q\Psi(x) + kT\ln\left(\frac{N_V}{N_A} - E_g - E_0(\Psi(x))\right)}{kT}\right\}\right] \tag{15}$$

where g is the degeneration factor, m_d is the density of states effective mass, N_V is the effective density of states in the valence band, $\hbar$ is the planks constant, Ψ(x) is the electrostatic potential and E_g is the band gap of the material.

The density of electrons for weak inversion obtained using Fermi-Dirac statistics can be expressed as follows [19].

$$n_w = \frac{g m_d kT}{\pi\hbar^2}\ln\left[1 + \exp\left\{\frac{q\Psi(x) + kT\ln\left(\frac{N_V}{N_A}\right) - E_g - E_{0\omega}(\Psi(x))}{kT}\right\}\right] \tag{16}$$

where $E_{0\omega}$ is the first subband energy level expression.

The electron density in the strong inversion (n_s) can be given as:

$$n_s = \frac{C_{ox,eff}\left(V_g - V_{th}\right)}{q} \tag{17}$$

where, $C_{ox,eff}(V_g)$ can be given as below,

$$C_{ox,eff}\left(V_g\right) = \frac{\varepsilon_{ox}}{t_{ox} + \frac{\varepsilon_{ox}}{\varepsilon_s} \times \frac{3}{b(n_s, \Psi_{st})}} \tag{18}$$

Parameter b and Ψ_{st}, the potential at the onset of inversion can be expressed as:

$$b = (n,\ \Psi(x))$$

$$= \left[\frac{12}{\varepsilon_s \hbar^2} m q^2 \left(\frac{n\Psi(x)}{3} + N_A x_{max} \Psi(x)\right)\right]^{1/3} \tag{19}$$

where $m = 0.98\ m_0$ is the longitudinal effective mass. x_{max} is the maximum position of x.

$$\Psi_{st} = 2\Psi_f + \frac{E_{0\omega}(2\Psi_f)}{q} \tag{20}$$

where, $2\Psi_f$ is the classical value of potential at the onset of inversion.

3.3 Tunneling Phenomenon

Band to band tunneling is a phenomenon in which a particle can escape a potential barrier even when it has insufficient energy to overcome the barrier. If the electric field in the semiconductor is significantly large, there is a finite probability that the electrons can tunnel or excite directly from the valence band to the conduction band [20]. Figure 5 shows the triangular potential barrier approximation in TFET.

An expression of the tunneling probability in TFETs determined by using the WKB approximation can be given by

$$T_t \approx \exp\left[-2\int_{-x_1}^{x_2} |k(x)| dx\right] \tag{21}$$

where $-x_1$ and x_2 are the coordinates at which the triangular barrier is drawn, k(*x*) is the electron's wave vector in the triangular barrier and it can be expressed as,

$$k(x) = \sqrt{\frac{2m^*}{\hbar^2}(PE - E)} \tag{22}$$

where m^* is the effective carrier mass (material dependent), PE is the potential energy and E is the energy of the incoming electron. The energy of the electron at the widest part of the triangle is zero (E = 0) and as per equation of triangle, PE can be substituted by $\left(\frac{E_g}{2} - q\xi x\right)$, where ξ is the electric field at the tunnel junction. Then k(x) can be rewritten as,

$$k(x) = \sqrt{\frac{2m^*}{\hbar^2}\left(\frac{E_g}{2} - q\xi x\right)} \tag{23}$$

Substituting Eq. (23) in Eq. (21),

$$T_t \approx \exp\left[-2\int_{-x_1}^{x_2} \sqrt{\frac{2m^*}{\hbar^2}\left(\frac{E_g}{2} - q\xi x\right)}\right] dx \tag{24}$$

After integration, T_t is obtained as,

$$T_t \approx \left[\exp\left[\frac{4}{3}\frac{\sqrt{2m^*}}{q\xi\hbar}\left(\frac{E_g}{2} - q\xi x\right)\right]^{3/2}\right]_{-x_1}^{x_2} \tag{25}$$

From Fig. 5, at $x = x_2$, $\left(\frac{E_g}{2} - q\xi x\right) = 0$ and at $x = -x_1$, $\left(\frac{E_g}{2} - q\xi x\right) = E_g$, substituting this in Eq. (21) yields T_t as below,

$$T_t \approx \exp\left(-\frac{4\sqrt{2m^*}E_g^{3/2}}{3q\hbar\xi}\right) \tag{26}$$

From Eq. (26) it can be observed that a particle with lower mass, with lower bandgap and higher electric fields will yield higher tunneling probability which in turn offers higher I_{ON}.

4 Validation of Results

The simulated plots of the three electrical parameters, electron density, electron barrier tunneling and electrostatic potential could be validated with their corresponding analytical expressions as discussed in the previous section. The various parameters are extracted and fitted into the appropriate expressions using MATLAB version 9.6. All the input parameters of the device (material parameter, geometrical parameter, doping, etc) are given into the MATLAB and the values of the output electrical parameters are obtained along with the corresponding plot.

4.1 Electrostatic Potential Distribution

The predicted electrostatic potential profile simulated from TCAD along with the model values extracted from MATLAB for all the devices are shown in Fig. 6. It can be

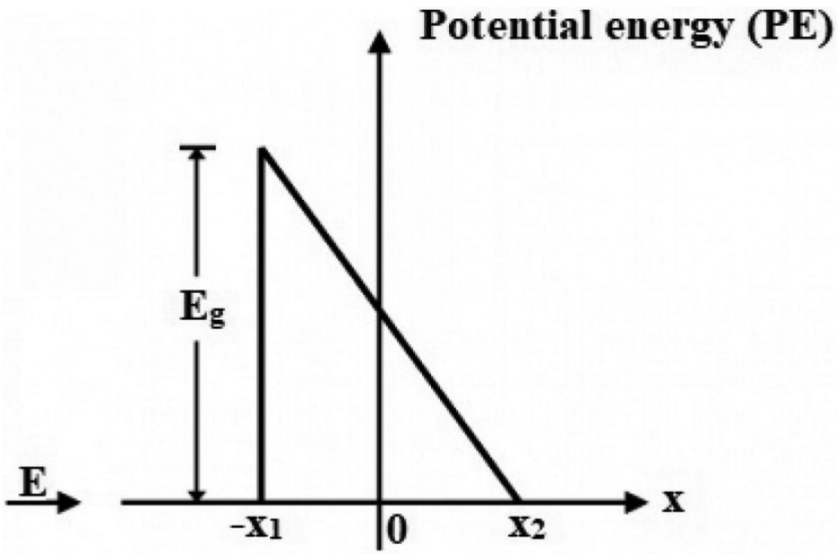

Fig. 5 Triangular potential barrier approximation in TFETs

found from the plot that the model value shows good agreement with the TCAD simulated values. From the plot it can be observed that the electrostatic potential at the source end is high for the device with gate-drain overlap as compared to the device without overlap and this can be attributed due to the injection of carriers at a higher velocity from the source side. It can also be seen from the plot that electrostatic potential is high for DG TFETs with gate-drain overlap in comparison with the DG TFETs without overlap. Due to this, high tunneling current is obtained for DG TFETs with gate-drain overlap.

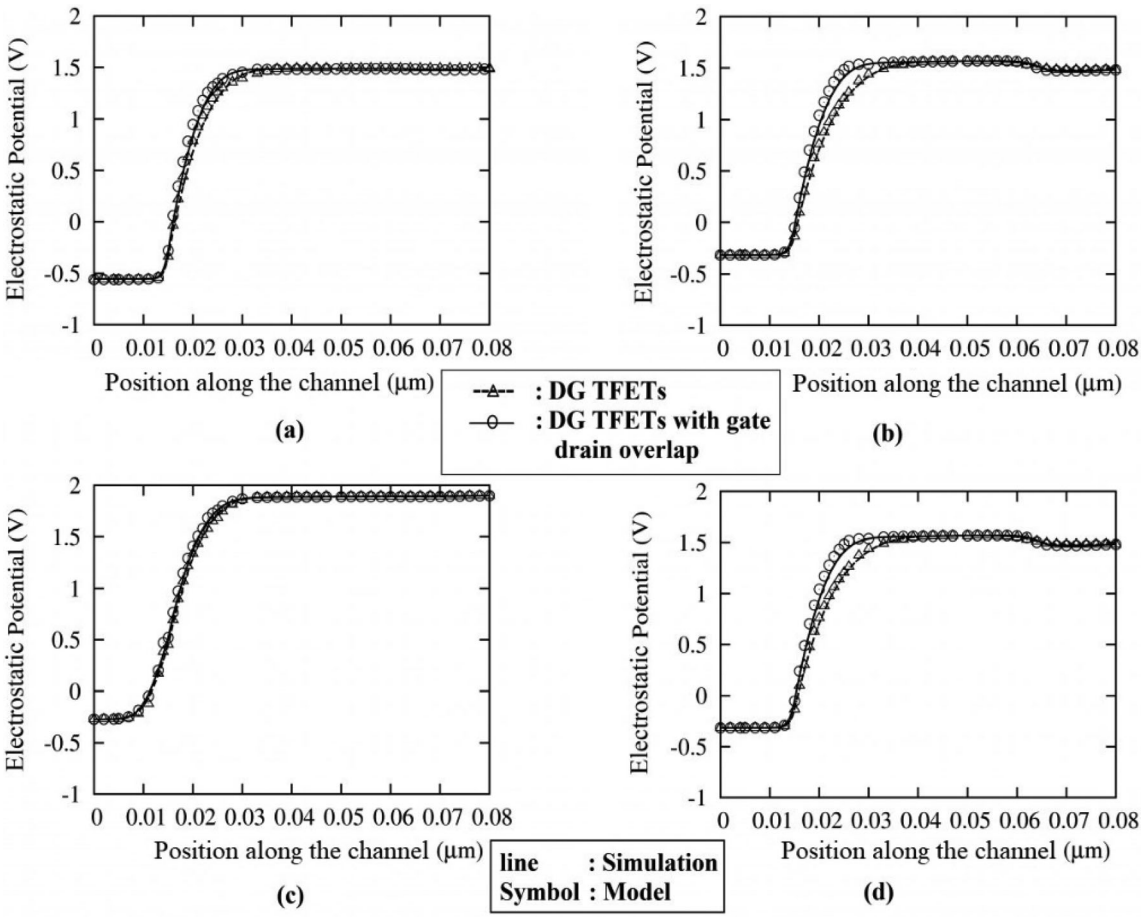

Fig. 6 Electrostatic Potential of (**a**) Si based DG TFETs (**b**) SiGe/Si based DG TFETs (**c**) InAs/Si based DG TFETs and (**d**) GaSb/Si based DG TFETs

4.2 Electron Density Profile

Figure 7(a-d) shows the electron density profile simulated from TCAD along with the model values extracted for all the devices. It can also be observed from the plot that GaSb/Si-based DG TFETs offers enhanced electron density compared with other devices. This can be attributed due to the volume inversion taking place in the channel. The volume inversion in the channel improves the I_{ON}. Also, the electron density at the source end has improved for the devices with gate-drain overlap comparing to devices without overlap and thereby resulting in higher I_{ON} [21].

4.3 Electron Barrier Tunneling

Figure 8 shows the TCAD simulated electron barrier tunneling distribution along with the extracted model values for all the devices. From the plot, the rate at which the electrons are generated at the source side due to tunneling can be obtained. From Fig. 8 it can also be seen that DG TFET with gate-drain overlap has more electron tunneling probability compared to that of DG TFET. It is also evident from the plot that GaSb/Si based DG TFET devices offers higher tunneling rate compared to other materials. Since GaSb/Si based DG TFETs offers higher tunneling rate of electrons, increased I_{ON} is obtained for the same compared to other devices.

5 Conclusion

In this study, the plots of electron density along with the electron barrier tunneling and electrostatic potential distribution of homo and hetero DG TFETs were extracted. The simulated values were validated by fitting them with their corresponding analytical expressions. It could be observed that a simulated value shows good agreement with the modeled values for all the devices taken into consideration. The injection of carriers at a higher velocity from the source side have enhanced the electrostatic potential for DG TFETs with gate-drain overlap in comparison with the DG TFETs without overlap. Also, the high density of the electrons at the source end and higher

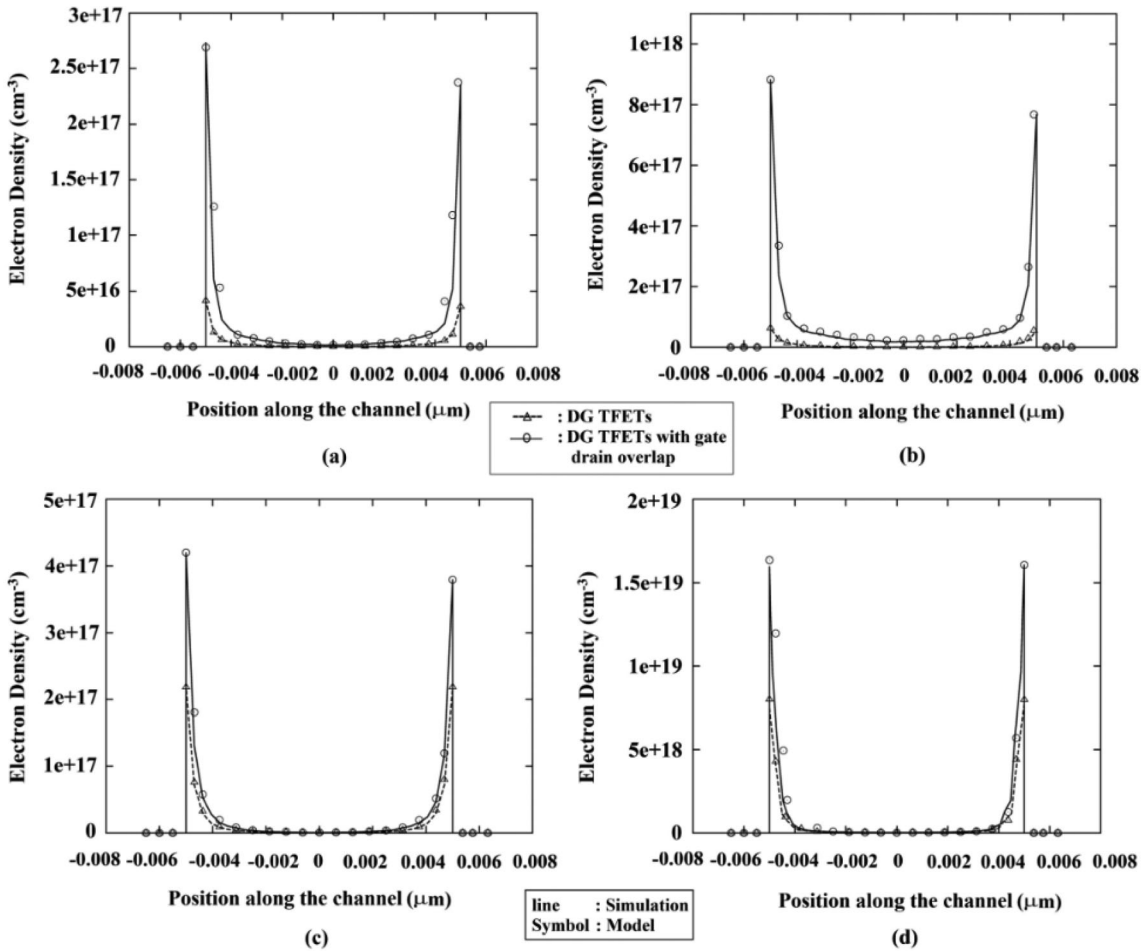

Fig. 7 Electron Density of (**a**) Si based DG TFETs (**b**) SiGe/Si based DG TFETs (**c**) InAs/Si based DG TFETs and (**d**) GaSb/Si based DG TFETs

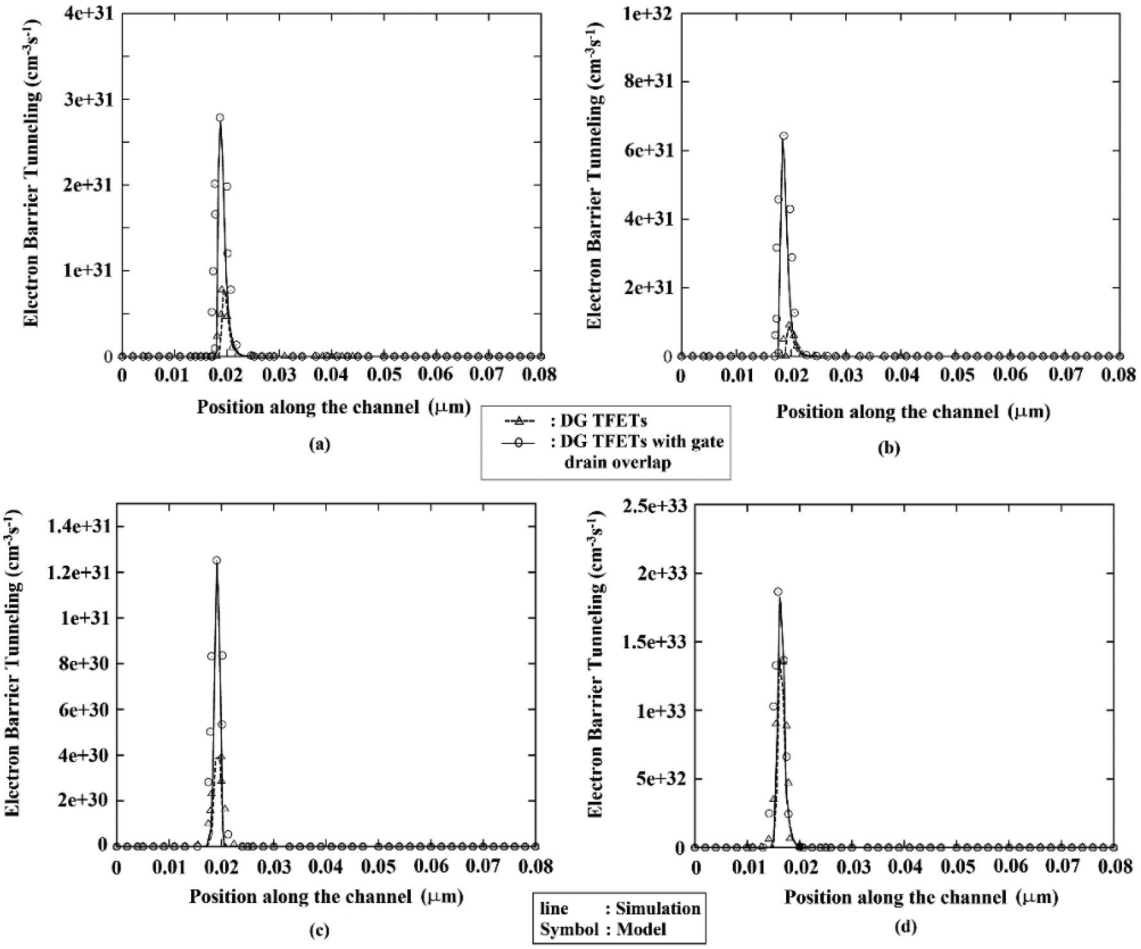

Fig. 8 Electron Barrier Tunneling of (**a**) Si based DG TFETs (**b**) SiGe/Si based DG TFETs (**c**) InAs/Si based DG TFETs and (**d**) GaSb/Si based DG TFETs

tunneling probability rate have improved the device performance for DG TFETs with gate-drain overlap in comparison to DG TFETs without overlap, leading to increased I_{ON}. From the material aspect, GaSb/Si based DG TFETs with gate-drain overlap provides enhanced device performance compared to DG TFETs without overlap due to its material property, electron affinity. Hence heterjunction based DG TFET seems to be a promising candidate for future RF/ analog or mixed signal circuit applications.

Author Contributions S. Poorvasha and B. Lakshmi have contributed to the design and implementation of the research, to the analysis of the results and to the writing of the manuscript.

Data Availability Not Applicable.

Compliance with Ethical Standards This study was approved by the university research ethics committee. All procedures performed in this study follow the ethical standards of the institutional and research committee.

Conflict of Interest The authors declare that there is no conflict of interest.

Consent to Participate Not Applicable.

Consent for Publication Yes

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