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ORIGINAL PAPER

Simulation Study of Carbon Vacancy Trapping Effect on Low Power 4H-SiC MOSFET Performance

Hichem Bencherif[1] · **Lakhdar Dehimi**[2,3] · **Nour eddine Athamena**[1] · **Fortunato Pezzimenti**[4] · **Mohamed Larbi Megherbi**[2] · **Francesco Giuseppe Della Corte**[4]

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Abstract

The carbon vacancy in 4H-SiC is an important recombination center of the minority carrier and a direct consequence of SiC-based device degradation. In 4H-SiC, this defect acts as the primary carrier-lifetime killer. Whether, low-energy electron radiation exposure or high temperature processing in an inert ambient gas will produce the carbon vacancy defect. Despite, the extensiveness of the studies concerning the defect's modeling and characterization, numerous essential questions remain. Amongst them, we have the impact of these defects on the performance of 4H-SiC MOSFET. Herein, the influence of intrinsic defect states, namely, $Z_{1/2}$ and $EH_{6/7}$ centers, on the 4H-SiC MOSFET electrical outputs is examined via 2D numerical simulation. The obtained results show that the traps act to increase the device on-state resistance (R_{ON}), reduce the channel mobility, increase the threshold voltage (V_{th}). Besides, the increase of the temperature leads to less influence of the traps on the threshold variation. Furthermore, due to their locations in the bandgap, the impact of both $Z_{1/2}$ and $EH_{6/7}$ centers at room temperature on the device electrical outputs is extreme. For high temperature the $EH_{6/7}$ have the severest impact because of the cross section temperature dependency.

Keywords 4H-SiC · Low power MOSFET · Defect states · Device modeling · ON-state resistance

1 Introduction

In state-of-the-art power electronics, silicon carbide (SiC) based MOSFETs are very interesting devices [1]. They are broadly valued for their high efficiency, noticeable switching capabilities and low on-state resistance. Silicon carbide exhibits a low drift region resistance allowing the design of extremely high voltage devices with reduced on-state voltage drop and outstanding switching characteristics. Furthermore, 4H-inherent SiC's material properties, specifically its large bandgap structure, are responsible for its outstanding output at elevated temperatures. SiC has three times greater bandgap energy than Si (3.24 eV vs 1.1 eV), which mitigates the impact of high temperatures on the conduction of minority carriers through reverse recovery in SiC systems. Besides, SiC has around six times Si′s breakdown field, providing high blocking voltages. In conclusion, the three-fold higher SiC thermal conductivity reduces the high temperature effects down to at least 150 C compared to Si, where substantial rises in the reverse recovery charge and leakage current over 100 C are reported. Standard SiC MOSFETs are intended to sustain high breakdown voltages varying from 0.6 to 2 KV [2–4]. Though, Low breakdown voltage 4H-SiC MOSFETs for photovoltaic (PV) applications has also been discussed in new research studies [5–10]. Hence, they will be able to operate in harsh conditions ensuring a considerable life-time. In fact, in PV modules, power optimizers are typically utilized at voltages in the range of 100–200 V.

A key material problem for these devices is the control accuracy of the lifetime of the carrier that is needed to maximize the output of the device. The charge carrier lifetime is modified in the material through recombination by deep levels, of which the main recombination center was identified to be the $Z_{1/2}$ center in the as-grown 4H-SiC material [11, 12]. The center consists of two negative -U, double-acceptor-like levels,

✉ Hichem Bencherif
hichem.bencherif@univ-batna2.dz;
hichem.bencherifeln@gmail.com

[1] University of Mostefa Ben Boulaïd, Batna 2, Batna, Algeria

[2] LMSM laboratory, University of Biskra, Biskra, Algeria

[3] Faculty of Science, University of Batna 1, Batna, Algeria

[4] DIIES, Mediterranea University of Reggio Calabria, Reggio Calabria, Italy

and was specifically defined as arising from the defect of the carbon vacancy (CV) [13–16]. CV has also been estimated by Abinitio calculations to have single donor (+ /0) and double donor (2+/+) levels deeper in the bandgap in addition to the acceptor (−/0) and double-acceptor (2−/−) levels [14, 17–21]. Indeed, the existence of deep defects has a significant effect on the electrical characteristics of MOSFET based on 4H-SiC and, probably depends on their capture cross-section. These defects behave either as traps or as recombination centers for electrons and holes. The free carrier density of semiconductor is reduced by traps located inside the band gap, while recombination centers implement generation-recombination current through rectifying devices [5, 6]. Consequently, in order to get information about defect operation, intense efforts should be made to recognize the essential scattering mechanisms. The study of the reliability of the 4H-SiC MOSFET through device manufacture or measurement via experimental analysis is considered to be very costly and time-consuming. Due to all these constraints, numerical simulations can be used to examine device performance and reliability.

In this article, the electrical characteristics of a 4H-SiC MOSFET designed for low voltage (150 V) over a broad range of temperatures are investigated on the basis of a detailed numerical simulation study. Preliminary results at room temperature and neglecting CV defect effects are presented in [15–17]. For a device with no CV defects (density of 10^{13} cm^{-2} [22]), its R_{ON} is in the order of 200 kΩ×μm2 at V_{GS} = 15 V,V_{DS} = 1 V and T = 300 K. Such performances can be reached by the suppression of the CV defects, which is attained experimentally by: (a) Implantation of carbon ions and subsequent annealing at 1600–1800° C [23, 24], (b) High-temperature thermal oxidation (1200–1400° C) [25, 26], (c) thermal annealing with a carbon cap [27], (d) Post-growth annealing will minimize CV defects by providing hydrocarbon gas diluted in hydrogen.

The founding elucidates the role of the CV defects in decreasing the channel mobility. Simultaneously the threshold voltage of the device increases harshly as the trap density and temperature increase which can be considered as insignificant effect. Finally, this study indicates that $Z_{1/2}$ at 300 K have harsh effect in determining the R_{ON} of the MOSFET, as well as the $EH_{6/7}$becomes dominant traps once the temperature increased.

2 MOSFET Structure

Cross-sectional view of the assumed n-channel 4H-SiC MOSFET is illustrated in Fig. 1. The geometrical parameters are described as follows: W_{cell} and W_G denote the cell width and the gate contact width, respectively. W_J and W_{drift} represent the space between the base regions and the n$^-$ drift region thickness, respectively. W_{drift} and W_{sub} are the base-to-substrate distance and the starting substrate thickness,

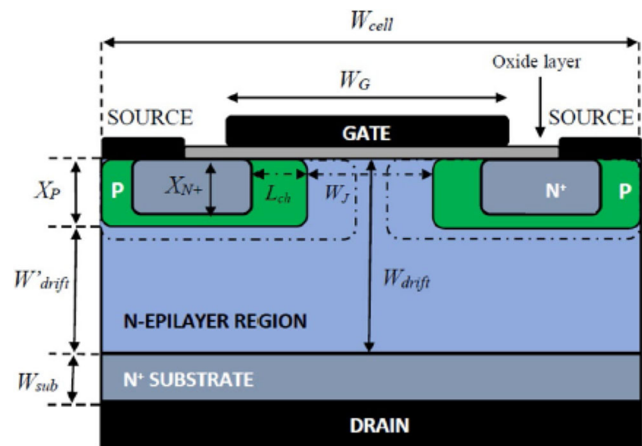

Fig. 1 The 4H-SiC MOSFET Cross-sectional View

respectively. X_{N+} represents the depth of source junction (n+), X_P is the depth of the p-base junction, L_{ch} represents the device channel length. To avoid the switch-on of the parasitic epilayer (n)/base (p) /source (n+) bipolar junction transistor, the source contact shorts the source and base regions. Table 1 summarizes the geometrical and physical parameters used during the simulations.

From Table 1, the epilayer thickness (W_{drift}) of 1.8 μm ensures a BV_{DS} value close to 150 V.

Although to simplify the simulation purposes, the proposed structure is, in principle, designed compatible with a manufacturing process based on doping by ion implantation [28–30].

3 Physical Models

The numerical study was performed via Atlas-Silvaco TCAD physical simulator [31]. In particular, the device structure was

Table 1 4H-SiC MOSFET references parameters

Design parameters	Values
Gate contact width, W_G (μm)	9.4
Cell width, W_{cell} (μm)	15
oxide thickness, T_{OX} (μm)	0.08
Channel length, L_{ch} (μm)	1
Source thickness, X_{N+} (μm)	0.5
N^+-source doping, N_D (cm^{-3})	1×10^{18}
Base junction depth, X_P (μm)	1.3
P-base doping, N_A (cm^{-3})	1×10^{17}
Base-to-base distance, W_J (μm)	7
Epilayer thickness, W_{drift} (μm)	1.8
Base-to-substrate distance, $W_{_drift}$ (μm)	0.5
N_{drift} doping, N_{drift} (cm^{-3})	1×10^{15}
Substrate thickness, W_{sub} (μm)	100
N^+-substrate doping, N_{sub} (cm^{-3})	1×10^{19}

finely meshed underneath the SiO_2/4H-SiC interface all across the p-n junctions and the surface channel area. A number of mesh points around 32,000 is assumed and at the interfaces, the mesh distance was reduced in size to 0.5 nm.

The main physical models accounted include the temperature dependence of the 4H-SiC bandgap, the apparent narrowing effect of the bandgap, the recombination mechanisms of Auger and Shockley-Read-Hall, the incomplete activation of doping, the ionization of effects, and the expressions of carrier lifetime and carrier mobility depending on temperature and doping concentration.

The numerical simulation includes the following expressions to model Auger and SRH recombination rates [32]:

$$R_{Auger} = (C_P p + C_n n)\left(np - n_i^2\right) \tag{1}$$

where C_n and C_p refers to the Auger coefficients.

$$R_{SH} = \frac{pn - n_i^2}{\tau_p\left(n + n_i \exp\left(\frac{E_{trap}}{kT}\right)\right) + \tau_n\left(p + n_i \exp\left(\frac{-E_{trap}}{kT}\right)\right)} \tag{2}$$

E_{trap} denotes the energy gap that separate trap energy and intrinsic Fermi levels. τ_n and τ_p are the carrier lifetimes.

In order to calculate the breakdown voltage thoroughly, electron and hole impact ionization rates $\alpha_{n,\ p}$ are expressed [33]:

$$\alpha_{n,p} = \alpha_{0n,p} \exp\left(\frac{-b_{0n,p}}{E}\right) \tag{3}$$

where the coefficients $\alpha_{0n,\ p}$ and $b_{0n,\ p}$ are measured [33].

According to [34], incomplete impurity ionization is expressed as follows:

$$N_{d^+,a^-} = N_{d,a}\left(\frac{-1 + \sqrt{1 + 4g_{d,a}\frac{N_{d,a}}{N_{C,V}(T)}\exp\left(\frac{\Delta E_{d,a}}{kT}\right)}}{2g_{d,a}\frac{N_{d,a}}{N_{C,V}(T)}\exp\left(\frac{\Delta E_{d,a}}{kT}\right)}\right) \tag{4}$$

The subscripts d and a signify, donor and acceptor, respectively. $N_{d,\ a}$ refers to the doping densities. $\Delta E_{d,\ a}$ stands for energy levels. $g_{d,\ a}$ is the degeneracy factors of the conduction and valence band. N_C, N_V are the conduction and valence states densities, respectively.

According to Lindefelt's model [35], the bandgap narrowing effect for p-type (ΔE_{ga}) and n-type (ΔE_{gd}) regions are expressed as:

$$\Delta E_{ga} = A_a\left(\frac{N_a^-}{10^{18}}\right)^{\frac{1}{2}} + B_a\left(\frac{N_a^-}{10^{18}}\right)^{\frac{1}{3}} + C_a\left(\frac{N_a^-}{10^{18}}\right)^{\frac{1}{4}} \tag{5}$$

$$\Delta E_{gd} = A_d\left(\frac{N_d^+}{10^{18}}\right)^{\frac{1}{2}} + B_d\left(\frac{N_d^+}{10^{18}}\right)^{\frac{1}{3}} + C_d\left(\frac{N_d^+}{10^{18}}\right)^{\frac{1}{4}} \tag{6}$$

where $A_{a,\ d}$, $B_{a,\ d}$and $C_{a,\ d}$ are specific material parameters.

Furthermore, Fermi-Dirac statistics and multidimensional dependent anisotropic effects (Aniso) are taken into account in all the simulations. In reference [31], a complete overview of the models used can be found. In order to take into account the scattering mechanisms, that hinders the channel mobility Lombardi model is assumed. This model account for phonon scattering, surface roughness scattering, impurity scattering and coulomb scattering, and verified for SiC MOSFET simulations [36].

Based on the experimental validation of [37], the Caughey-Thomas analytical model is used to express the carrier's mobility. It is worth noting that all the physical models used in this investigation are intensively exploited by our laboratory researchers [38, 39]. Besides, the experimental results are a concrete validation of the considered device in a broad range of temperatures [40–42].

4 Results and Discussion

The objective of this analysis is to study the degradation of 4H-SiC MOSFET's electrical characteristics through using specialized simulator. This degradation is caused by both interactions with energetic particles or by the growth of the epitaxial layer attributed to crystal defects formation.

The carbon vacancy acceptor level (named $Z_{1/2}$ center [43] has been recognized as the main lifetime killer, in lightly doped n-type SiC [44, 45]. The energy levels of a carbon vacancy (CV) defect in SiC are shown in Fig. 2 [46, 47]. The (2−/−) and (−/0) levels named "$Z_{1/2}$ center" are energetically situated closely to each other. The (2−/−) level is lower than the (−/0) level, suggesting that the negative -U nature of

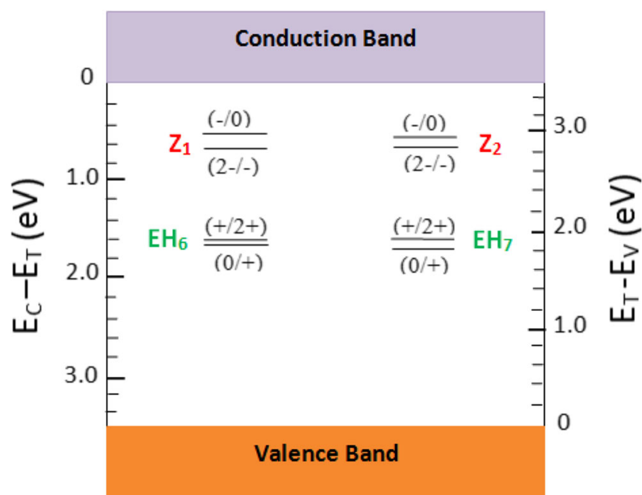

Fig. 2 Energy levels of a carbon vacancy (CV) defect in 4H-SiC [46, 47]

Table 2 Fundamental traps parameters [53, 54]

Trap name	Location (eV)	Density (cm^{-3})	Electron cross section (cm^2) 300 K	Hole cross section (cm^2) 300 K
$\mathbf{Z_{1/2}}$	0.67	$0.01–3\times10^{16}$	2×10^{-14}	3.5×10^{-14}
$\mathbf{EH_{6/7}}$	1.65	$0.01–3\times10^{16}$	2.4×10^{-13}	1.0×10^{-15}

the $Z_{1/2}$ center is present [48]. In other terms, two electrons are attracted or generated from the center of $Z_{1/2}$ practically at the same. The Z_1 and Z_2 centers arise from a carbon vacancy in the middle of the hexagonal site and in the lattice of the cubic site respectively [46]. The levels (0/+) and (+/2+) are narrowly located and named the "$EH_{6/7}$ center" [47, 49]. Experimental and theoretical studies have established the sources of both $Z_{1/2}$ and $EH_{6/7}$ centers as various charge states of carbon mono-vacancy in SiC [46, 50–52]. Furthermore, it was reported that the centers $Z_{1/2}$ and $EH_{6/7}$ arise from the same defect point with diverse charge states and are positioned at the edge of the conduction band at 0.67 eV and 1.65 eV, respectively [50]. Density Function Theory (DFT) calculation supports these experimental results [46, 51].

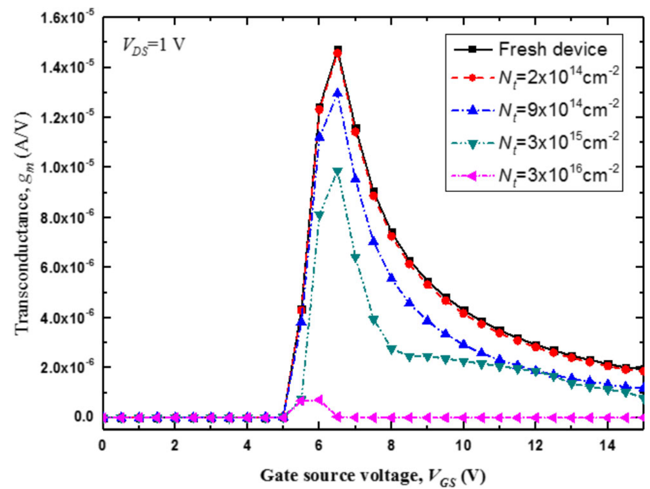

Fig. 4. transconductance as function of gate source voltage for different $Z_{1/2}$ intrinsic traps density values, at T=300 K

Table 2 lists the basic traps parameters considered during the simulations.

(a)

(b)

(c)

Fig. 3 Transfer characteristics in linear scales for different intrinsic traps $Z_{1/2}$ values, **a**) T=300 K, **b**) T=400 K, **c**) T=500 K

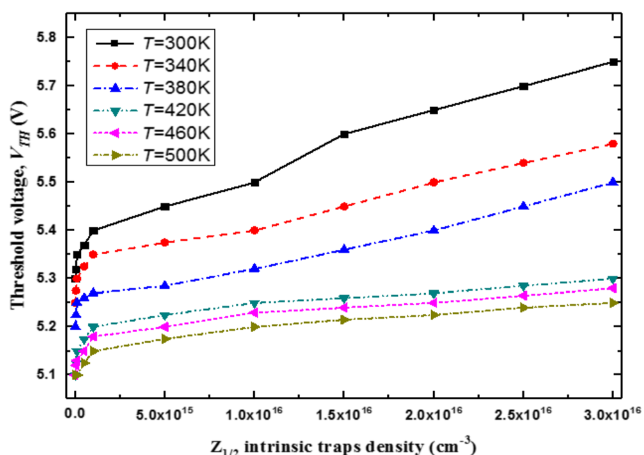

Fig. 5 V_{th} as function of $Z_{1/2}$ intrinsic traps values for different temperature values

4.1 I-V-T Characteristics

4.1.1 Effect of $Z_{1/2}$ Intrinsic Traps

By considering the 4H-SiC MOSFET described in Table 1 with different $Z_{1/2}$ intrinsic traps densities, the current density curves I_D-V_{GS} for different V_{DS} for the device in Fig. 1 (A = 7.5μm^2) at different temperatures are shown in Fig. 3.

As intended, by raising the temperature, the drain current reduces severely. The temperature dependence of the carrier mobility in the inversion layer and the increase in total on-state resistance determine this effect.

Moreover, it can be observed from Fig. 3 that when the intrinsic traps $Z_{1/2}$ density increases the drain current decreases. The main explanation for this lies in the affected flow of electrons, due to defect effects that arise in the drift region. The drain current is thus reduced because these defects minimize the lifetime of the carrier and serve as carrier traps in the active region of the device, adding high-resistive ways.

A basic figures of merit is the transconductance g_m. The greater the transconductance, the greater the cut-off frequency. The g_m curve as a function of V_{GS} for different $Z_{1/2}$ centers traps density values is shown in Fig. 4. It is obvious from Fig. 4 that the more the traps density increase the more the g_m is penalized. This fact is mainly due to the effect of the acceptor-level of a carbon vacancy (named "$Z_{1/2}$ center"), recognized to be the primary carrier-lifetime killer in SiC [55]. With $_{VGS}$ firmly higher than the device threshold voltage ($V_{GS} \geq 4.5$ V for $V_{DS} = 1$ V), significant increases of gm can be

Fig. 6 Transfer characteristics (I_{DS}-V_{GS}) in linear scales for different $EH_{6/7}$ intrinsic traps values, **a**) T=300 K, **b**) T=400 K, c) T=500 K

attained. A g_m peak close to 15 μAV^{-1} is calculated for V_{DS} = 1 V and V_{GS} = 6.5 V.

Figure 5 depicts the threshold voltage variation with $Z_{1/2}$ intrinsic traps density for different temperature values. The device's threshold voltage tends to increase as the traps density increases. This fact is due to the defect effects that increase the local recombination rate via reducing carriers' life time. The $Z_{1/2}$ center shows the negative -U nature [48], i.e.: two electrons are simultaneously confined at or emitted from the $Z_{1/2}$ center, which in turn make the channel creation more difficult by excluding the electrons from the carrier transport mechanisms.

In order to reduce the $Z_{1/2}$ center density, the optimization of the epitaxial growth condition is required. The density of the $Z_{1/2}$ center in SiC epitaxial layers is, in fact, highly dependent on the conditions of growth [24–26, 56–59]. Besides, the higher the temperature the lower the number of filled traps, so the threshold voltage is reduced.

4.1.2 Effect of $EH_{6/7}$ Intrinsic Traps

The capture cross-section of electrons (minority p-type carriers) for the $EH_{6/7}$ center has been identified to be far wider than that of holes [47], since the attractive force of Coulomb operates between the positively charged CV defect ($EH_{6/7}$) and the electron. Nevertheless, in order to clarify the dominating mechanism of carrier recombination in SiC material, further studies are needed (Fig. 6).

The transconductance g_m versus $_{VGS}$ for different densities of $EH_{6/7}$ centers is shown in Fig. 7. It is shown in Fig. 7 that increasing the traps density cause a decrease in the g_m, this is linked to the penalized carrier lifetime due to the augmentation of carbon vacancy donor-level. With V_{GS} firmly above the system threshold voltage ($V_{GS} \geq 4.5$ V for V_{DS} = 1 V), maximum value of g_m can be attained. V_{DS} = 1 V and V_{GS} = 6.5 V was estimated to have a g_m maximum around 15 μAV^{-1}.

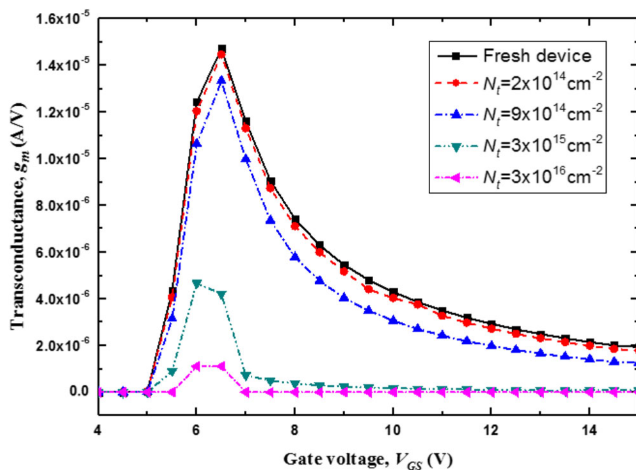

Fig. 7. transconductance as function of different $EH_{6/7}$ intrinsic traps values at room temperature

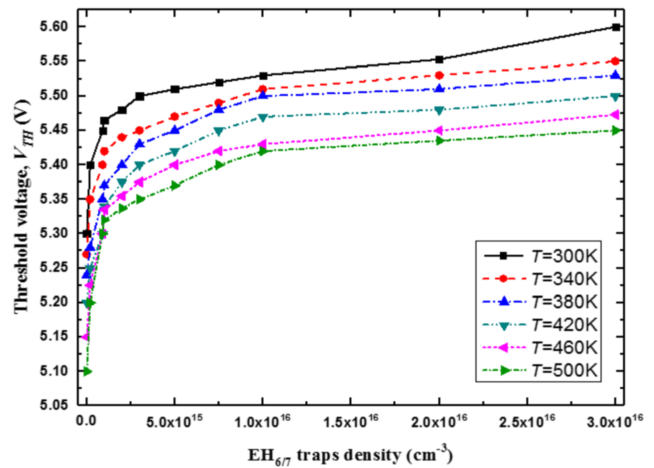

Fig. 8 V_{th} as function of $EH_{6/7}$ intrinsic traps values for different temperature values

Figure 8 shows the threshold voltage versus $EH_{6/7}$ intrinsic traps density with different temperature values. The threshold voltage of the system continues to increase as the density of the traps increases, this is attributed to the defect effects that increase the local recombination rate through the reduction in

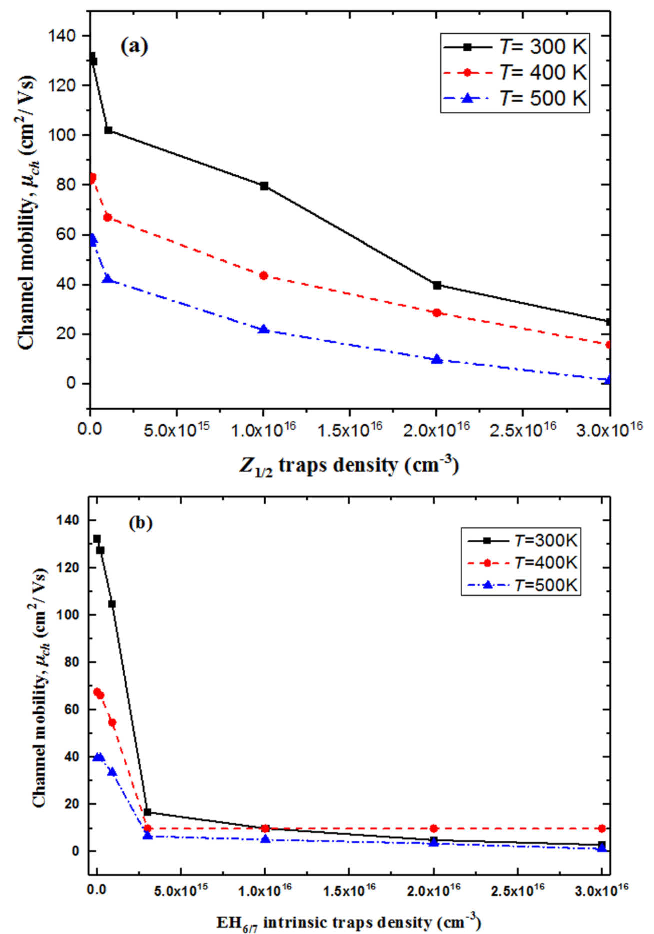

Fig. 9 Channel mobility as function of: **a**) $Z_{1/2}$ intrinsic traps values, **b**) $EH_{6/7}$ intrinsic traps values for different temperature values

the lifetime of the carriers. This in turn makes the formation of the channel more difficult by removing the electrons from the transport mechanisms of the carrier.

The $Z_{1/2}$ center together with $EH_{6/7}$ are really the merely deep levels identified in sufficient concentration in n- type 4H-SiC [42–44, 47]. The concentrations of these two centers are inversely associated with the lifetime of the minority carrier as well as the concentration of the nitrogen donor, and it was unclear which defect center was the responsible in decreasing the carriers' lifetime [48, 49]. Researcher conducted lifetime measurements and DLTS on a set of 4H-SiC epitaxial layers samples of growing thickness, and identified that the $Z_{1/2}$ concentration is very closely associated with the inverse effective lifetime [60]. Furthermore, this center has broad, perhaps identical, capture cross sections (10–14 cm^2), rendering it an effective recombination center. Conversely, the EH6/7 center concentration showed almost no relationship. The lifetime is no longer limited by the $Z_{1/2}$ center below a concentration of 1×10^{13} cm^{-3} [61], and it has been speculated that structural defects or surface recombination may dominate in this regime. In our study at temperature exceeding 300 K the 4H-SiC MOSFET is more affected by $EH_{6/7}$ than $Z_{1/2}$, this is mainly due to the dependence of EH6/7 capture cross sections on temperature and the correlation with the inverse effective lifetime.

4.2 Mobility and ON Resistance

This part concentrates on the ON state resistance R_{ON}. With a focus on channel mobility,

Figures 9-**a** and **9-b** show the channel mobility variation as function of $Z_{1/2}$ and $EH_{6/7}$ intrinsic traps density for a temperature range of 300 K-500 K. The channel mobility is reduced as well when the traps density increases; this may be due to the increased recombination rates in the inversion region.

The changes of the ON-resistance for different $Z_{1/2}$ and $EH_{6/7}$ concentrations are depicted in Fig. 10 in temperature range of 300 K–500 K. The existence of defects greatly augments the resistance, which depends heavily on the $Z_{1/2}$ at T=300 K and the $EH_{6/7}$ at temperatures above 300 K. In other words, $EH_{6/7}$ becomes the dominant defects at high temperature levels. It is a common knowledge, that among ON state

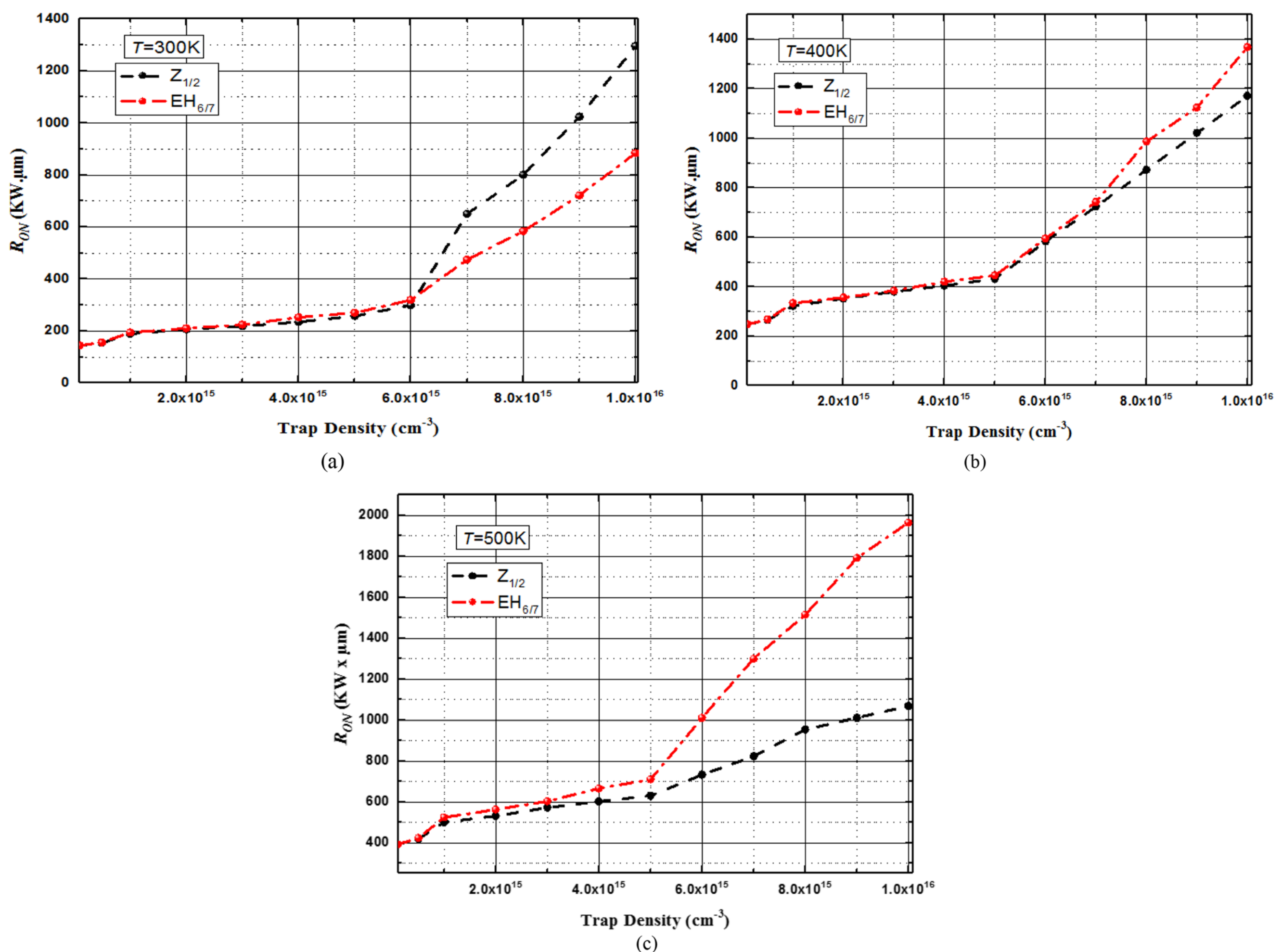

Fig. 10 Effect of different intrinsic traps' concentrations on the 4H-SiCMOSFET-ON resistance, **a**) T=300 K, **b**) T=400 K, **c**) T=500 K

resistance components that lay with drift layer cause a serious resistive path to the current flow. This is attributed to the defects produced in this region where the Fermi level is near the minima of the conduction band and the carbon vacancy is charged double-negative (2^{-}) through electron capture. Latest measurements using DLTS and minority carrier transient spectroscopy (MCTS) have observed that the capture cross section of a hole is very wide for the $Z_{1/2}$ center [64]. This is the major cause why the center of $Z_{1/2}$ acts in the n-drift region as an effective carrier recombination center. Besides, the $Z_{1/2}$,in the channel region, is positively charged and excludes electrons from channel which make R_{ch} increase. For the $EH_{6/7}$, this defect is positively charged in drift region which increases also the region resistance component. At high temperature the effect of EH6/7 is dominated this may be due to the temperature recombination cross section relationship.

5 Conclusion

In this paper, the effect of intrinsic defect states of silicon carbide, such as $Z_{1/2}$ and $EH_{6/7}$ centers, on the electrical merit Fig. 4H-SiC MOSFET is investigated using a physics-based simulator. The simulations show that the traps increase the device ON-state resistance (R_{ON}), reduce the channel mobility, increase the threshold voltage (V_{th}). In more detail, it was found that high intrinsic defect densities may lead to undesirable device properties and instability of the threshold voltage. The MOSFET channel mobility decreases harshly due to the increase of the carrier recombination rate. The defects create a resistive path in n-type SiC drift region which in turn increase the drift region resistance. Furthermore, due to their locations in the bandgap, the impact of both $Z_{1/2}$ and $EH_{6/7}$ centers at room temperature on the device's electrical outputs is harsher.

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Compliance with Ethical Standards

Conflict of Interest The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Consent to Participate Informed consent was obtained from all individual participants included in the study.

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