Silicon (2022) 14:521–529
https://doi.org/10.1007/s12633-020-00824-4

ORIGINAL PAPER

# Performance Analysis of Group IV Material Based Tunnel Field Effect Transistor: Effect of Drain Splitting and Introducing Ge-Strip at Source- Channel Junction

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Received: 26 September 2020 / Accepted: 3 November 2020 / Published online: 21 November 2020


**Abstract**
The performance effect of splitting and abrupt doping in the drain region, use of a Ge strip at source-channel junction in group IV material based ($Ge_{1-x}Sn_x$/ $Si_{1-y-z}Ge_ySn_z$) Tunnel Field Effect Transistor (TFET) is investigated in the present manuscript. The variation of certain device parameters, such as mole fraction, different gate dielectrics, gate dielectric thickness and drain doping concentrations are applied to analyze the performance of proposed group IV material based TFET in terms of current-voltage (*I-V*) characteristics, potential profile and $I_{ON}/I_{OFF}$ ratio using device simulator SILVACO TCAD. The simulation results obtained for the proposed TFET structure are compared with the other TFET structures available in the literature, which shows better results as $I_{ON}/I_{OFF}$ ratio was received of the order of $10^{12}$ in comparison to conventional group IV material based TFET and subthreshold swing of 25.03 mV/decade, which makes the proposed structure promising for high speed switching action with low power CMOS compatibility.

**Keywords** Subthreshold Swing (SS) · Ambipolar behavior · Tunnel field effect transistor (TFET) · ON current to OFF current ($I_{ON}$/ $I_{OFF}$) ratio · Tunneling$Ge_{1-x}Sn_x$/ $Si_{1-y-z}Ge_ySn_z$, etc.

## 1 Introduction

With the advancement and improvement in the technology, the market for portable products like smartphone, smartwatch, tablet, and notebook was growing due to which the demand for high scalability of CMOS (Complementary Metal Oxide Semiconductor) devices are increased. With the downscaling of the transistor, threshold voltage ($V_{th}$) and supply voltage ($V_{dd}$) must be reduced, by doing so, the overdrive ($V_{dd} - V_{th}$) factor remains high to meet the performance requirements [1]. As $V_{th}$ reduces, the off-state current ($I_{OFF}$) increases exponentially. However, to reduce $I_{OFF}$, sub-threshold swing (SS) must be reduced. In case of MOSFET, at room temperature, there was a physical restriction on the SS of 60 mV/decade because of the constant value of the $K_bT/q$ thermal voltage, (where $K_b$ is the Boltzmann constant, $T$ is the absolute temperature and $q$ is the charge of an electron) [2, 3]. The large value of SS caused a leakage current of the high value in the subthreshold part with the reduction in the device size. Furthermore, as per Moore's law, in the integrated circuit (IC), an exponential trend has been taking place in the miniaturization of the transistors for more than the past five decades i.e. in every two years approximately, there was a trend of doubling the number of the transistors per IC [4]. There was one more trend noticed by Koomey et al., that the rate of electrical efficiency has been steadily increasing or we can say, in every one and half a year, power consumption has been reduced by half [5]. To catch up with these important trends, currently researchers are primarily concentrated on designing and manufacturing devices with smaller feature size, better

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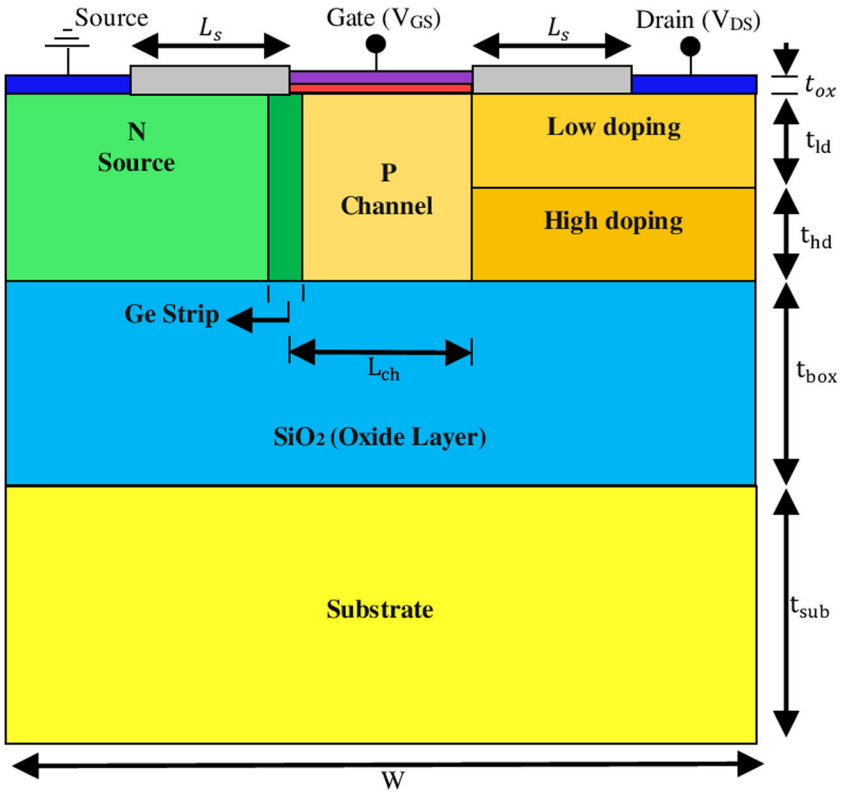


**Fig. 1** The cross-sectional sketch of the TFET structure

transfer and output characteristics without downgrading the electrical performance of the device. Hence, the small feature size of transistor tends to reduce the power consumption, delay and ultimately cost of manufacturing or fabrication [6]. However, with the decreasing transistor's geometry and reducing supply voltage, a various detrimental phenomenon like channel length modulation, short channel effects, and velocity saturation, etc. also starts arising. These detrimental factors guide to more leakage current as well as higher power consumption in an IC [3, 4]. To overpower such bottlenecks of the continued scaling, the need of the hour is to invent some novel devices and new technologies.

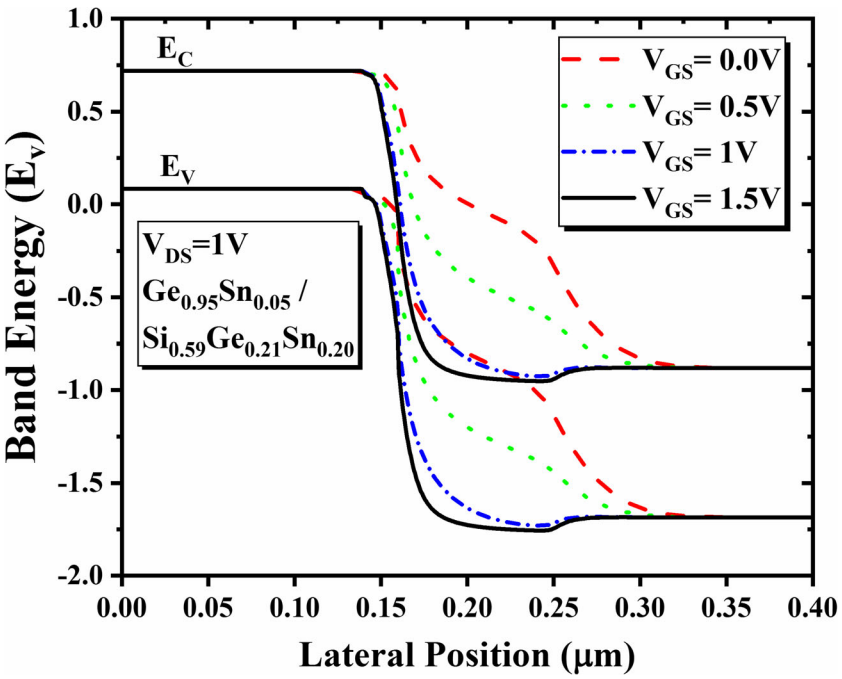


**Fig. 2** The Energy Bands of the proposed TFET at the different gate voltage levels i.e. 0.0 V, 0.5 V, 1 V and 1.5 V

**Table 1** The parameters of the proposed structure

| Position | Material | Doping ($cm^{-3}$) | Length (nm) |
|---|---|---|---|
| Source | $Ge_{1-x}Sn_x$ | $1x10^{20}$ | 150 |
| Channel | $Si_{1-y-z}Ge_ySn_z$ | $5x10^{16}$ | 100 |
| Drain | $Si_{1-y-z}Ge_ySn_z$ | $1x10^{17}$<br>$1x10^{19}$ | 150 |

Thus, various new devices with SS lower than 60 mV/decade have been put forward such as TFET [1, 7–11], FinFET [12], Impact ionization FET,'s (IFET) [13]. Among these devices, one of the highly favourable contenders, tunnel field effect transistor (TFET), reduces the leakage current and overcomes the limit of 60 mV/decade of mainstream metal oxide semiconductor field effect transistor (MOSFET) [14] and fast response time $I_{ON}/I_{OFF}$. The tunnel transistor appears to be a captivating device for quite a lot of analog & digital applications as it is considered as the potential descendant of CMOS technology [15]. Out of all the research studies, TFET came out to be the most reliable because of its inherent property of sub-60 mV/Dec SS employing high-speed performance and temperature insensitivity, was a gated reversed biased p-i-n diode which can be turned ON by applying appropriate gate bias.

However, TFET has some glitches like ambipolar behavior, low ON current ($I_{ON}$), etc. which degrades the performance and switching characteristics, that need to overcome before TFET completely supersede MOSFET in the semiconductor industry. So to compensate these problems, TFET structures have been introduced such as DGTFET to provide better gate control [8, 16], multi-gate [17, 18] multi-junction (PNPN) [19, 20] drain underlap, hetero-dielectric-gate (HG) [9], and overlapping gate on the drain [21]. To raise the ON current level, various TFET structures have been proposed so far using compounds like III-V semiconductors such as InAs and InGaAs [22]. However, they have a lattice mismatch, with current planar CMOS technology in semiconductor fabrication. Besides, the III-V group materials have some more limitations such as highly toxic, very costly, lack of integration and some immaturity problems.

Nowadays, group IV semiconductor materials compounded with tin (Sn) have drawn more consideration from researchers [23–25]. Both of the strained and unstrained GeSn alloys can now be successively developed over the virtual substrates (VS) evolved upon the silicon wafer. With appropriate strain or the concentration of tin (Sn) surpassing 6–8% in GeSn, the alloy demonstrates a direct bandgap [26]. The compatibility of GeSn with CMOS platform, direct bandgap, and high mobility make it a potential contender for employing in TFET [27].

The prime focus of this literature is to study the impact of using material $Ge_{1-x}Sn_x$ and highly doped Ge strip, in the source region and at the source-channel junction respectively and $Si_{1-y-z}Ge_ySn_z$ material for channel and drain regions. In the drain region of the newly proposed TFET structure, an abrupt doping profile is utilized to obtain high ON current, low sub-threshold swing, low OFF current and for suppression of ambipolar behavior through simulation results. Also, due to the low bandgap of Ge material, it will steer to downsizing of the tunneling width, consequently, it will increase the tunneling current. Further, the impacts of various parameters like dielectric material of the gate oxide, doping concentration of materials used and the thickness of the gate oxide are also studied on the performance of the tunnel field effect transistor.

The organization of this manuscript is as follows: Section II explains about the structure of the device, Section III describes the theory related to the device, results and discussions were arranged in Section IV. Ultimately, the conclusion part of this paper laid out in section V.

## 2 The Device Structure

A cross-sectional sketch of a $Ge_{1-x}Sn_x/Si_{1-y-z}Ge_ySn_z$ material based TFET design was depicted in Figs. 1 and 2. This work was mainly focused on the device simulation using TCAD of the proposed structure. There were two major dissimilarities between typical conventional TFET structure and the proposed TFET structure [13], first, the later has employed a highly doped Ge strip at the source-channel junction and second, there was a divided drain region (a lightly doped region above the heavily doped region) in place of a constantly doped unified drain region. The studied device was an n-type $Ge_{1-x}Sn_x/Si_{1-y-z}Ge_ySn_z$ heterojunction TFET. To make tunneling possible in the proposed device, the doping concentrations employed in the source as well as in the drain regions were maintained inconsistent. The splitting of the drain region also helps in suppressing the ambipolar behavior of a proposed n-channel TFET without deteriorating the performance. Besides, a highly doped strip of Ge material was introduced at the source-channel junction, proved helpful to increase the level of ON current of the device. The abruptness used in

**Table 2** The Band parameters at $L$ and $\Gamma$ valleys used for band alignment calculation [32–34]

| Valley | $E_{Ge}$ (eV) | $E_{Si}$ (eV) | $E_{Sn}$ (eV) | $b_{GeSi}$ (eV) | $b_{GeSn}$ (eV) | $b_{SiSn}$ (eV) |
|---|---|---|---|---|---|---|
| **L** | 0.66 | 2 | 0.14 | 0.0 | 0.91 | 0.0 |
| $\Gamma$ | 0.795 | 4.06 | −0.413 | 0.21 | 2.1 | 13.2 |

**Table 3** The comparison of the ON current ($I_{ON}$) and the OFF current ($I_{OFF}$) between established and proposed device(s)

| Paper | $I_{ON}$ (A/$\mu$m) | $I_{OFF}$ (A/$\mu$m) | $I_{ON}/I_{OFF}$ |
|---|---|---|---|
| Reference [1] | $1 \times 10^{-6}$ | $1 \times 10^{-17}$ | $10^{11}$ |
| Reference [15] | $0.9 \times 10^{-6}$ | $1 \times 10^{-15}$ | $\sim 10^{9}$ |
| Proposed Work | $1 \times 10^{-5}$ | $1 \times 10^{-17}$ | $10^{12}$ |

the doping profile of the drain increases the electric field, which as a result increases the tunneling current.

The horizontal dimensions of the proposed structure were displayed in Table 1. The Ge strip was chosen to be 20 nm. The material used for the gate dielectric was $SiO_2$ with the thickness ($t_{ox}$) of 2 nm. The gate work function of 3.92 eV was considered in this work. For this TFET configuration, the doping concentration of source $N^+$ ($Ge_{1-x}Sn_x$) was set to $1x10^{20}cm^{-3}$. The doping concentration of $1x10^{18}cm^{-3}$ was taken for the Ge strip used in the TFET whereas channel $P^+$ ($Si_{1-y-z}Ge_ySn_z$) was doped at $5x10^{16}cm^{-3}$. The doping concentrations used in the upper and the lower drain regions were preferred as $1x10^{17}cm^{-3}$ and $1x10^{19}cm^{-3}$ respectively as tabulated in Table 1.

The energy band diagram with the different gate voltage levels i.e. 0.0 V, 0.5 V, 1 V and 1.5 V was displayed in Fig. 4. When we start increasing the positive gate bias in the ON state, the energy band of the channel area was brought down, which reduces the widening of the tunneling barrier. As the energy barrier got reduced, tunneling of charge carriers occurred from the valence band of the source at the source-channel junction to the conduction band of the channel-drain interface, which leads to the formation of tunneling current. A considerable change can be noticed in the valence and conduction band energy levels close to the channel area. The tunneling width can be spotted decreasing, with the gate voltage increased from 0.0 V to 1.5 V. This change allows the band-to-band tunneling (BTBT) phenomenon.

## 3 Theory

The drain current of the TFET can be determined by various factors like $V_{GS}$ (gate-to-source voltage), $V_{DS}$ (drain-to-source voltage), the material used and some other device parameters. The relationship of the drain current with different material parameters is given as-

$$I_D \propto exp\left[-\frac{4\sqrt{2m^*}E_G^{*\frac{3}{2}}}{3|e|\hbar\left(E_G^* + \Delta\Phi\right)}\sqrt{\frac{\varepsilon_{si}}{\varepsilon_{ox}}t_{si}t_{ox}}\right]\Delta\Phi \quad (1)$$

where $m^*$, $E_G^*$, $\hbar$ and $\Delta\Phi$, are the carrier's effective mass, effective bandgap, normalized Plank's constant and the energy overlap window respectively, while $\varepsilon_{si}$, $\varepsilon_{ox}$, $t_{si}$ and $t_{ox}$ represent the relative permittivity of the Silicon, the relative permittivity of the oxide of the metal gate, the thickness of the Si and the thickness of gate oxide respectively [28]. From eq. 1, we can derive that the level of the tunneling current may be enhanced by raising the value of the dielectric constant of the gate oxide ($\varepsilon_{ox}$), by lowering the gate oxide thickness ($t_{ox}$), by using material of smaller bandgap ($E_G^*$) and of lower effective carrier mass ($m^*$). So, the drain current $I_D$ can be controlled by any of the above parameters.

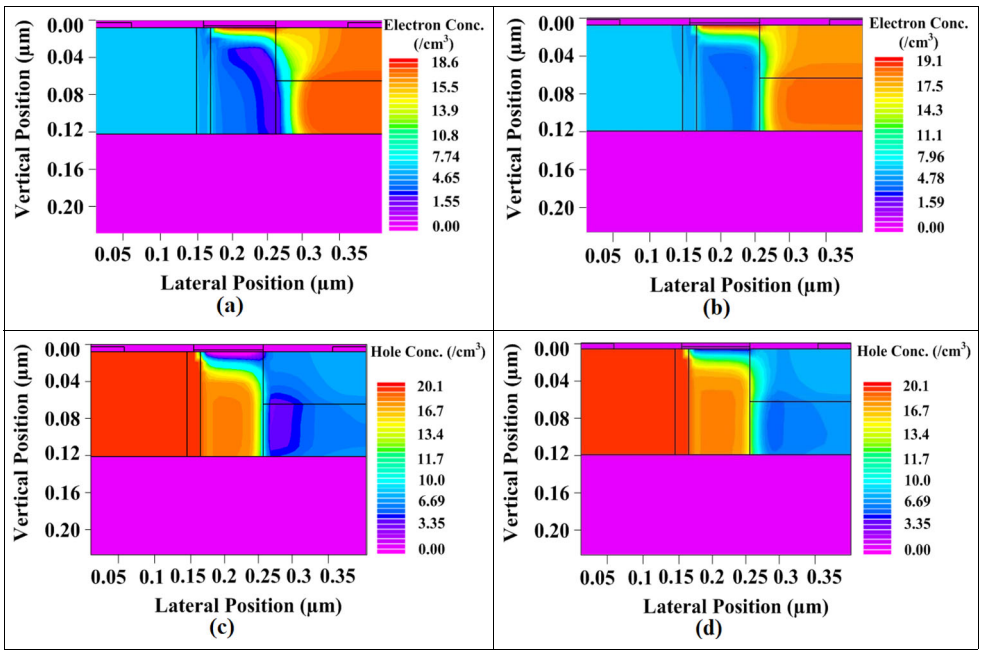


**Fig. 3** The contour plots of the electron carrier concentrations at (**a**) $V_{GS} = V_{DS} = 0$ V (**b**) $V_{GS} = V_{DS} = 1$ V and hole carrier concentration at (**c**) $V_{GS} = V_{DS} = 0$ V (**d**) $V_{GS} = V_{DS} = 1$ V

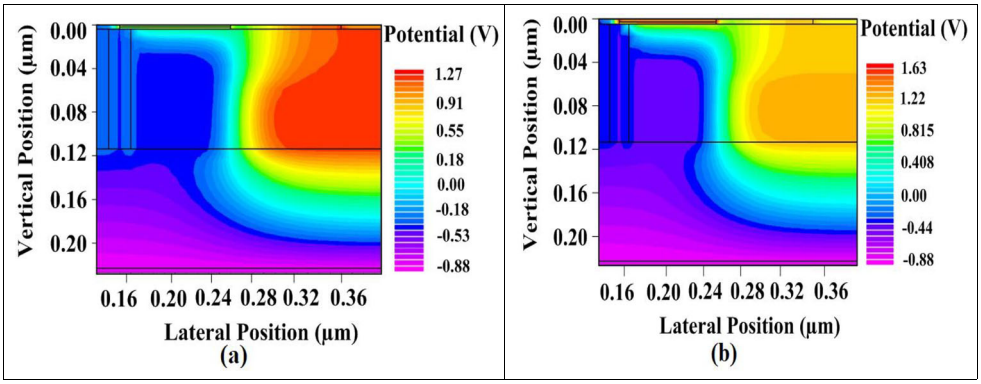


**Fig. 4** The potential distribution in the proposed structure at (**a**) $V_{GS}$ = 0 V, (**b**) $V_{GS}$ = 1 V

The Subthreshold region describes the region where the switching takes place between the ON state level and OFF state level. For switching in digital logic such as low-power devices and some memory devices, the SS is very significant.

The mathematical expression of subthreshold swing (SS) for the Field Effect Transistor (FET) can be given as

$$SS = \frac{dV_{GS}}{d(logI_D)} \tag{2}$$

where $V_{GS}$ and $I_D$ are gate-to-source voltage and drain current respectively.

For the operation of low power devices, for a transistor, it was much preferable to have a smaller value of SS. TFET gives a smaller value of SS i.e. typically less than 60 mV/decade, while there was a limit of 60 mV/decade in MOSFET's context at room temperature. Hence, because of the small value of SS, the TFET device can function at very high speed (switching) for small supply voltages. [29, 30]

The energy bandgap structures for the materials $Ge_{1-x}Sn_x$ and $Si_{1-y-z}Ge_ySn_z$ were measured by employing the nonlocal empirical pseudopotential method (EPM) [26, 31] and Table 2 shows the band parameters at $L$ and $\Gamma$ valleys used for band alignment calculation [32–34].

The bandgap of $Ge_{1-x}Sn_x$ *and* $Si_{1-y-z}Ge_ySn_z$ were fitted as per experimental data [34].

$$E_G(Ge_{1-x}Sn_x) = (1-x)E_G(Ge) + xE_G(\mathrm{Sn}) - x(1-x)b_T(GeSn) \tag{3}$$

$$E_G(Si_{1-y-z}Ge_ySn_z) = (1-y-z)E_G(Si) + yE_G(Ge) + zE_G(Sn) - (1-y-z)yb_T(GeSi) - yzb_T(GeSn) - (1-y-z)zb_T(SiSn) \tag{4}$$

where $E_G(Ge)$, $E_G(Si)$, $E_G(Sn)$ are the bandgaps of Germanium, Silicon and Tin respectively and.

$b_T(GeSi)$, $b_T(GeSn)$, $b_T(SiSn)$ are the bowing parameters as listed in Tables 2 and 3.

## 4 Results and Discussion

All the simulations presented in this paper have been realized using the SILVACO TCAD ATLAS module. To consider the

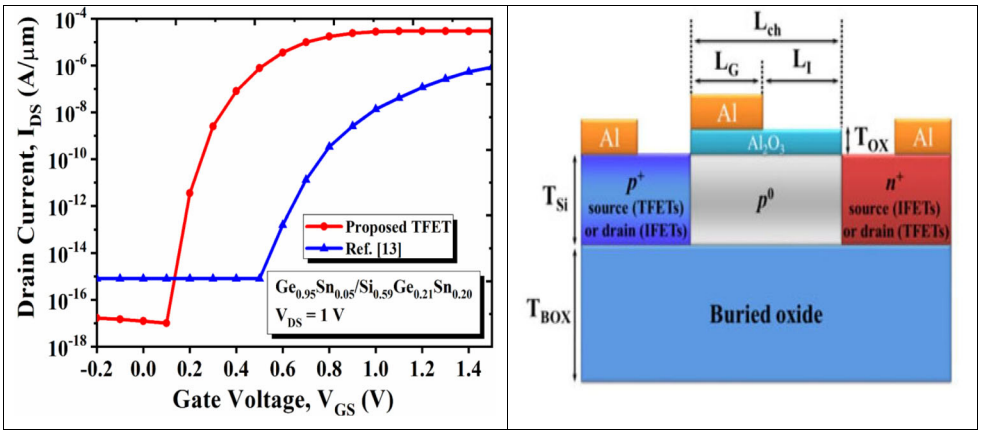


**Fig. 5** The $I_D$-$V_{GS}$ curves of the conventional TFET [13] structure and the proposed TFET with drain split. Device structure [13]

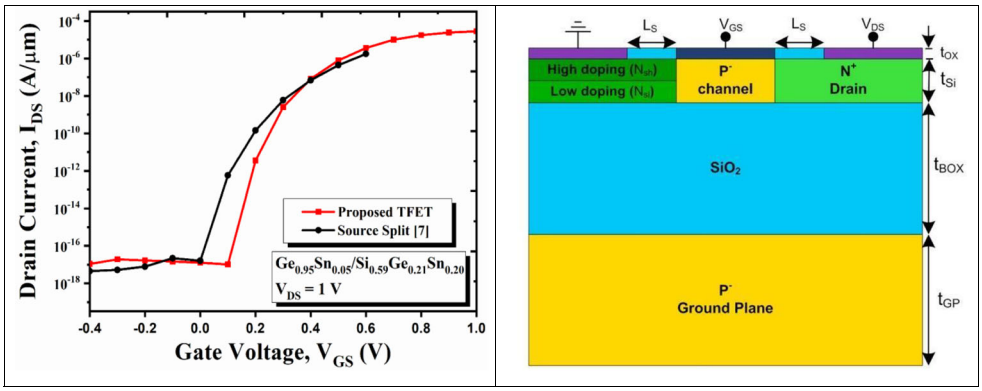


**Fig. 6** The $I_D$-$V_{GS}$ curves of source split [7] and the proposed GeSn/SiGeSn based drain split TFET. Device structure [7]

effects of high doping, bandgap narrowing (bgn) model was included due to the high level of doping used in the source region and the drain region. Also, some physical models were included such as mobility, Fermi-Dirac Statistics (FRM), Shockley Read Hall (SRH) and Auger Recombination models. The Non-Local Band to Band Tunneling (BBT.NONLOCAL) model was utilized to enable tunneling in the sideward. Further, it can be emphasized that the prime target of this research article was to establish the comparative results of presented drain doping engineering together with intensely doped Ge strip on the characteristics of the proposed structure with comparison to the conventional TFET structure.

This section includes a variation of electron-hole concentration and potential distribution at different $V_{GS}$ values, the comparison of traditional TFET structure with the introduced drain split TFET with Ge strip, the impact of changing doping concentration in the drain, varying gate oxide thickness and varying mole fraction. Also, potential distribution through the cross-section of device and contour plots comparison of the electron carrier concentration and hole carrier concentration at the different drain to source voltages.

The variation in electron-hole concentration by varying gate to source voltage ($V_{GS}$) along with drain to source voltage ($V_{DS}$) depicted in Fig. 3. At $V_{GS}$ = 0 V, the electron concentration in Fig. 3a was less across the channel-drain junction. After applying $V_{GS}$ = 1 V, the depletion width becomes very narrow due to which tunneling starts at the junction. As a result of that the electron concentration across the channel-drain junction increases that can be noticed in Fig. 3a and b. The same applies to hole concentration and can be observed in Fig. 3c and d. The above plots assist us to understand how the hole and electron carrier concentration differs over the device at various bias conditions.

Figure 4 depicts the electrical potential variation across the device by varying gate to source voltage ($V_{GS}$). Figure 4a represents the OFF state i.e. $V_{GS}$ = 0 V, the maximum potential variation was seen adjacent to the channel-drain junction. In Fig. 4b, $V_{GS}$ was increased to 1 V, due to which the tunneling phenomena take place and hence, TFET gets turned ON. The drain current in ON state begins to circulate within the structure.

Tunneling current may be changed by varying the effective bandgap value which depends upon the material. This can be understood by eq. 1. The comparison between traditional TFET [13] and the proposed GeSn/SiGeSn TFET structure shown in Fig. 5. By introducing, GeSn in the source region, the bandgap of the source region reduces, so more ON current $I_{ON}$, lesser OFF current $I_{OFF}$ can be attained. The rise in $I_{ON}$ and reduction in $I_{OFF}$ current results in higher $I_{ON}/I_{OFF}$ ratio, which reduces ambipolar behavior. Hence, the value of SS was lowered.

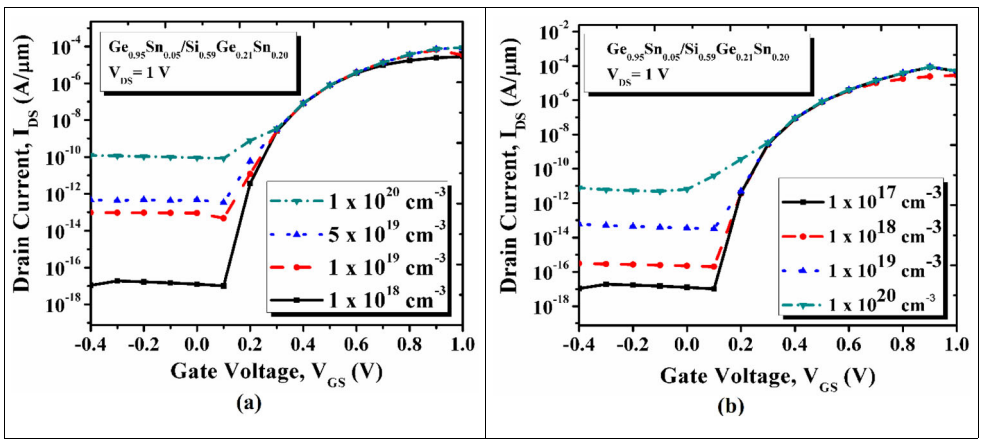


**Fig. 7** The $I_D$-$V_{GS}$ curves of GeSn/SiGeSn TFET for varying drain concentration (**a**) high doped region with concentration varying from $1x10^{18}cm^{-3}$ to $1x10^{20}cm^{-3}$by keeping low doped region fixed to $1x10^{17}cm^{-3}$ and (**b**) low doped region with concentration varying from $1x10^{17}cm^{-3}$ to $1x10^{20}cm^{-3}$by keeping high doped region fixed to $1x10^{19}cm^{-3}$

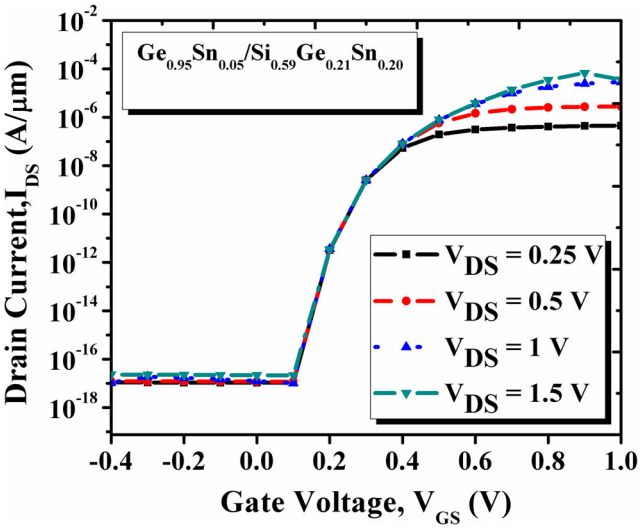


**Fig. 8** The transfer characteristics variation for the different values of $V_{DS}$

A comparison between proposed GeSn/SiGeSn based TFET and Source Split TFET [7] presented by Basu et al. is depicted in Fig. 6. TFET structures were almost the same, the only difference was that in the proposed structure drain was splitted while in the reference structure, source was splitted. Hence, a significant comparison was possible. The $V_{GS}$ voltage was varied from −0.4 V to 1 V. For the proposed TFET, a large value of ON current ($I_{ON}$) was obtained, which is possible due to a reduction in bandgap and splitting of the drain. In the source split type TFET, the magnitude of $I_{OFF}$ was almost same that of proposed TFET while $I_{ON}$ was less than that of proposed. Therefore, we can say that our proposed TFET has higher $I_{ON}/I_{OFF}$ ratio, which ascertains the fast switching application.

The consequences of varying concentration of drain-doping over the transfer characteristics of the TFET indicated in Fig. 7. The drain region was split into two doping levels, low doped region and highly doped region. With the increase in doping concentration in the highly doped drain region, there was a very slight increment in $I_{ON}$ current while there was a very large increment in $I_{OFF}$ current due to which $I_{ON}/I_{OFF}$ ratio reduces so for the highly doped region $1x10^{19}cm^{-3}$was the optimum doping level. Similarly, with an increase in the level of the doping concentration of the low-doped region, there was a very high increment in $I_{OFF}$ current while $I_{ON}$ current was almost the same, $I_{ON}/I_{OFF}$ ratio reduces. Therefore, for the low-doped drain region $1x10^{17}cm^{-3}$ was optimized doping concentration. Besides, we observed that the $I_{OFF}$ or ambipolar current rises, when there was an increment in the doping concentration.

The transfer characteristics or $I_D/V_{GS}$ curves of the proposed TFET with different values of the drain voltage, from 0.25 V to 1.5 V demonstrated in Fig. 8. It has been observed that, as the drain voltage reaches 1 V from 0.25 V, there was a continuous increase in the tunneling current keeping $I_{OFF}$ almost the same because in Tunnel FET, tunneling current depends on drain voltage along with the gate voltage. But beyond 1 V, it was observed that $I_{ON}$ increases by very less fraction (i.e. not much improvement in the $I_{ON}$) due to the adverse consequences of the Short Channel Effects (SCE's) (for example Drain Induced Barrier Lowering - DIBL, Impact ionization, pinch-off mechanism and Velocity saturation). For proposed TFET, all transfer characteristics data were studied at $V_{DS}$ = 1 V. The length of the gate region, $L_g$ as 100 nm and the thickness of the gate oxide of 20 nm were taken for the transfer characteristics ($I_D/V_{GS}$).

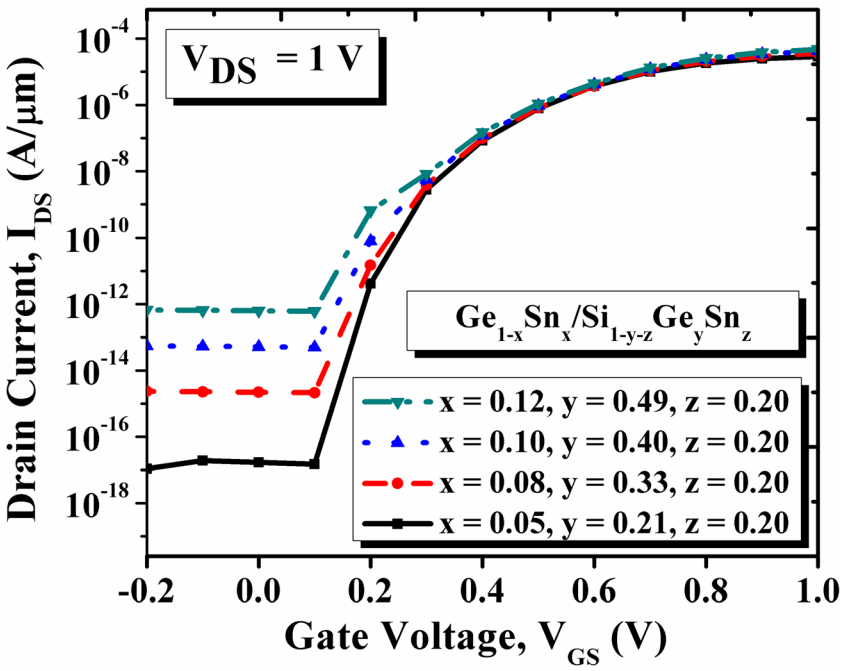


**Fig. 9** The variation of $I_D$ with $V_{GS}$ at different Sn(x) and Ge(y) concentration

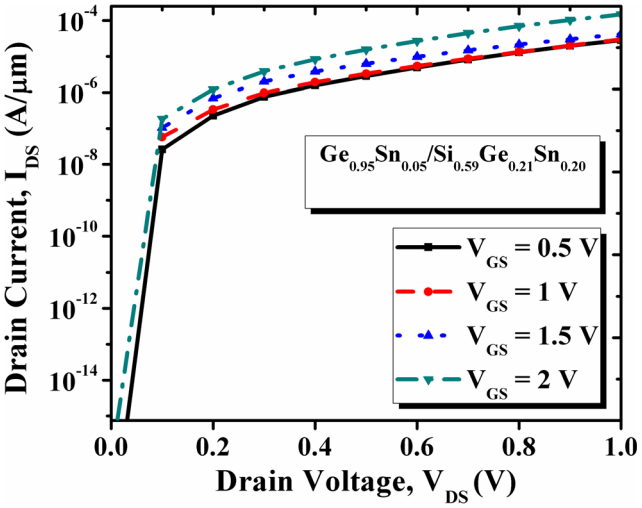


**Fig. 10** The output characteristics at the different gate to source voltages ($V_{GS}$)

The impact of different mole fraction of $Ge_{1-x}Sn_x/Si_{1-y-z}Ge_ySn_z$ on transfer characteristics ($I_D$ vs $V_{GS}$) depicted in Fig. 9. With the change in mole fraction, electrical characteristics of $Ge_{1-x}Sn_x/Si_{1-y-z}Ge_ySn_z$ based TFET varies. By increasing, the Sn concentration in GeSn and increasing Ge concentration in SiGeSn, $I_{OFF}$ current increases while $I_{ON}$ current was almost the same. Due to which, the ratio of $I_{ON}/I_{OFF}$ current reduces, so, in order to get high $I_{ON}/I_{OFF}$ ratio for proposed structure x = 0.05, y = 0.021, z = 0.20 has been considered for $Ge_{1-x}Sn_x/Si_{1-y-z}Ge_ySn_z$.

The output characteristics with the different levels of the $V_{GS}$ voltages expressed in Fig. 10. For lower gate voltage, the ON current is lowest and for higher gate voltage ON current is highest. This occurs because the tunneling barrier in the previous case was large and therefore, the charge carriers will have the less tunneling probability. However, with the applied voltage levels incremented over the gate terminal from 0.5 V to 2 V, a continuous improvement in ON current was noticed. This occurred due to the reduction in the width of the tunneling barrier, therefore, the tunneling probability of the charge carriers will improve. So, there was a continuous increase in the ON current level due to $V_{GS}$ voltage changes from 0.5 V to 2 V.

The variation in potential at (a) different insulating materials ($SiO_2$, $Si_3N_4$, Sapphire, $HfO_2$) and (b) at three different gate oxide thickness ($T_{OX}$) as 1 nm, 3 nm, 5 nm indicated in Fig. 11. Dielectric constants of the above materials are taken as $SiO_2$–3.9, $Si_3N_4$–7.5, Sapphire- 12 and $HfO_2$–22. The utmost inflection in the potential distribution can be noticed in the channel region where the tunneling phenomenon happens. It was deduced from eq. 1, the tunneling current may be improved by enhancing the value of gate oxide dielectric constant ($\varepsilon_{ox}$) and with the reduction of the thickness of the gate oxide ($T_{OX}$). The optimum characteristics can be obtained for $HfO_2$ at 1 nm oxide thickness.

The comparison of the ON current $I_{ON}$ and the OFF current $I_{OFF}$ between various established TFET devices [from reference papers] and proposed device clearly indicates the better performance.

## 5 Conclusion

With this research article, the evaluation of the use of Ge strip and the use of abrupt doping profile in the $Ge_{1-x}Sn_x/Si_{1-y-z}Ge_ySn_z$ TFET was carried out. By using $Ge_{1-x}Sn_x$ material, the effective bandgap has been reduced. This directly improves band-to-band tunneling current. The ON-state current was improved as a result of the bending of the band at the source side and the OFF-state current was decreased because of the barrier formed in the channel. The results of the proposed paper were compared with the conventional homogeneous Si TFET, SiGe-Si-SiGe heterogeneous TFET. By considering all these scenarios, the proposed TFET device delivered superior results in the relation of $I_{ON}/I_{OFF}$ ratio, which directly improves the device performance. The study includes varying various device parameters such as drain doping concentration, mole fraction(x). In the proposed structure, the

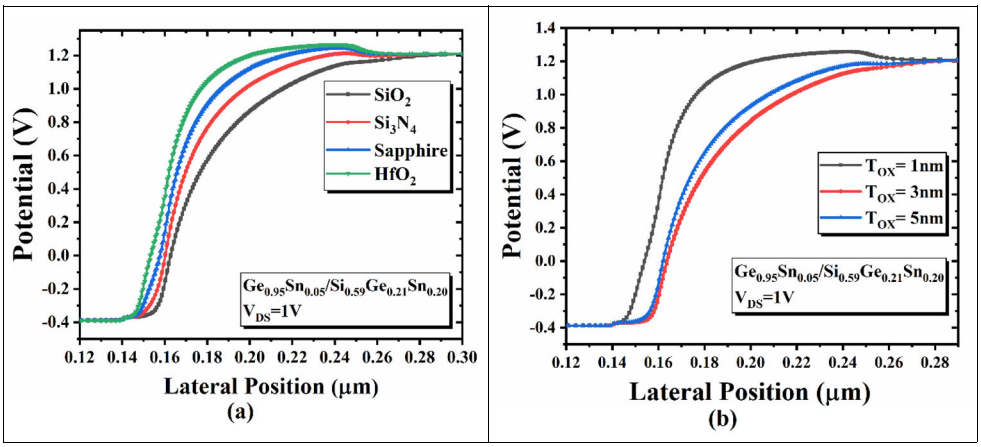


**Fig. 11** The comparison of the potential distribution curves for (**a**) insulating material and (**b**) oxide thickness

subthreshold swing attains a small value of 25.03 mV/decade accompanied by high $I_{ON}/I_{OFF}$ ratio of order around $10^{12}$ at $V_{DS}$ = 1 V. The TFET is a strong candidate to replace MOSFET because of its promising behaviour and suitable for low power application devices. Further improvement in the device characteristics can be made by using other direct bandgap materials, by varying gate length.

**Acknowledgments** The Authors would like to extend special thanks to Director, NIT Delhi and DST-Science and Engineering Research Board (DST-SERB) project, Govt. of India, (under Early Career Research Award Scheme 2017 (FILE NO. ECR/2017/000794) awarded to Rikmantra Basu) for supporting this research work.

## Compliance with Ethical Standards

**Conflict of Interest** The authors declare that they have no conflict of interest.

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