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REVIEW ARTICLE

Comparative Analysis of Nanowire Tunnel Field Effect Transistor for Biosensor Applications

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Abstract

Nanowire based devices are most important candidate for future generation application. The unique advantage of Nanowire as a channel material is one dimensional conduction, low subthreshold leakage current as well high electron mobility. Moreover Nanowire posses unique prosperities such as chemical, optical, electrical and mechanical making them suitable for sensor design. Nanowire Tunnel Field Effect Transistor (NW-TFET) has potential bio-sensor applications as ultra-low power highly sensitive sensors alternative to conventional sensors. NW-TFET can offer sharp inverse subthreshold slope (SS) leads to low leakage current. The important working mechanism is band-to-band tunnelling (BTBT) in TFET and their structures are based on gate-all-around (GAA). This paper presents, recent advancements made on process, purpose and properties of NW-TFET and comparison on various NW-TFET structures and their characteristics. Various categories include in this paper are GAA, Junctionless, hetrojunction, charge plasma, doppingless, or in combination with multigate work functions are discussed. The comparative study revealed that HT-JL-DG-NW-TFET outperforms and highly sensitive bio-sensor application and better device performance over other NW-TFET.

Keywords Nanowire-TFET · Charge plasma (CP) · Band-to-band Tunnelling (BTBT) · Gate-all-around (GAA) · Biosensor

1 Introduction

Tunnelling Field-Effect-Transistors (TFETs) emerged as a popular semiconductor device in the field of high sensitive bio-sensor based scientific research and industry for its merits over other semiconductor devices to deal with sub-threshold effects [1–4]. Corresponding, advancement in Nanowire research recognized as industry need to meet requirements of miniaturization [5–7]. Combining TFET and Nanowire structures offers optimized silicon device for biosensors [8–10]. Biosensors require high sensitivity to bio-molecules, while being tiny in size, and Nanowire TFET meets these requirements. Conventional MOSFETs (metal–oxide–semiconductor field-effect transistors) compete with TFETS with their ON-OFF current ratio and lower off current leakage [11]. But small sub-threshold swing and high ON current operation of TFET is first choice for high sensitive devices [11–14]. The low-power electronics applications, transistor with sharp slopes are fundamental for high Ion/Ioff ratios and TFETs are most energy efficient switch with inverse subthreshold slope SS < 60 mV/dec. Various device materials have been proposed to improve I_{ON}-current.

NW with hetrojunction, gate all around (GAA), junctionless, or doppingless (DL) architecture widely reported for various sensor applications [15, 16]. Furthermore ambipolar behaviour of devices as negligible I_{OFF}-currents due to charge carrier Tunnelling limits the sensor performance. In last decade, since the Nanowire based devices become first choice for scientific community working in nanotechnology based biomedical applications. Recent research reports dedicate optimization methods to implement properties of JL-TFET Nanowire structures based on gate-all-around (GAA) and band to band Tunnelling (BTBT). While, progress in performance enhancement of NW-TFET is still require stimulus to improve on its applicability to bio-sensor applications. This paper presents, recent advancements made on process, purpose and properties of Nanowire-Tunnel-Field-Effect Transistor (NW-TFET). NW-TFET review at the end of this

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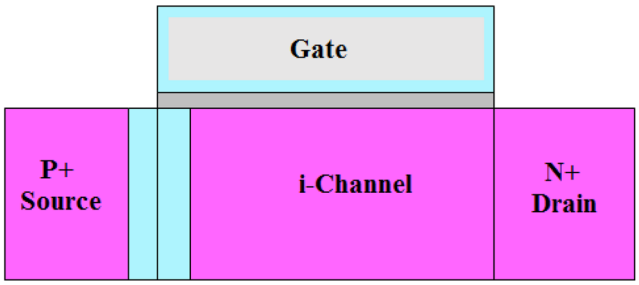

Fig. 1 Single gate TFET [7]

paper will justify need for biosensor application for highly sensitive devices in the arena of biomedical applications. Commonly illustrated Nanowire TFET can be classified in following categories:

2 Single Gate TFET

TFET and MOSFET device structure is similar, beside source and drain regions having opposite doping in TFET device structure, the band-to-band-tunnelling (BTBT) is controlled by the gate between p + or n + by means of energy band bending. While source and drain are highly doped. Figure 1 illustrates an n-type p-i-n structure TFET [17].

3 Double-Gate JL-Nanowire TFET

Nanowire-TFET devices with multiple gate incorporates more than one gate on a non-planner or 3D structure controlled by one single gate electrode.

Most common multigate devices are FinFET and GAAFET that made advancement to TFET structure for very high frequency operations. Double-gate JL-TFET is proposed and investigated by B. Ghosh and M. W. Akram (2013), designed with two isolated gates of different metal work-functions. Figure 2 shows device structure of DG-JL-TFET with

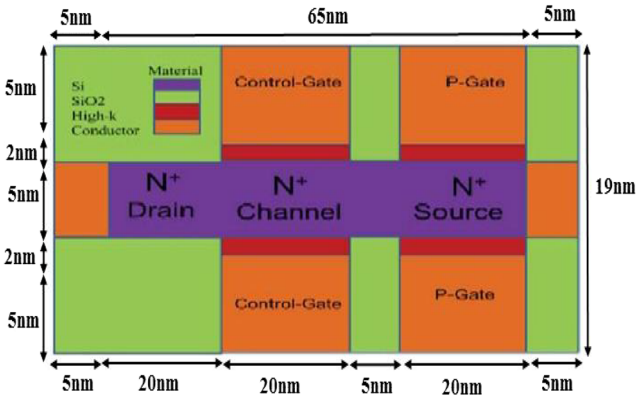

Fig. 2 Double gate JL-TFET [3]

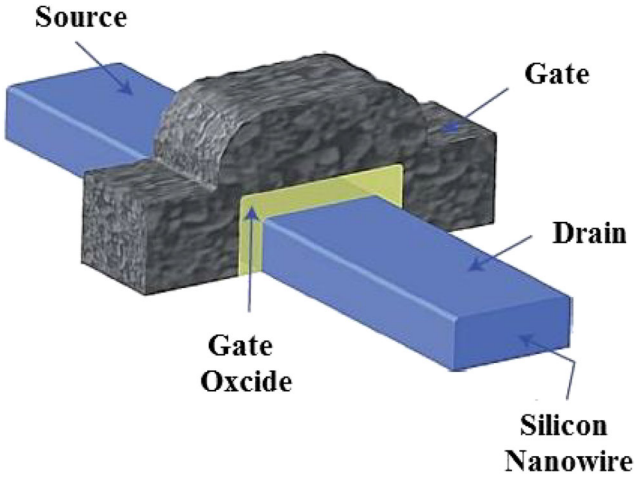

Fig. 3 N-channel Junctionless Nanowire TFET [18]

Si-channel heavily n-type-doped (1×10^{19} cm − 3) having 20-nm channel length source/drain extension length of 20 nm, silicon film thickness of 5 nm, 2-nm gate oxide thickness, and 5 nm of isolation in between Control-Gate work functions of 4.3 and, P-Gate work functions of 5.93 eV. Researcher observed high I_{ON}/I_{OFF} ratio and SS of 38 mV to 70 mV per decade for high switching operation [3].

4 Junction-Less Nanowire TFET

Majority of semiconductor devices form junctions, while a fabrication of nano devices junctions below 10 nm is difficult. Nanowire devices are being fabricated with no-junctions and dopingless structures (see Fig. 3; n-type with a concentration of 1×10^{19} cm^{-3} to p-type with a concentration of 1×10^{18} cm^{-3}) having complete CMOS operations and are fabricated with silicon materials [18].

Researchers reported these devices with near-ideal subthreshold slope, extremely low leakage currents, and less degradation of mobility with gate voltage and temperature than classical semiconductor devices.

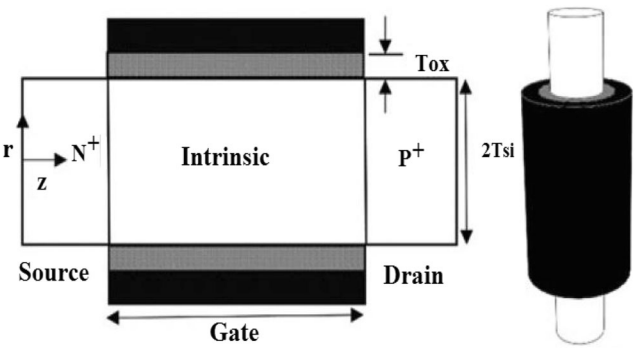

Fig. 4 Structure of GAA Nanowire TFET with p-channel [19]

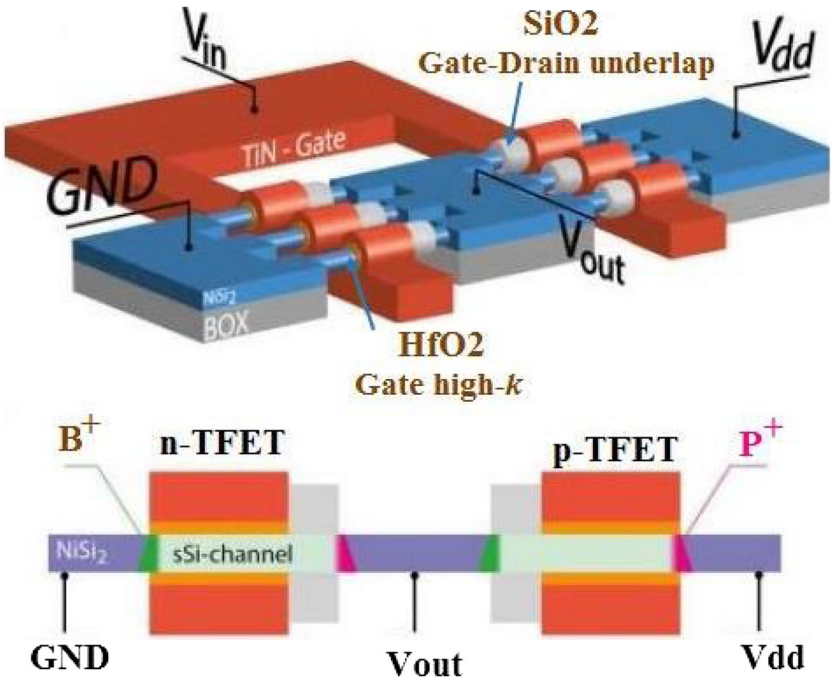

Fig. 5 Complementary Strained Si GAA NW-TFET [20]

5 Cylindrical/Gate-all-around (GAA) Nanowire TFET

GAA devices also known surrounding-gate transistor (SGT) as gate material surrounds the channel completely. Figure 4; illustrates gate-all-around Nanowire structure with p-type channel length of 50 nm, doping concentration of $10^{15}/cm^3$, and gate work-function 5.0 eV [19].

Figure 5 shows a complementary tunnelfield-effect transistor (CTFET) based on strained Silicon with gateall around nanowire structures on a single chip. This device suppress ambipolar behavior of the TFETs with a gate–drain underlap. The maximum switching with sharp transition with high noise margin levels of 40% of V_{dd} are observed [20].

6 Hetro-Gate Dielectric Nanowire TFET

Hetro-Gate-Dielectric Nanowire devices offers high speed operation due to its scalability and low leakage current. Figure 6; demonstrate Nanowire TFET structure using hetero-gate-dielectric structure introduce dip in conduction band at

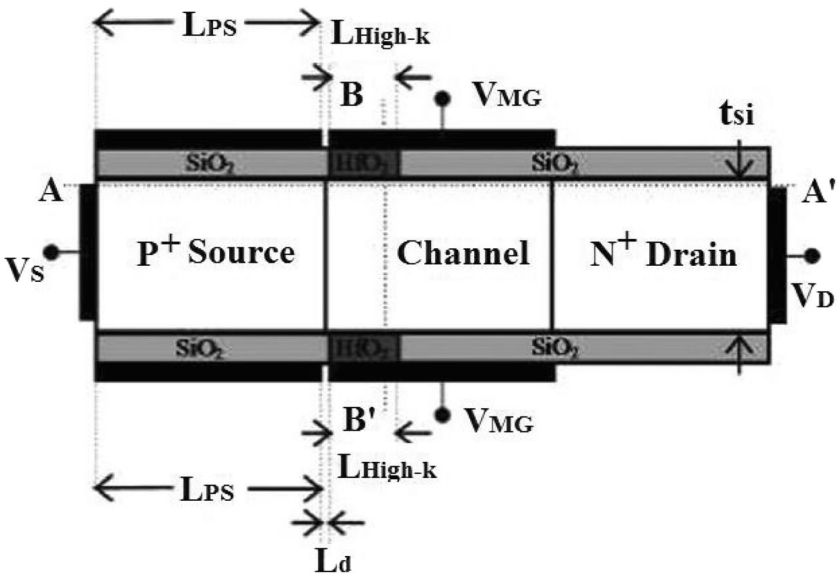

Fig. 6 Hetro gate dielectric nanowire TFET [21]

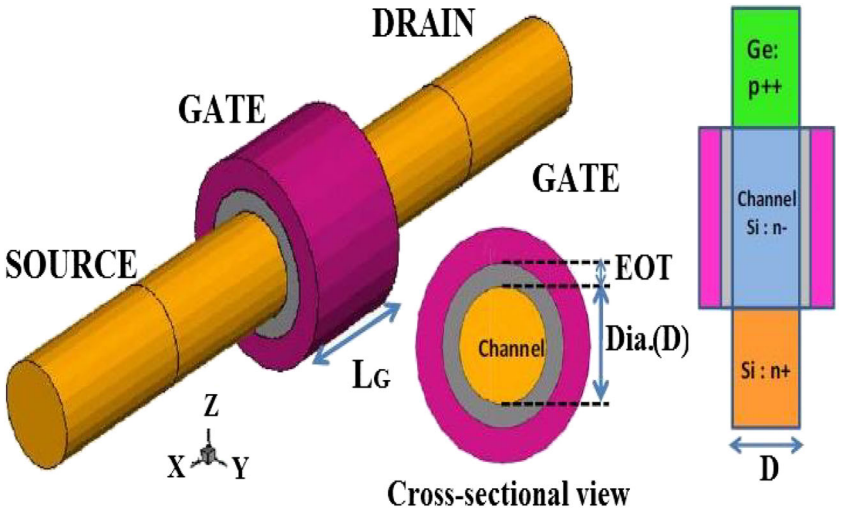

Fig. 7 Ge-Si heterojunction nanowire tunnel FET [25]

Tunnelling junction with better subthreshold swing (SS) at low drain voltages and power efficiency [21].

Ge-Si Heterojunction Nanowire TFET BTBT model considered to design three-dimensional (3D) Ge-Si heterojunction TFET having length of gate 10 nm (see Fig. 7) and also made comparison with Si TFET. The results revealed that this device performs better as compared to Si TFET. The reason for this is lower bandgap and having larger Tunnelling windows [22–24]. The BTBT generation rate is higher near source and channel junction while the peak is located near the gate dielectric [25].

7 Charge Plasma Nanowire TFET

Charge-plasma (CP) method stimulates doping charge carriers concentration of in intrinsic semiconductor. Researcher investigated dopingless, hetro gate dielectric, charge plasma based NWTFET structure (see Fig. 8) with double gate $ZrSiO_4$ and SiO_2 as two gate materials. The observed ON and OFF currents was 5.54 μA/μm, and 0.1 aA/μm respectively. Further the reported device observed negligible ambipolar current was 10^{-19}A/μm with $V_{GS} = -0.8$ V making proposed device a better candidate for low power applications [26].

The GAA vertical Nanowire TFET based CPshown in Fig. 9, represent positive interface trap charges (ITCs) made it suitable for analog applications. The reported device has same cutoff frequency at 0.8 V gate bias and having threshold voltage half of that for higher positive ITCs [27].

8 Nanowire TFET Biosensor

Various semiconductor devices have been used as sensors for biomedical applications, such as: temperature, light, gas sensors are commonly used in physiological measurement systems [28–31]. Challenge lies in high sensitivity of sensors to change in bio-molecules under observation [32–34]. NW TFET bio-sensors with high sensitivity may use to detect pathological conditions in subjects, such as early detection of cancer. Figure 10 represents gate underlap DM-JLTFET structure

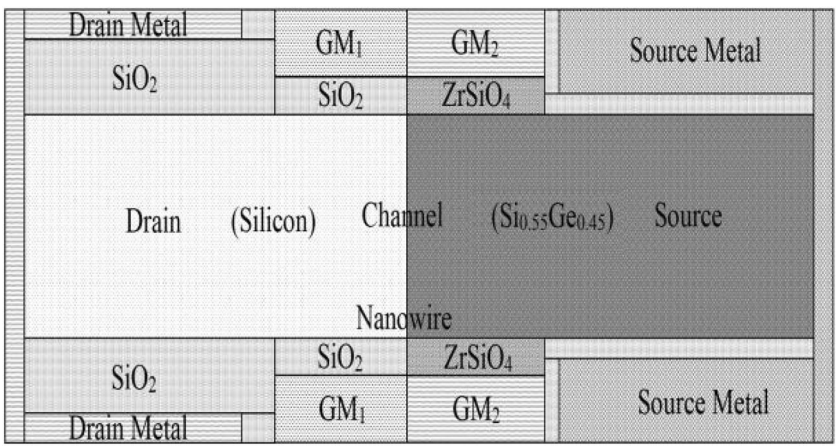

Fig. 8 Charge plasma nanowire TFET [22]

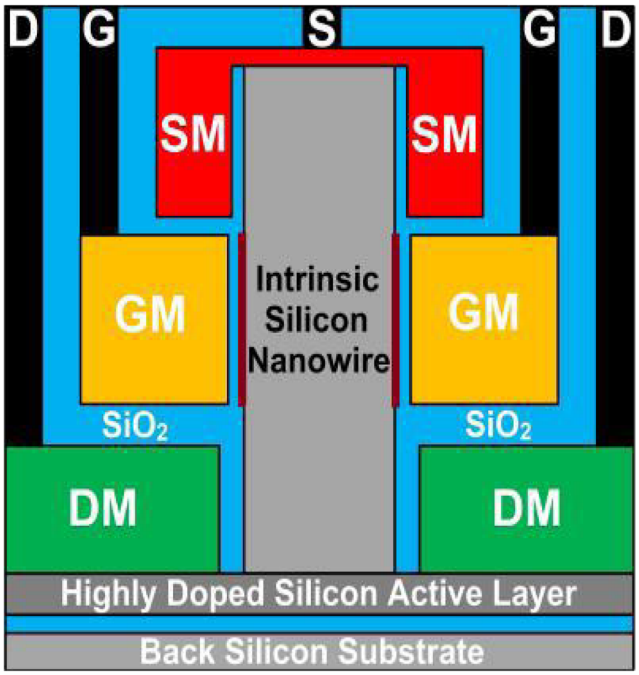

Fig. 9 Vertical nanowire TFET [27]

based on CP were proposed by Wadhwa G and Raj B (2018). Results illustrated drain current variation because of open cavity with bio-molecules ranging from 7 nm to 10 nm and V_{ds} = 0.5 V–1.5 V [35].

The I_{ON} and I_{OFF} current varies with respect to presence of positively or negatively charged bio-molecules. Indeed researcher reported that, the increase in length of the cavity leads to reduced channel length, thus band to band Tunnelling current improved in OFF state [36]. Research proposed that DM-JL-TFET structure outperforms while detecting variations of bio-molecules cavity region for higher sensitivity. Near the junction of Tunnelling by selecting properly cavity length as well as thickness, low leakage currents and high sensitivity device operation has been achieved.

Table 1 Device parameter of CP-JL-TFET

Device parameters	Values used for TCAD simulation
Total length gate/channel (L_g)	50 nm
Gate underlap length (L_{cavity})	5 nm, 7 nm and 9 nm
Gate overlap length (L_{open})	45 nm, 43 nm and 41 nm
Work function ($Ø_{m1}$ and $Ø_{m2}$)	3.9 eV and 5.93 eV
Gate underlap thickness	2.5 nm
Gate oxide thickness (t_{ox})	3 nm
Channel concentration	1.0×10^{-15} cm^{-3}

9 Results and Discussion

CP-JL-TFET with gate underlap technique has been simulated with device characteristics as enumerated in Table 1. Bio-molecules are immobilize near the In the gate underlap region. The different work function of electrodes for n^+ drain and p^+ source are implemented by hafnium metal (3.9 eV) and platinum metal (5.93 eV) respectively are used with intrinsic semiconductor material such as silicon for structure designing. The total channel is divided into underlap/cavity (R_u) as well as overlap/open (R_o) region respectively. The length of R_u region is changes from 5 nm

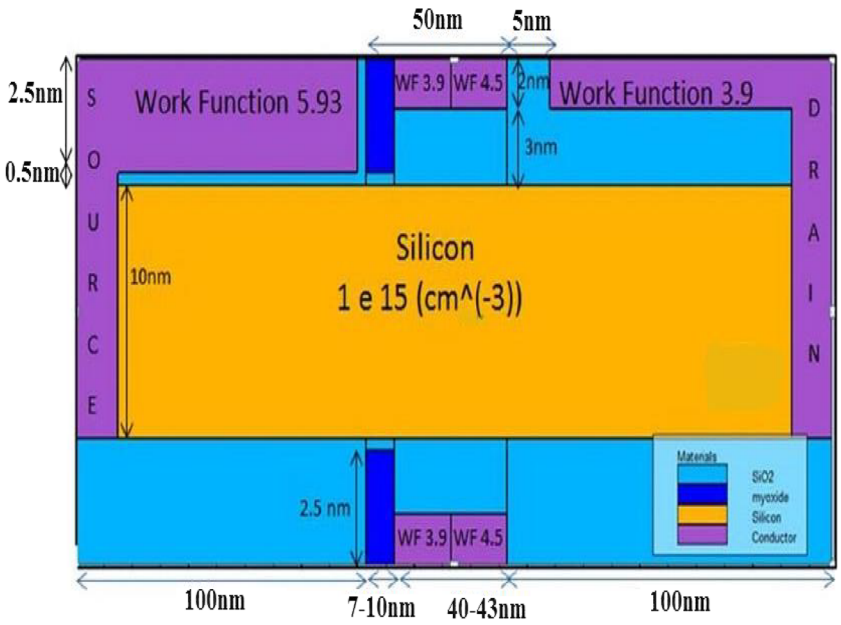

Fig. 10 DM-JL-TFET as biosensor [35]

to 9 nm and gate overlap region (L_{open}) from 41 nm to 45 nm by maintaining total channel length is equal to 50 nm. The thickness of Silicon film is maintained bye range of Debye length that is $\sqrt{[\epsilon_{si}\ \frac{V_T}{q+60.N}]}$, where as the carrier concentration of substrate (N), electronic charge (q), thermal voltage (V_T) and Silicon dielectric constant (ϵ_{si}) [34].Table 1 shows the Device parameters which is used for SILVACO TCAD simulation.

The SILVACO TCAD Tool is used for simulation of device. The field-dependent mobility and Lombardi (CVT) model, Fermi–Dirac statistics, recombination model (Shockley–Read–Hall) while band to band tunnelling (BTBT) model for calculation of generation rate.

10 Drain Current Variation Due to Impact of Cavity

Figure 11 illustrate V_gI_d characteristics for variation of length of gate underlap region ($L_{cavity)}$ from 5 nm to 9 nm and length of gate overlap (L_{open}) from 41 nm to 25 nm by with total length i.e. 50 nm at $V_{ds} = 0.5$ V. It is inferred that ON current ($I_{on)}$ is decreases as the cavity length increases.

The cavity formation increases due to increase in barrier width between valance and conduction band, which shows the low electron tunnelling. So that conduction of current is low. Moreover, due to variation in cavity length it was also noted that I_d at $V_{ds} = 1.5$ V is compliably very low as compared to $V_{ds} = 0.5$ V. Thus it can be observed that CP-JL-TFET with gate underlap technique exhibits Tunnelling principle.

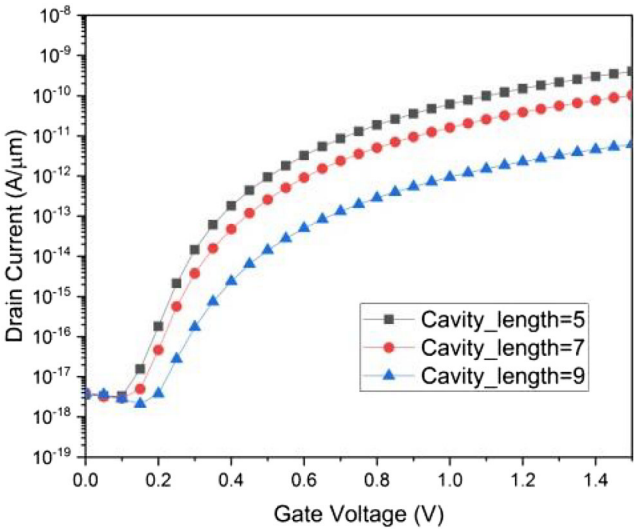

Fig. 11 Drain current variation due to impact of Cavity

11 Drain Current Variations with Dielectric Constant (K) and Bio-Molecules Charge

Because of bounding neutral bio-molecules, variation of drain current are noticed in region of open cavity as shown in Fig. 12 when $L_{cavity} = 7$ nm and $L_{open} = 43$ nm at $V_{ds} = 0.5$ V.

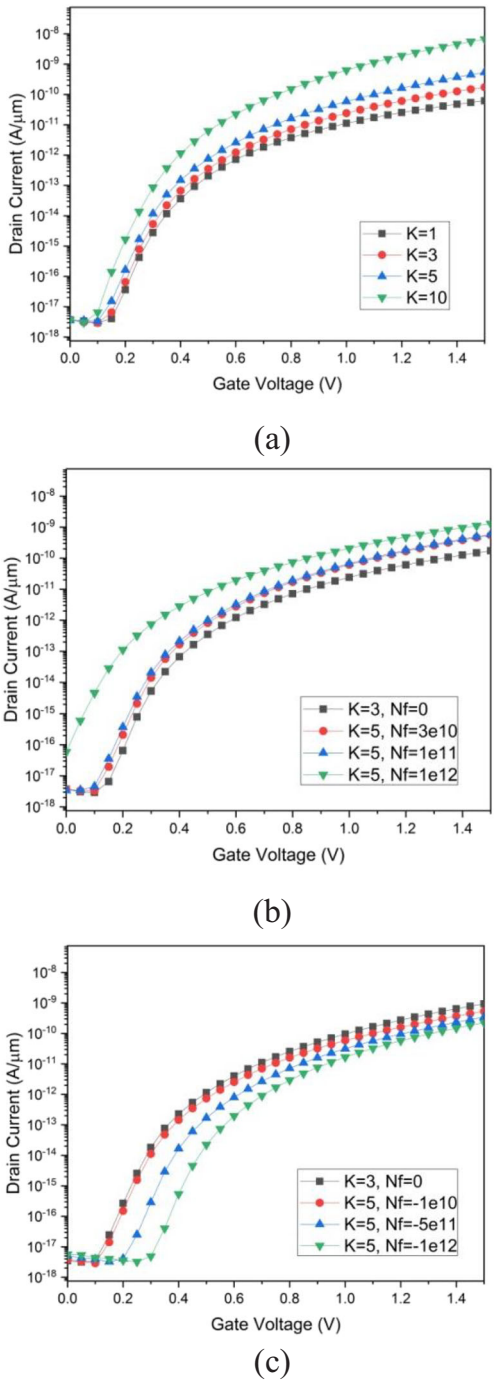

Fig. 12 Drain current variations with dielectric constant (K) and bio-molecules charges (**a**) Variation of dielectric constant at K = 1, 3, 5, 10; **b** Variation of charge densities (positive) from (0 cm^{-2} -10 cm^{-2}); **c** Variation of charge densities (negative) from (0 cm^{-2} -10 cm^{-2}) by using work function 3.9 eV (n^+ drain) and 5.93 eV (p^+ source)

Table 2 Comparative analysis of device structures for Nanowire TFET

Reference number	Device Structure	Channel Material	Gate Dielectric	I_{ON}	I_{OFF}	I_{ON}/I_{OFF} Ratio	Minimum SS	Voltage
[1]	DL-TFET	Si	SiO_2	1.1×10^{-5} A/μm	1×10^{-17} A/μm	1.1×10^{12}	100mv/dec	1 V
[3]	DG-JL-TFET	Si	TiO_2	36 μA/μm	5×10^{-14} A/μm	6×10^{8}	38mv/dec	–
[17]	N-channel Junction-Less Nanowire TFET	Si	SiO_2	1×10^{-7}A	1×10^{-15} A	1×10^{6}	60 mV/ dec	1 V
[19]	Gate-All-Around Nanowire p-TFET	Si	HfO_2	0.14 μA/μm	1 nA/μA	–	110 mV/dec	0.5 V
[20]	Hetero-gate-dielectric (HGD) JN-TFET	Si	SiO_2 and HfO_2	8.7×10^{-6} A/μm	1.29×10^{-10} A/μm	6.75×10^{4}	45 mV/dec	–
[21]	Hetro-JL-TFET	GeAs:Ge	HfO_2	2.6 mA/ μm	1.2×10^{-15} A/μm	2×10^{12}	16 mV/dec	1 V
[24]	Hetro-Gate Dielectric Nanowire TFET	Si	SiO_2	–	–	5×10^{6}	46 mV/dec	0.5 V
[25]	Charge Plasma Nanowire TFET	Si:SiGe	SiO_2 and ZiO_4	5.54 μA/μm	0.1 aA/μm	–	–	−0.8 V

It is observed form Fig. 12 (a) that ON current rises with increase in dielectric constant (K) while OFF state current remain unchanged. The reason for this is that band bending increases with the increase in dielectric constant which results in barrier width reduction and higher electron tunnelling.

Figure 12 (b) and (c) illustrate V_gI_d characteristics for charged bio-molecules inside the cavity. In the existence of positive bio-molecule ON-state current increases (as shown in Fig. 12 (b)) while decreases in the existence of negative charged bio-molecules within the cavity (as shown in Fig. 12 (c), but OFF-state current almost constant. It is occurs due to immobilization of positive/negative charged bio-molecules within cavity, leads to decrease/increase in width between valance band (source) and conduction band (channel), which shows high/low electron tunnelling. Table 2 enumerated a comparative assessment of NW-TFET device structure and its characteristics. I_{ON} and I_{OFF} currents represent basis of comparison among device structure and performance quantified using SS value represents switching speed and device sensitivity.

12 Conclusion

A detailed overview and description of various nanowire TFET devices structures for was discussed in this paper. This survey illustrates the need of improvement in I_{ON} and ambipolar characteristics of the device. The biosensor applications require high sensitivity to bio-molecule changes under consideration. Thus, selecting different device structures results in better device performance and improved SS. Comparison analysis enumerated the HT-JL-DG-NW-TFET as highly sensitive bio-sensor application and better device performance.

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