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ORIGINAL PAPER

Low Frequency Noise Analysis of Single Gate Extended Source Tunnel FET

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Abstract

This paper presents the analysis of noise in Single Gate Extended Source TFET (SG-ESTFET) considering the absence and presence of interface trap charges, when the device is subjected to scaling and variation of parameters like device gate length (L_g), extended source length and height, SiGe mole fraction (x), oxide thickness (t_{ox}), gate dielectric material, and frequency (f). Furthermore, the influence of variation of dimensionality and material parameters in presence of noise on Drain Current Noise Power Spectral Density (S_{id}) and Gate Voltage Electron Noise Power Spectral Density ($S_{vg}ee$) are studied for different trap charge conditions. Assuming Gaussian distribution of trap charges at the interface, it is perceived that the effect of noise is more as compared to the case of absence of trap charges. In reference to other FET devices, present paper reports that, the proposed SG-ESTFET device under absence of trap charges, illustrates an improved S_{id} and $S_{vg}ee$ value of 1.4×10^{-29} A^2/Hz and 5.21×10^{-16} V^2/Hz, respectively whereas under the presence of trap charges, S_{id} and $S_{vg}ee$ value are 6.6×10^{-26} A^2/Hz and 8.74×10^{-12} V^2/Hz, respectively. Moreover, this study also reports that the generation recombination (G-R) noise is mainly prevailing at low and mid-frequencies in presence of trap charges while diffusion noise is prevailing at high-frequencies. Likewise, the flicker noise is observed to be noteworthy at low and medium-frequencies in absence of trap charges.

Keywords Trap charges · TFET degradation · SRH · Bandgap narrowing · Fermi-Dirac statistic

1 Introduction

The advancement of semiconductor industry and material science has demonstrated excessive importance in most aspects of modern society. MOS transistors are assumed as brick units in ICs and conquer the central position in contemporary electronic devices. Since the introduction of miniaturization concept in 1960s (i.e. Moore's Law), the integration density has grown-up exponentially, leading to continuous and stringent efforts to comply the goal of increasing performance [1]. To keep footpath with the ITRS roadmap, we have mainly observed technological revolutions which include scaling of the device dimensions [2], addition of novel materials [3], and modernization in the fabrication process [4]. Undesirably with scaling and other developments, the main difficulty is complex short channel effects (SCEs), which leads to negotiation of long term reliability of the transistor (device) performance [5]. Above all, the fundamental understanding behind the transistor's detrimental performance is still not totally understood however the universal agreement on the explanation is defect-generation in the course of device operation over-time, predominantly in the semiconductor and oxide interface [6]. Ultimately, the modeling, simulation, and characterization of defects corrupting the device performance became a motivating and unavoidable focus of study. In recent years scientific community have proposed some unique device structures to improve the electrical performance. One such device design is Tunnel Field Effect Transistor (TFET). TFET can withstand against the SCEs in the field of low power applications [7, 8]. It basically uses interband tunnelling mechanism for current conduction, thus providing improved performance in case of leakage current, subthreshold swing, and improved switching ratio. However, TFETs main concern is low ON current [9].

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Hence, some alternative structures of TFET have been discovered by researchers to improve ON current and to make the most reliable device for commercial use.

Now this study is focused on the TCAD simulation study considering the low frequency noise component in absence and presence of trap charges at the semiconductor oxide interface by introducing a second order effect i.e. applying noise. Most of the noise in devices is due to the temporary random fluctuations of charge carrier, where the mobility of the carrier is influenced by the carrier scattering and different trapping de-trapping processes. In addition, noise is an important parameter to gain insight into material for studying defects/imperfections in various devices, and it can be considered as a technology quality metric [10, 11]. However, the impact of noise on various TFET structures is less frequently addressed in the literature. The flicker noise characterization in reference [12], analysis of low-frequency noise for different TFET structures in reference [13–16] have been reported, but a broad analysis of noise for different geometrical and material parameters has not been studied yet. In this work, various noise components are considered are such as generation recombination (G-R), flicker and diffusion noise having Gaussian profile at the oxide interface and extend the study by varying different structural and material parameters of the device. The noise analysis may help to gain insight in the charge trapping effects those results in deteriorating the transistors performance and ensuing implication in the circuit reliability.

2 Device Structure

The schematic device structure considered for present work is shown in Fig. 1. The device study for simulation is considered with 1×10^{20} cm^{-3} (Source), 1×10^{18} cm^{-3} (Drain), and 1×10^{16} cm^{-3} (Channel) doping concentrations. The device in Fig. 1 has a channel length (L_g) of 40 nm and is grown on an insulator (SiO_2) with a thickness of 20 nm. In brief, from the fabrication perspective, the total device length is 100 nm. For this first we define the device area i.e. Si layer can be patterned into mesa structures [17]. Standard oxidation process followed by the Chemical vapor deposition (CVD) method can be used for gate oxidation and gate material deposition of the structure as briefly explained in reference [4]. The material for gate and gate oxide (t_{ox}) are Aluminium (Al) and Hafnium oxide (HfO_2), respectively. Then the source and drain regions can be implanted by the optical lithography process [4]. The area of source and drain is 30 nm × 20 nm without considering the extended portion of the source. Next, for the SiGe layer, the selective area is etched away and SiGe can be deposited to fill the gap as briefly described in reference [18].

Here Sentaurus TCAD simulator has been used for simulation of the structure. Figure 2 shows the Drain Current-Voltage ($I_d - V_{gs}$) characteristics of the device which is calibrated [19] against experimentally validated SOI TFET [20]. For high doping concentration and resulting mobility, the *fermi-Dirac statistic transport* model and doping dependent mobility model have been incorporated. *Non-local BTBT* (band to band tunneling) model has been activated at each mesh point of the tunneling region to consider the generation of carriers and the basic operation of TFET. *Bandgap narrowing* model is enabled to reduce the semiconductor bandgap. *Shockley-Read-Hall (SRH)* recombination model is used for the recombination of carriers [21]. Noise model of *McWhorter's* (free carrier fluctuation) [22] and *Hooge's* (mobility fluctuation) [23, 24] are used for the low-frequency investigation. For the presence of trap charges Gaussian distribution profile is considered at different semiconductor-insulator interfaces, such as Si-HfO_2 and Si-SiO_2 as shown in Fig. 1 to the consider the practical device effects [25]. Different energies for the trap charge distribution is 0 eV and 0.1 eV, respectively.

3 Analysis and Discussion

This section presents the detailed noise analysis of SG-ESTFET considering Diffusion noise, Generation-Recombination (G-R) noise, and Flicker noise for various trap

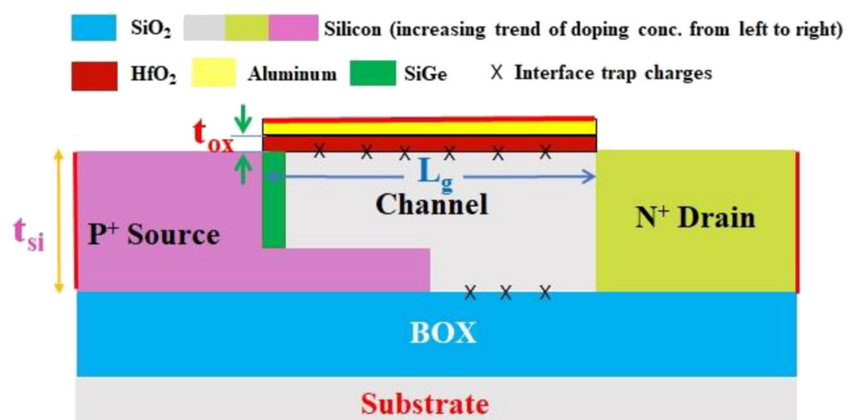

Fig. 1 Schematic structure of Single Gate Extended Source TFET (SG-ESTFET) with interface trap charges

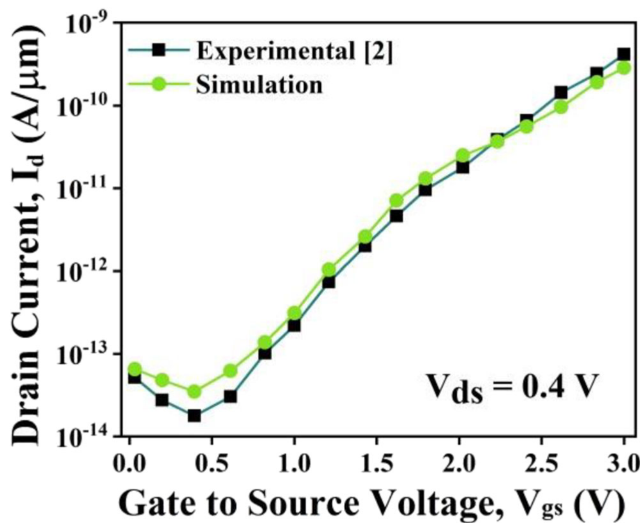

Fig. 2 Calibration of $I_d - V_{gs}$ characteristics for SG-ESTFET

charge conditions across the silicon-insulator interfaces (see Fig. 1). Analysis of drain current (S_{id}) and electron gate voltage noise power spectral densities (S_{vg}ee) as a function of frequency for variation of structural and material parameters have been systematically presented.

To understand the device operation, the variation of noise power spectral densities for SG-ESTFET, S_{id} and S_{vg}ee are plotted as a function of gate to source voltage (V_{gs}) for the constant frequency of 10 MHz and at a temperature of 300 K. As illustrated in Fig. 3a it can be observed that S_{id} increases with an increase in V_{gs} which is possibly due to the direct proportionality between S_{id} and I_d as can be seen from Eq. 1. Further, it can be observed that for higher V_{gs}, S_{id} shows a decreasing trend for both the presence and absence of trap charges. It is mainly attributed to the uneven band to band generation rate of the device as shown in Fig. 3c, which further affects the device electric field [26]. However, sources for generation of S_{id} and S_{vg}ee are different; in case of trap charges these charges have their dominance whereas in case of absence of trap charges the scattering of carriers is largely responsible [23]. Various comparative results illustrated in Fig. 3a and c indicates that at 0.2 V S_{id} starts increasing and attains it's a peak value at 0.6 V and thereafter S_{id} decreases. Figure 3b shows the S_{vg}ee of SG-ESTFET as a function of V_{gs} at a frequency of 10 MHz and at a temperature of 300 K, which is similar to the case of S_{id} of the device, as mentioned in [27]. In addition, the presence of trap charges at the interface causes an increase in S_{id} and S_{vg}ee. This is due to the presence of interface trap charges, which cause fluctuations among the carriers at the channel and affect the trapping and de-trapping process [28].

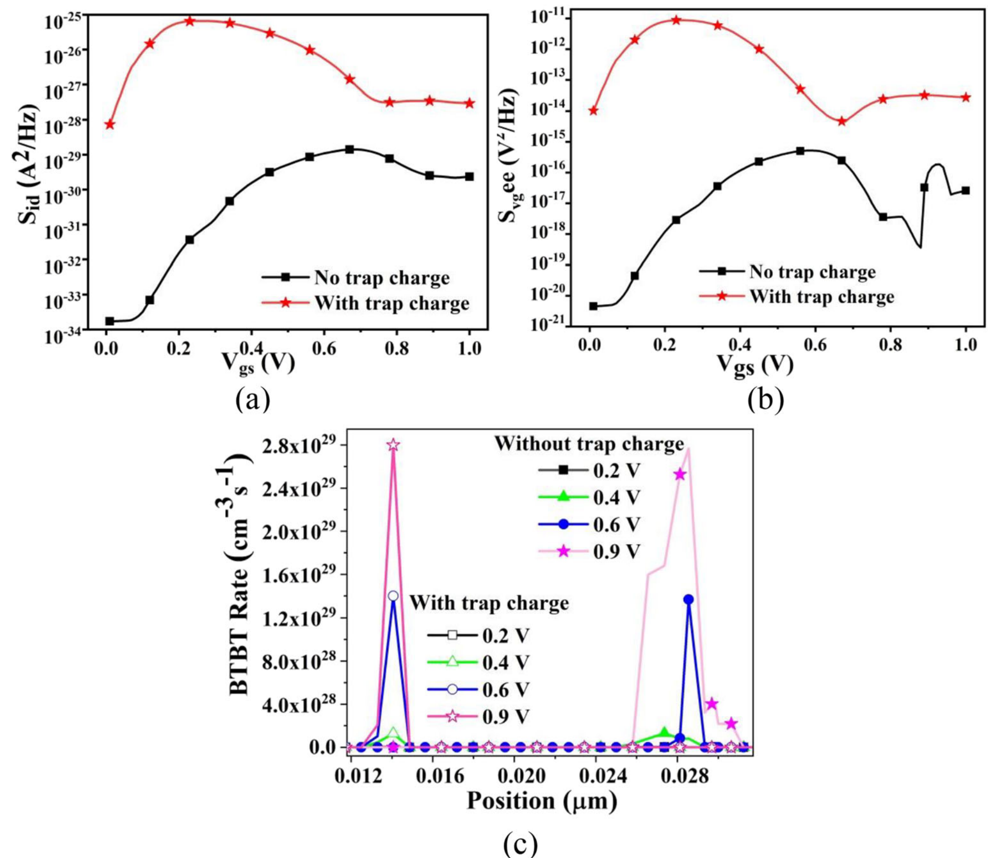

Fig. 3 Plot of (**a**) S_{id}vs. V_{gs}, (**b**) S_{vg}ee vs. V_{gs}, (**c**) Band to band generation rate at different V_{gs} for presence and absence of trap charges

A mathematical relation to express the relationship of trap charges on S_{id} and $S_{vg}ee$ is expressed in Eq. 1 which in brief correlated that, the introduction of trap charges increases S_{id} and similarly, $S_{vg}ee$ of the device. The S_{id} in terms of trap charges can be expressed as [29]:

$$S_{id} = I^2 \frac{N_{trap}}{N^2} \frac{\tau}{1 + (2\pi f \tau)^2} \quad (1)$$

where I is the current, N is the number of carriers, τ is the time constant of transition, f is the frequency, and N_{trap} is the number of traps, where $N_{trap} = N_{filled_trap} + N_{empty_trap}$.

Table 1 compares the peak value of current and voltage noise PSD of SG-ESTFET and other reported TFET devices. It can be observed that SGTFET is found to be less noisy then other reported TFET devices.

3.1 Effect on S_{id} and $S_{vg}ee$ Due to Gate Length Variation (L_g)

Figure 4a and b show the variation of S_{id} and $S_{vg}ee$ as a function of the V_{gs} at 10 MHz for various gate lengths (i.e. 20 nm, 40 nm, 60 nm, and 80 nm) considering the presence and absence of trap charges. From the Fig. 4a and b, it can be highlighted that with the scaling of gate length there is an increasing trend on S_{id} and $S_{vg}ee$, which is in consequence of the increase in OFF state and ambipolar current of the device structure [32]. In addition, a general expression for PSD is given as [33].

$$S_{id} = I_d^2 \frac{q\alpha_H}{wL_g Qf} \quad (2)$$

where, α_H is the Hooge's parameter and is equal to 10^{-8} for silicon, $N = \frac{wL_gQ}{q}$ is the number of carriers in the channel. From Eq. 2 it is apparent that the PSD varies inversely with gate length (L_g) which holds true for both number and mobility fluctuations of noise.

From Fig. 4a it can be noticed that when trap charges are present at the semiconductor-insulator interface the value of S_{id} increases significantly. The presence of trap charges affects the junction electric field by trapping and de-trapping processes, which is evident from the change in drain current in the $I_d - V_{gs}$ plot of Fig. 4c. It is found that a peak in S_{id} appears near 0.7 V and 0.2 V in the case of absence and presence of trap charges, respectively. This is due to the non-monotonic change in the electric field of the device for different cases of trap charges. Similarly, the introduction of trap charges increases the $S_{vg}ee$ of the device and for the presence and absence of trap charges $S_{vg}ee$ encounters peaks very similar to the plot of S_{id} [30].

3.2 Effect on S_{id} and $S_{vg}ee$ Due to Extended Source Height and Length

The variation of S_{id} and $S_{vg}ee$ with V_{gs} for presence and absence of trap charges when extended source height (6 nm, 8 nm, 10 nm, and 12 nm) is varied is shown in Fig. 5a and b. It can be observed that S_{id} increases with the increase in extended source height for both the presence and absence of trap charges. This is due to the increase in drain current with the increase in extended source height, as presented in Fig. 5c. In addition, the peak value of S_{id} and $S_{vg}ee$ can be observed at different gate voltages for both trapping and de-trapping cases, which is due to the non-monotonic BTBT generation rate. For the case of presence of trap charges, the S_{id} variation is almost negligible near V_{gs}=1 V, this is attributed to the fact that at higher values of V_{gs}, the high e-density and the presence of extra trap charges can screen off the effect of extended source height. From Fig. 5b it can be portrayed that, $S_{vg}ee$ varies in a similar way as S_{id}, as a result of the direct dependency of $S_{vg}ee$ on S_{id}.

The analysis of S_{id} and $S_{vg}ee$ for various extended source lengths (16 nm, 18 nm, 20 nm, and 22 nm) in the presence and absence of trap charges is plotted in Fig. 6a and b. It is observed that S_{id} and $S_{vg}ee$ of the device increase significantly with the increase in extended source length which is due to the nearness of source and drain depletion regions inherent for nanoscale FET devices. Likewise, the presence of trap charges increases the values of S_{id} and $S_{vg}ee$ and it is important to mention that the same trend is preserved as in the case of variation of absence of trap charges.

3.3 Effect on S_{id} and $S_{vg}ee$ Due to the Variation of SiGe Mole Fraction

The response of S_{id} and $S_{vg}ee$ with the variation of SiGe mole fraction (x = 0.3, 0.4, 0.5, 0.6) in the presence and absence of

Table 1 Current and voltage noise PSD comparisons for various TFET devices

Devices Structure	Without trap charge		With trap charge	
	S_{id} (A^2/Hz)	$S_{vg}ee$ (V^2/Hz)	S_{id} (A^2/Hz)	$S_{vg}ee$ (V^2/Hz)
SG-ESTFET [This work]	1.40×10^{-29}	5.21×10^{-16}	6.6×10^{-26}	8.74×10^{-12}
CG-TFET [26]	$\sim 10^{-12}$	$\sim 10^{-10}$	$\sim 10^{-12}$	$\sim 10^{-10}$
SELBOX-TFET [30]	–	–	$\sim 10^{-19}$	$\sim 10^{-7}$
Heterojunction SOI TFET [31]	–	–	$\sim 10^{-31}$	$\sim 10^{-14}$

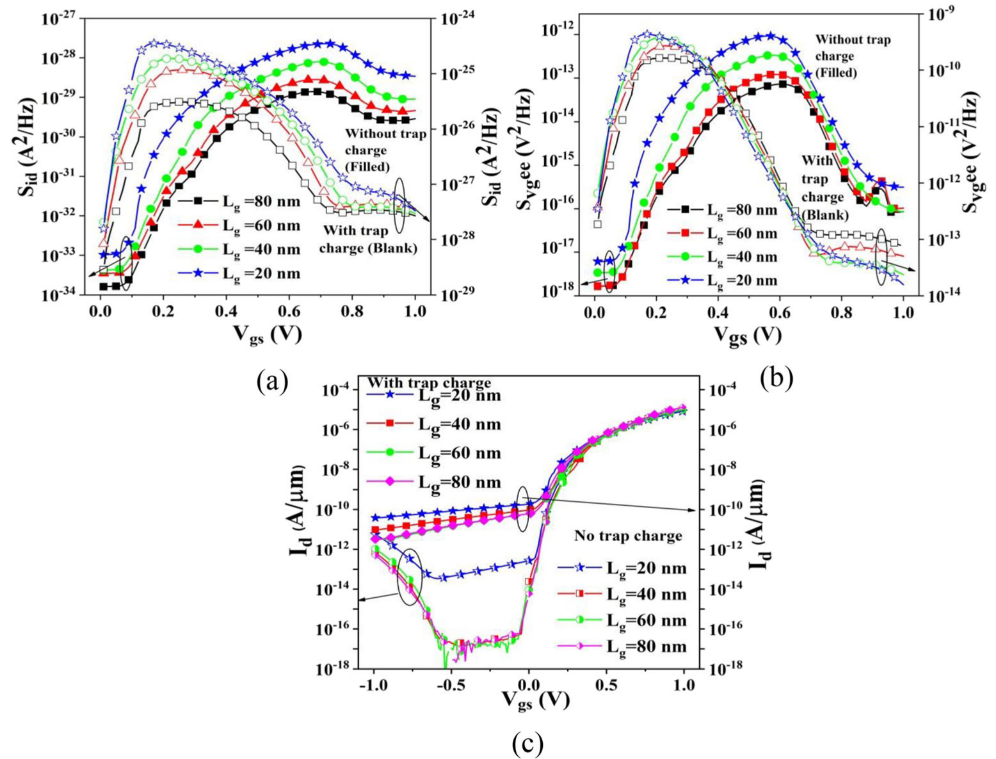

Fig. 4 Plot for various gate lengths (L_g = 20 nm, 40 nm, 60 nm, and 80 nm) in the presence and absence of trap charges for (**a**) S_{id} vs. V_{gs}, (**b**) $S_{vg}ee$ vs. V_{gs}, (**c**) I_d − V_{gs} characteristics

trap charges is presented in Fig. 7a and b. Figure 7a and b illustrate that S_{id} and $S_{vg}ee$ increases with the increase of mole fraction, well in accordance with the relation $(\Delta E_g)_{SiGe} = 0.467x$ [34], where, ΔE_g is the change (decrease) in band gap of SiGe and x represents germanium mole fraction. It is observed that as mole fraction increases band gap decreases as a result S_{id} and $S_{vg}ee$ increases. Therefore, tunnelling probability increases which lead to higher ON current for higher

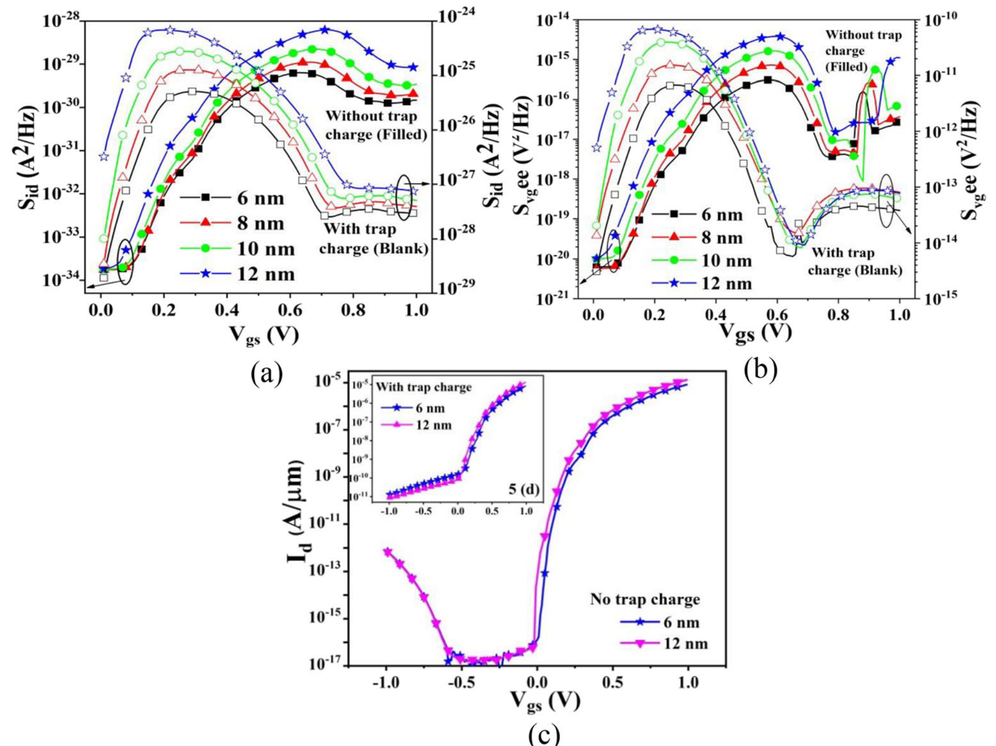

Fig. 5 Plot for various extended source height (6 nm, 8 nm, 10 nm, 12 nm) in the presence and absence of trap charges for (**a**) S_{id} vs. V_{gs}, (**b**) $S_{vg}ee$ vs. V_{gs}. (**c**, **d**) I_d − V_{gs} characteristics

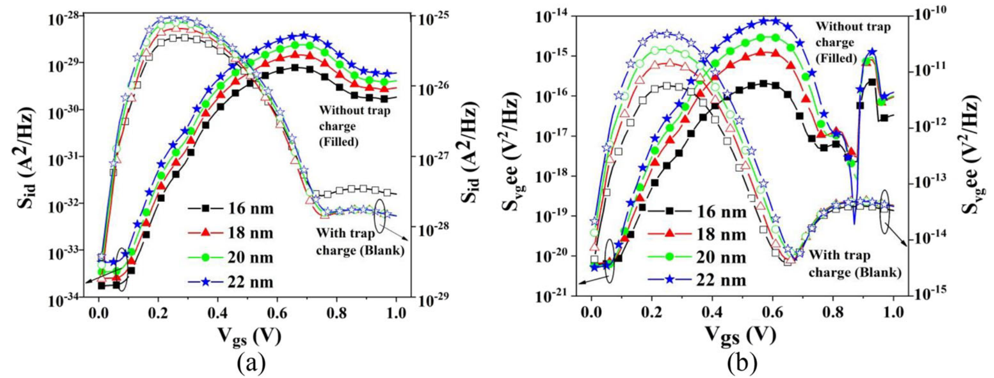

Fig. 6 Plot for various extended source lengths (i.e. 16 nm, 18 nm, 20 nm and 22 nm) in the presence and absence of trap charges for (**a**) S_{id}vs. V_{gs}, (**b**) S_{vg}ee vs. V_{gs}

mole fraction as evident from Fig. 7c. In addition, the presence of Gaussian trap charges increases the S_{id} and S_{vg}ee due to the enhancement in the device electric field.

3.4 Effect on S_{id} and S_{vg}ee Due to the Variation of Oxide Thickness (t_{ox})

Figure 8a and b report the variation of S_{id} and S_{vg}ee with the variation of oxide thickness (t_{ox} = 0.5 nm, 1 nm, 1.5 nm and 2 nm) in the presence and absence of trap charges. It is apparent that with the decrease in oxide body thickness S_{id} and S_{vg}ee of the device increases. It is because the decrease in oxide thickness results in increase of the coupling of the gate with the semiconductor surface as a result steeper tunneling profile at the source-channel junction is observed. This leads to an escalation of the leakage current as can be seen from Fig. 8c.The presence of Gaussian trap charges increases the values of S_{id} and S_{vg}ee of the device, but variation due to oxide thickness is small as compared to the case of absence of trap charges.

3.5 Effect on S_{id} and $S_{vg}ee$ Due to the Variation in Gate Dielectric Material

Now, considering the presence and absence of trap charges the variation of S_{id} and S_{vg}ee against V_{gs} for the number of gate dielectric materials is illustrated in Fig. 9a and b. The gate dielectric materials considered include Hafnium oxide ($_r$=22), Aluminum oxide ($_r$=10), and Silicon dioxide ($_r$=3.5). Figure 9a and b depicts that, S_{id} and S_{vg}ee increase

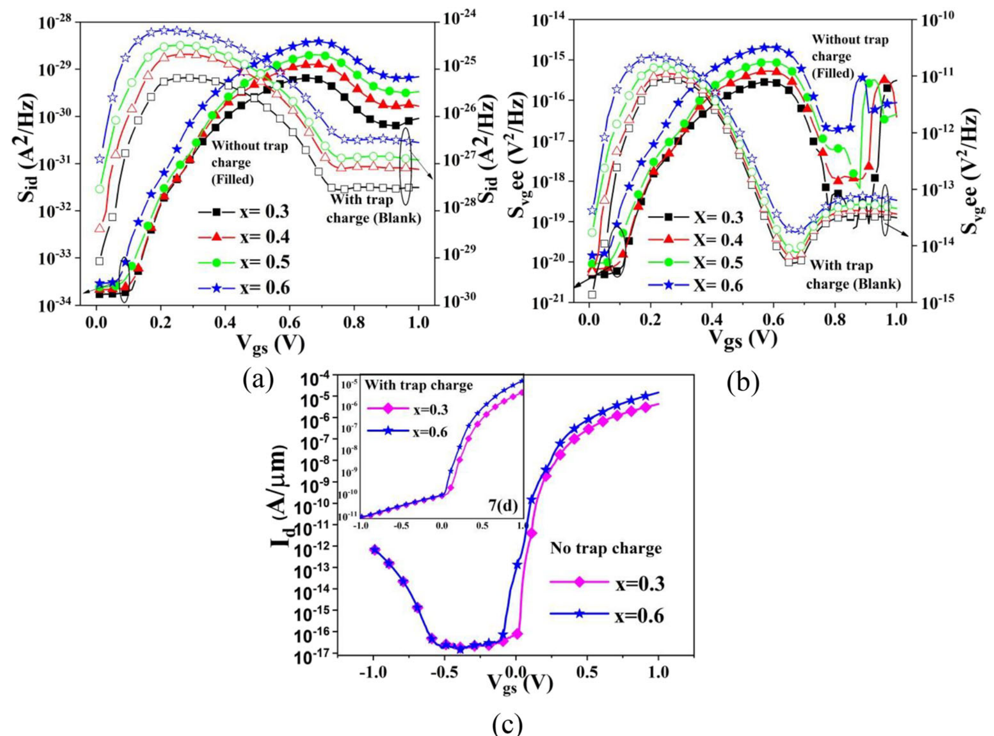

Fig. 7 Plot for various mole fractions (x =0.3, 0.4, 0.5, 0.6) in the presence and absence of trap charges for (**a**) S_{id} vs. V_{gs}, (**b**) S_{vg}ee vs. V_{gs} (**c**, **d**) I_d – V_{gs}characteristics

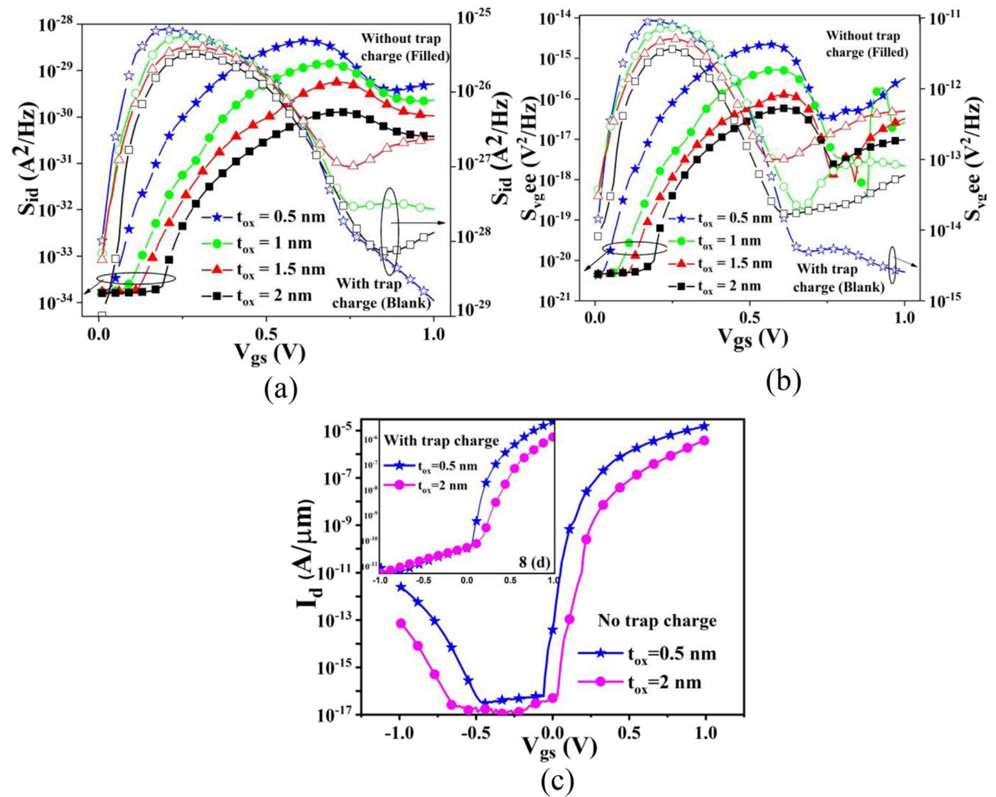

Fig. 8 Plot for various oxide thickness (t_{ox} = 0.5 nm, 1 nm, 1.5 nm, 2 nm) in the presence and absence of trap charges for (**a**) S_{id} vs. V_{gs}, (**b**) $S_{vg}ee$ vs. V_{gs} (**c**, **d**) I_d − V_{gs} characteristics

with an increase in the value of the dielectric constant of the gate oxide layer. It is widely reported that, in TFET due to an increase in dielectric constant a better electrostatic coupling can be achieved between the channel surface and the gate, which further helps to decrease the barrier width. This directly affects the drain current (I_d) as evident in Fig. 9c and

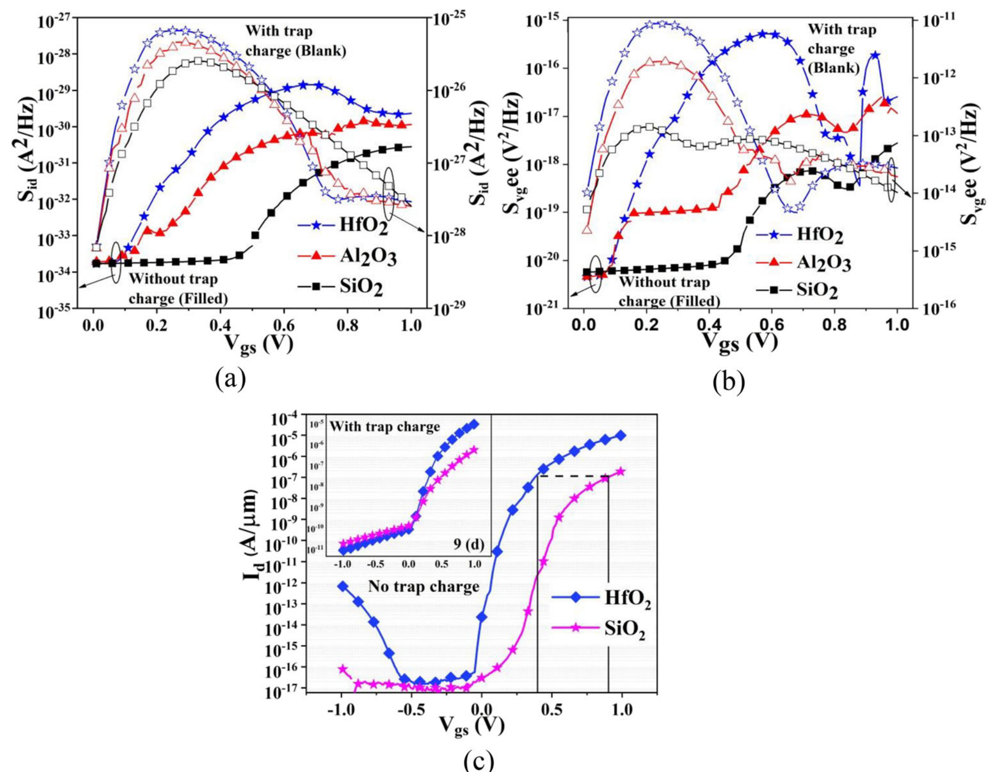

Fig. 9 Plot for various gate dielectric material (i.e. HfO_2, Al_2O_3, SiO_2) in the presence and absence of trap charges for (**a**) S_{id} vs.V_{gs}, (**b**) $S_{vg}ee$ vs. V_{gs} (**c**, **d**) I_d − V_{gs} characteristics

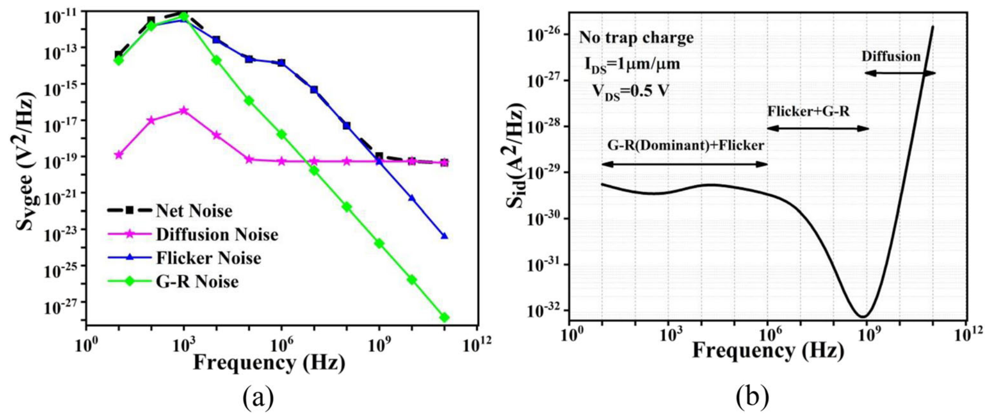

Fig. 10 Plot of (**a**) gate voltage electron noise PSD ($S_{vg}ee$) vs. frequency, (**b**) drain current noise PSD (S_{id}) vs. frequency in absence of trap charges

consequently noise power spectral densities are also transformed. In addition, high-*k* dielectrics are more prone to mobility fluctuations that arise due to the scattering of carriers. The presence of trap charges increases the S_{id} and $S_{vg}ee$ values due to the introduction of more fluctuations. Next, the variation of S_{id} due to the change in dielectric constant is less in the presence of trap charges as compared to the case of absence of trap charges which can be explained from the drain current plot of Fig. 9c. In addition, various peaks of S_{id} and $S_{vg}ee$ can be observed at different gate voltages because of the fact that material with high dielectric constant reaches a particular drain current at lower V_{gs} as compared to the case of low dielectric constant as marked in Fig. 9c leading to different BTBT generation rate.

3.6 Effect on S_{id} and $S_{vg}ee$ Due to Variation in Frequency (f)

The variation of S_{id} and $S_{vg}ee$ in the absence of trap charges for a range of frequencies between 1 MHz to 100GHz is presented in Fig. 10. It can be perceived that at lower frequencies, the effect of both generation recombination noise (G-R) and flicker noise dominates over the diffusion noise. As frequency increases the effect of flicker noise dominates over G-R noise with 1/f trend. Usually, the flicker noise is formed from the superposition of G-R noise which arises due to the mobility fluctuations. The flicker noise in TFET is given by [21].

$$S_{id} = \left(\frac{2}{F} + \frac{B}{F^2}\right) \frac{q^2 I_d^2 N_t(E_{FN})}{\varepsilon_{ox}^2 W L_g' \alpha f^\gamma} \tag{3}$$

where F is the electric field, B is a constant, $N_t(E_{FN})$ is the interface trap charge concentration, I_d is the drain current, α is the attenuation factor, f is the frequency, γ is the factor that governs the dependency of S_{id} on frequency, ε_{ox} is the dielectric constant, WL_g' are gate width and effective gate length, respectively. Next, on incrementing the frequencies we observed that both flicker and G-R noise shrinks; it is well in accordance with Eq. 3 which highlights the inverse relationship of noise with frequency. Now furthermore, at very high frequencies (above GHz range) the effect of diffusion noise dominates over all other existing noise sources which are the result of diffusion current of the device.

Figure 11 reports the variation of S_{id} and $S_{vg}ee$ of the device in the presence of Gaussian trap charges for a range of frequencies between 1 MHz to 100GHz. It is noted that the peak values of S_{id} and $S_{vg}ee$ of the device are more when

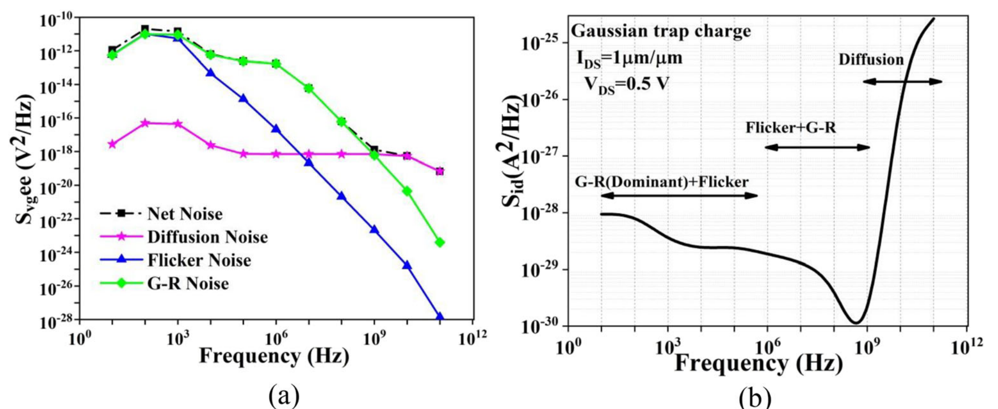

Fig. 11 Plot of (**a**) gate voltage electron noise PSD ($S_{vg}ee$) vs. frequency, (**b**) drain current noise PSD (S_{id}) vs. frequency in presence of trap charges

compared to the case of absence of trap charges. The presence of trap charges increases the effect of G-R noise, which causes dominant number fluctuations over mobility fluctuations [29]. This is due to the presence of trap charges near the Fermi level within a range of kT/q. In addition, G-R noise also originates from Shockley–Read–Hall based defect assisted carrier fluctuation process [13, 28]. Hence, the 1/f trend in Fig. 11b appears for a very small duration of the frequency range as compared to Fig. 10b. It can be portrayed that in the absence and presence of trap charges the mobility fluctuations and number fluctuations are dominant respectively.

4 Conclusion

In this paper, the systematic analysis of noise considering the effect of trap charges at various Si-Insulator interfaces is investigated for a Single Gate Extended Source Tunnel FET (SG-ESTFET). The drain current noise power spectral density (S_{id}) and gate voltage electron noise power spectral density (S_{vg}ee) are calculated and discussed for various structural and material parameters. In brief, it is observed that the values of S_{id} and S_{vg}ee are larger in the presence of trap charges as compared to their absence. However, in the presence of trap charges the variation of S_{id} and S_{vg}ee is less with the change in device geometrical and material parameters. From this study, it can be concluded that the effect of flicker noise is smaller as compared to G-R noise for the presence of same trap charges at various interfaces leading to dominant number fluctuations. Furthermore, the key finding of the present study is that the overall noise behavior of SG-ESTFET is not only dependent on bias conditions but also on various structural and material parameters, as a result making the device more suitable for low noise applications. Finally, SG-ESTFET can be marked as less noisy as compared to other devices and this study helped in gaining some insight towards the charge trapping effects which results in deteriorating the transistors performance and ensuing implication in the circuit reliability.

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