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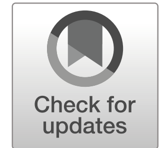

2-D Analytical Model for Electrical Characteristics of Dual Metal Heterogeneous Gate Dielectric Double-Gate TFETs with Localized Interface Charges

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Abstract
In this paper, a 2-D analytical model for electrical characteristics such as surface potential, drain current, and threshold voltage of dual metal (DM) heterogeneous gate dielectric (HGD) double-gate (DG) tunnel field-effect transistors (TFETs) with localized interface charges have been investigated. The surface potential model has been used to derive a compact model for the electric field by including the effects of the localized charges near the source/channel junction, mobile charges in channel region and the charges in the depletion regions formed at source/channel and drain/channel junctions. The band-to-band tunneling (BTBT) generation rate has been developed by considering t
he effect of the electric fields at both the source/channel and drain/channel junctions. The drain current has then been derived for all gate bias (i.e. ambipolar to forward gate bias) by using the tangent line approximation method. Finally, the threshold voltage model has been developed by using the concept of shortest tunneling path of DM-HGD DG-TFET under study. The impact of localized interface charges on the drain current and threshold voltage by varying the device dimensions are also investigated. The validity of our model results are verified by numerical simulation results obtained from 2-D device simulator ATLAS™ .

Keywords Band-to-band tunneling · Tangent line approximation method · Heterogeneous gate dielectric · Tunnel field-effect transistors · Localized interface charges;

1 Introduction

The tunnel field-effect transistors (TFETs) have been extensively in recent times due to their extremely low OFF current and low subthreshold swing even below the Boltzmann limit of 60mV/dec in conventional MOS devices [1–4]. However, the poor drain current and its dependence on the polarity of the gate bias voltage, commonly known as ambipolarity effect, are the major drawbacks of the TFETs[5, 6]. Further, the presence of localized interface donor/acceptor trap charges (i.e., positive/negative localized charges) near the source side due to high transverse electric field at the source/channel junction also affect the performance of the TFETs [7–9]. Moreover, the depletion regions formed at the source/channel and drain/channel junctions also affect the drain current of the TFETs [10]. In view of the above, the modeling of electrical characteristics of the TFETs by taking all the charges (i.e. localized charges, mobile charges and charges in the depletion regions) into consideration is very important for the performance optimization of the TFETs.

A number of theoretical investigations [11–13] have been reported on the modeling drain current of different TFET structures obtained by exploring the gate-dielectric engineering [14, 15] and work function engineering [16] and combining of both engineering [13]. Wang et al. [11] have modeled the drain current of hetero gate dielectric (HGD) DG TFETs with a source pocket. Upasana et al. [12] have reported the modeling of the surface potential and threshold voltage ofDM hetero dielectric DG TFET structures. Madan et al. have proposed an analytical drain current model of HGD DM GAA-

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TFETs [13]. Vishnoi and Kumar [17] have modelled the threshold voltage of SOI TFETs by the localized charges into consideration. However, none of the above models [5, 7–10] have included the effects of the depletion regions at the source/channel and drain/channel depletion regions on the performance of their proposed TFET devices.

Ignoring the localized charges, Kumar et al. [18] have recently modelled the electrical characteristics of fully depleted DM DG-TFETs by considering the depletion charges at both source/channel and drain/channel junction. Although, their proposed model shows good validity for low gate bias and high drain bias operation of the TFETs, but the model is not applicable for the high gate bias and low drain bias operation of the device where the surface potential of the TFETs becomes insensitive due to dominant mobile charge carriers (i.e., inversion /accumulation charge for p^-/n^- type channel material) in the channel [19–21]. In this direction, Wu et al. [19] have modelled surface potential of SOI TFETs while Jain et al. [20] have proposed a surface potential based model for the drain current of DG TFETs by taking the mobile charge carriers in the channel into consideration. However, Both Wu et al. [19] and Jain et al. [20] did not consider the effects of localized charges. To the best of our knowledge, no significant work has been reported on the simultaneous modeling of surface potential, drain current and threshold voltage of the DM-HGD DG-TFETs by taking the effects of all charges (i.e., localized charges near the source/channel junction and mobile charges in channel region) and depletion regions at source/channel and drain/channel junction has been reported in a compact form. The objective of the present paper is thus to develop a unified model for electrical characteristics of the DM-HGD DG-TFETs by taking the effects of localized charges near the source/channel junction, mobile charges in channel region (for high gate bias and low drain bias) and charges in the depletion regions of the device. The proposed DM-HGD DG-TFETs under study are believed to be fabricated by combining the fabrication of DMG TFET device [21] and HGD TFET [22].

In this paper, the electric field has been modelled by using the surface potential model obtained by following similar method as in [18] with suitable modifications. The electric field model has been used to model the BTBT generation rate at both source/channel and drain/channel junction. The tangent line approximation (TLA) method [23] has been used to model obtain the drain current by including effects of localized charges, mobile charges and depletion charges as mentioned earlier. The threshold voltage has been modeled by using the shortest tunneling path [24, 25] of DM-HGD DG-TFET. We have neglected the quantum confinement effects for channel thickness above 10 nm for the simplification purposes of our proposed model [26]. For validity of our proposed model results, a 2-D device simulation software from ATLAS™ of SILVACO International has been used [27].

2 Model Formulation

The schematic cross-sectional view of DM-HGD DG-TFET with localized interface charges is shown in Fig. 1(a). HereL_1,$L_2$$L_3$,$L_4$, L_d, L, t_{ox} and t_{si} are source/channel depletion length, tunneling gate length, auxiliary gate length, drain/channel depletion length, localized charge length, channel length, gate-oxide thickness, and channel thickness of the device, respectively. Fig. 1(b) shows the surface junction potentials ψ_0,ψ_1,ψ_2,$\psi_3$and ψ_4 at the corresponding position x_0,x_1,x_2, $x_3$and x_4, respectively.

2.1 Modeling of Surface Potential

The surface potential becomes either sensitive or insensitive to mobile charges in the channel depending upon the applied gate and drain bias of TFET devices [19]. The regime of operation of the TFET in which the surface potential becomes linearly dependent on the applied gate bias at a fixed drain voltage is called the depletion regime [20]. On the other hand, the surface potential becomes insensitive to applied gate bias for a fixed drain voltage is called mobile regime [20]. We have first developed the surface potential model for the depletion regime of operation, which is then modified by incorporating the mobile charge carriers to make it applicable for both the depletion and mobile regimes of operation of the TFETs.

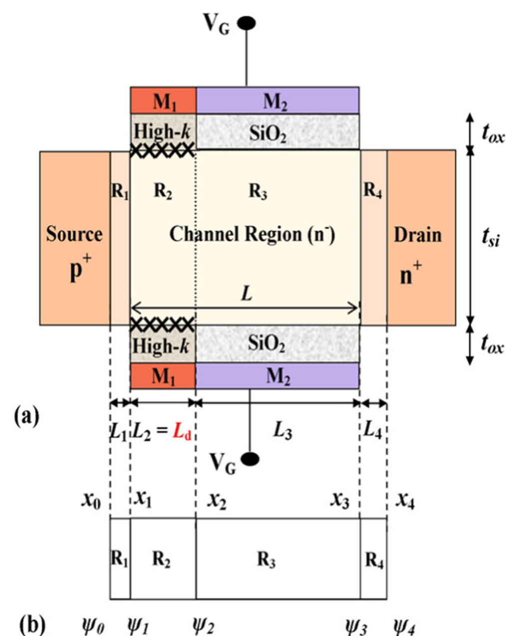

Fig. 1 (**a**). Schematic of DM-HGD DG-TFET with localized interface charges; (**b**) Surface junction potential of DM-HGD DG-TFET

2.2 2-D Electrostatic Surface Potential: Depletion Regime

In this case, the applied gate bias is assumed to be sufficiently low while the drain bias is considered to be high enough so that surface potential becomes linearly dependent on the applied gate voltage [20]. Now, following the similar methods as considered in [18], the expression of 2-D electrostatic surface potential $\psi_{dep,\ s,\ i}(x)$ in different regions $R_i(i=1,\ \ 2,\ \ 3,4)$ can given by:

$$\psi_{dep,s,i}(x) = \psi_{0i}(x) + \left[V_{G,i}^{eff} - \psi_{0i}(x)\right] \ (t_{Si}/2\lambda_i)^2 \qquad (1)$$

where, $V_{G,i}^{eff} = V_{GS} - \phi_{FB,i}$ is the effective gate voltage where V_{GS} is the gate-to-source voltage and $\phi_{FB,\ i} = (\phi_{FB0,\ i} - qN_{f,\ i}/C_i)$ is the effective flat band voltage where $\phi_{FB0,i} = \left(\phi_{M_i} - \chi_{Sub} - E_g/2\right)\ /q$ is the flat band voltage with $\phi_{M_1} = \phi_t$ and $\phi_{M_2} = \phi_a$ as the tunneling and auxiliary gate work functions, respectively; $N_{f,\ i}$ is the localized interface charge density with $N_{f,\ (1,3,4)} = 0$ and $N_{f,\ 2} = \pm 1 \times 10^{12}\text{cm}^{-2}$; χ_{Sub} and E_g are the electron affinity and energy band-gap of the substrate material, respectively; q is the electrostatic charge; $\lambda_i = \sqrt{(C_{ch}/C_i + 1/4)\ \ t_{si}^2}$ is characteristic length with $C_{ch} = \varepsilon_{si}/t_{si}$ and $C_i(i=1,\ \ 2,\ \ 3,4)$ as the channel region capacitance, and gate-oxide capacitance in the region $R_i(i=1,\ \ 2,\ \ 3,4)$, respectively. We have considered $C_1 \cong\ (2/\pi)\varepsilon_{ox}/t_{eq}$ and $C_4 \cong\ (2/\pi)\varepsilon_{ox}/t_{ox}$ as the respective fringing field capacitances in R_1 and R_4 regions obtained by the conformal mapping techniques [28]. $C_2 = \varepsilon_{ox}/t_{eq}$ and $C_3 = \varepsilon_{ox}/t_{ox}$ are the respective capacitances of high-k and SiO_2 with $t_{eq} = \varepsilon_{ox}t_k/\varepsilon_k$ as equivalent oxide thickness (EOT)where ε_{ox} and ε_k are the respective permittivities of SiO_2 and high-k gate dielectric, and $\psi_{0i}(x)$ is the center potential in the regions $R_i(i=1,\ \ 2,\ \ 3,4)$ which can be expressed as [18]:

$$\begin{gathered}\psi_{0i}(x) = A_i\exp(\beta_i(x - x_{i-1})) + B_i\exp(-\beta_i(x - x_{i-1})) + P_i \\ P_i = V_{G,i}^{eff} + \left(qN_i\lambda_i^2/2\varepsilon_{si}\right), \quad \beta_i^2 = 2/\lambda_i^2\end{gathered} \qquad (2)$$

where, P_i is the mid-surface potential of the device and, A_i and B_i are arbitrary constants to be determined from boundary condition [18].

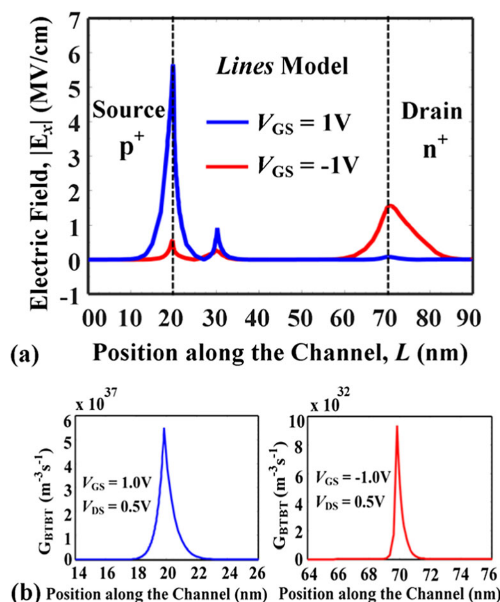

Fig. 2 Comparisons of (**a**) $|E_x|$, and (**b**) G_{BTBT} along the channel for different V_{GS} and constant $V_{DS} = 0.5$ V of DM-HDG DG-TFET

2.3 2-D Electrostatic Surface Potential: Impacts of Mobile Charges

In this sub-section, the impact of mobile charge carriers on the surface potential profile has been studied under a high gate bias and low drain conditions. The mobile charge carriers in the channel created under above biased conditions saturate the mid-surface potential, P_i [20] and narrows characteristics length, λ_i [29] of the device. To include the effect of the mobile charge carriers, we can write the surface potential, $P_{mob,\ i}$ by an empirical equation as:

$$P_{mob,i} = 0.5\left(P_i + \psi_m - \sqrt{(\psi_m - P_i)^2 + \delta^2}\right) \qquad (3)$$

where, δ is the smoothing factor (whose value is 0.04 for whole operation region) and ψ_m [19] is the mobile charge surface potential which can be expressed as:

$$\psi_m = \left[V_{DS} + \psi + u(P_i - V_{DS} - \psi) + v(P_i - V_{DS} - \psi)^2\right] \qquad (4)$$

where, u and v are two fitting parameters; ψ is the surface potential needed to create sufficient mobile charge carriers to protect the gate modulation which can be given by:

$$\psi = V_T\ln\left(N_{ch}N_m/n_i^2\right) \qquad (5)$$

where, V_T is the thermal voltage; N_{ch} is the channel doping concentration; N_m is the mobile charge density corresponding to the transition from linear to saturation variation and its extracted value is $1 \times 10^{18}\ \text{cm}^{-3}$ [20].

Similarly, $\lambda_{mob,\ i}$ can be expressed by considering the mobile charge carriers in the channel regions by variational approach [29] as:

$$\left(\frac{1}{\lambda_{mob,i}}\right)^2 = \left(\frac{1}{\lambda_i}\right)^2 - \left(\frac{8qN_{inv,i}}{t_{si}\varepsilon_{si}(\psi_0 - P_{mob.i})}\right) \qquad (6)$$

where, ψ_0 is the built-in-potential between source and channel region [18] and $N_{inv,i} = 2C_i\left(V_{G,i}^{eff} - P_{mob,i}\right)$ is the inversion charge density [30].

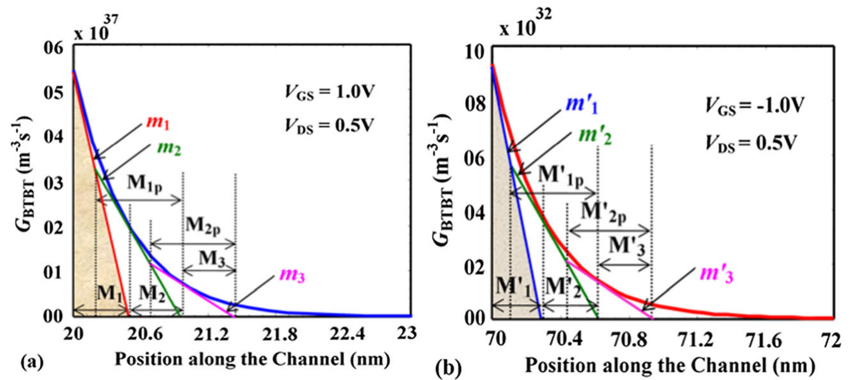

Fig. 3 G_{BTBT} along the channel for (**a**) forward gate bias i.e., $V_{GS} = 1$ V and; (**b**) ambipolar gate bias i.e., $V_{GS} = -1$ V of DM-HGD DG-TFET

Thus, the expression of 2-D electrostatic surface potential $\psi_{s,\ i}(x)$ after considering the mobile charge carriers can be expressed as:

$$\psi_{s,i}(x) = \psi_{mob,0i}(x) + \left[V_{G,i}^{eff} - \psi_{mob,0i}(x)\right] \ (t_{Si}/2\lambda_{mob,i})^2 \quad (7)$$

$$\psi_{mob,0i}(x) = [A_i \exp(\beta_{mob,i}(x - x_{i-1})) + B_i \exp(-\beta_{mob,i}(x - x_{i-1})) + P_{mob,i}] \quad (8)$$

$$\beta_{mob,i}^2 = 2/\lambda_{mob,i}^2 \quad (9)$$

Now, this surface potential $\psi_{s,\ i}(x)$ is applicable for both the depletion and mobile regimes of operation of the device.

2.4 Modeling of Drain Current

The drain current (I_d)of TFET devices can be defined as the integral of BTBT generation rate (G_{BTBT}) over the entire tunneling volume and can be expressed by Kane's model [31]:

$$I_d = q \int_{Voiume} G_{BTBT} dV = q t_{si} \int A_{Kane} E^{\alpha} \exp\left(-\frac{B_{Kane}}{E}\right) dx dw \quad (10)$$

where, A_{Kane} and B_{Kane} are the Kane's tunneling process-dependent parameters [18]; α is a material-dependent parameter and its value is 2 for direct band-gap material (e.g., InAs) and 2.5 for indirect band-gap material (e.g., Si); E is the local electric field. It has been mention that lateral electric field (E_x) considered mainly for obtaining the BTBT generation rate of TFETs device [7, 14, 21]; So, E can be replaced by E_x for obtaining the BTBT generation rate. E_x can be derived by differentiating the $\psi_{s,\ i}(x)$ with respect to x, ($E_x = -\partial\psi_{s,\ i}(x)/\partial x$). The variation of $|E_x|$ and its corresponding G_{BTBT} along the channel for different gate bias condition (i.e., forward bias, $V_{GS} = 1$V and ambipolar bias, $V_{GS} = -1$V) are shown in Fig. 2(a) and (b) at constant $V_{DS} = 0.5$V of DM-HGD DG-TFET device. From the Fig. 2(b), it is cleared that the value of $|E_x|$ at source/channel junction in forward bias, $V_{GS} = 1$V is much greater than ambipolar bias, $V_{GS} = -1$V; so, we have neglected the effect of ambipolar bias for G_{BTBT} calculation in forward bias. Similarly, the value of $|E_x|$ at drain/channel junction for forward bias is much smaller than ambipolar bias; so we have neglected the effect of forward bias for G_{BTBT} calculation in ambipolar bias. Hence, we have calculated G_{BTBT} for obtaining the drain current in all bias (i.e., ambipolar to forward bias) separately which is described in the subsection B-I and B-II, respectively.

2.5 BTBT Generation Rate in Forward Gate Bias

Under forward bias condition, we have calculated the area of G_{BTBT} curve at source/channel junction as shown in Fig. 3(a). The tangent line approximation (TLA) method [23] has been

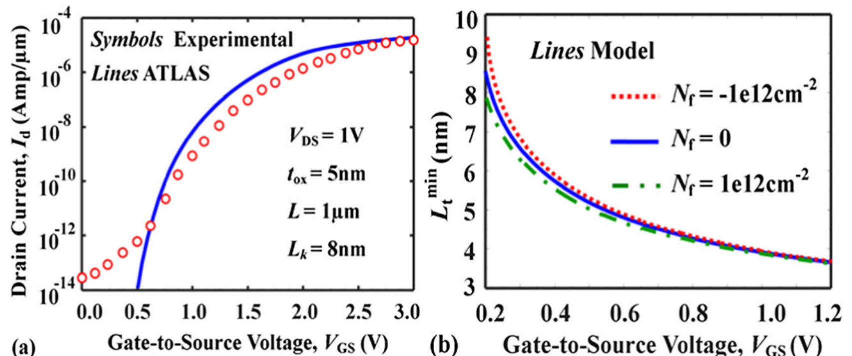

Fig. 4 (**a**) Calibration of the ATLAS™ TCAD data with the experimental results of HGD SOI-TFET [34]; (**b**) Variation of L_t^{min} with V_{GS} for different N_f of DM-HGD DG-TFET at V_{DS} = 0.5 V

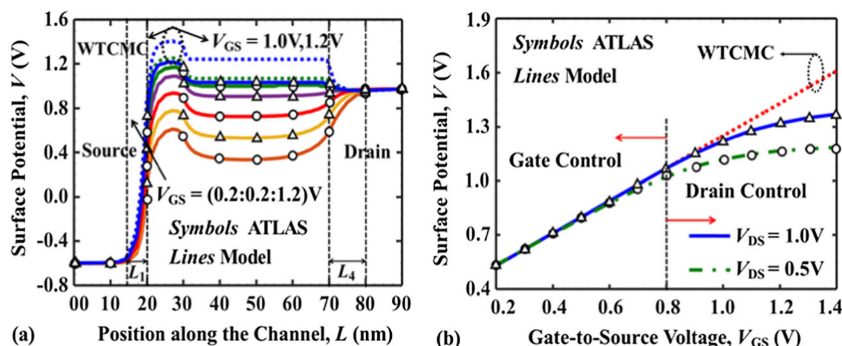

Fig. 5 (**a**) Variation of surface potential along the channel for different V_{GS} of DM-HGD DG-TFET at constant $V_{DS} = 0.5$ V; (**b**) Variation of surface potential against V_{GS} for different V_{DS} of DM-HGD DG-TFET

used for obtaining the area of G_{BTBT} curve to avoid numerical integration method [17, 23]. Following the method of [23], the area of G_{BTBT} curve can be expressed as:

$$G_{\text{BTBT}}(For) = [(G_1 + G_2 + \ldots\ldots\ldots\ldots + G_n) - (G_{1p} + G_{2p} + \ldots\ldots + G_{(n-1)p})] \quad (11)$$

where G_1,G_2………G_n are the area under the tangent lines m_1, m_2………m_n; and G_{1p}, G_{2p}. ………$G_{(n-1)p}$ are the overlap area between the tangent lines m_1 & m_2,m_2& m_3 and $m_{(n-1)}$ & m_n, respectively(see Fig. 3(a)).

$$G_n = \frac{G'_{BTBT}}{2}\left[(L_1 + M_1 + M_2 + \ldots\ldots\ldots\ldots + M_{n-1})M^2_{(n-1)p}\right] \quad (12)$$

$$G_{(n-1)p} = \frac{G'_{BTBT}}{2}\left[(L_1 + M_1 + M_2 + \ldots\ldots\ldots\ldots + M_{n-2}) \times (M_{(n-1)p} - M_n)^2\right] \quad (13)$$

$$M_{(n-1)p} = \left[\frac{G'_{BTBT}(L_1 + M_1 + M_2 \ldots\ldots\ldots\ldots + M_{n-2})M_n}{M'_{BTBT} - M_{BTBT}}\right] \quad (14)$$

$$M_n = \left[\frac{G_{BTBT}(L_1 + M_1 + M_2 \ldots\ldots\ldots\ldots + M_{n-1})}{G'_{BTBT}(L_1 + M_1 + M_2 \ldots\ldots\ldots\ldots + M_{n-1})}\right] \quad (15)$$

$$M'_{BTBT} = G'_{BTBT}(L_1 + M_1 + M_2 \ldots\ldots\ldots\ldots + M_{n-2}) \quad (16)$$

$$M_{BTBT} = G'_{BTBT}(L_1 + M_1 + M_2 + \ldots\ldots\ldots M_{n-1}) \quad (17)$$

where G'_{BTBT} is the derivative of G_{BTBT} with respect to x.

2.6 BTBT Generation Rate in Ambipolar Gate Bias

Figure 3(b) shows the variation of G_{BTBT} along the channel of DM-HGD DG-TFET in ambipolar bias condition (i.e.V_{GS} = − 1V). We have calculated the area of G_{BTBT} curve by using the TLA method in the same manner as described earlier for the forward bias condition.

$$G_{\text{BTBT}}(Amb) = G_{\text{BTBT}}(For)|_{L_1 \Rightarrow L_1 + L_2 + L_3} \quad (18)$$

Since, both G_{BTBT}(For) and G_{BTBT}(Amb) are symmetrical about the interface junction, total G_{BTBT} can be expressed as:

$$G_{BTBT} = 2(G_{BTBT}(For) + G_{BTBT}(Amb)) \quad (19)$$

It is reported that about 95% accuracy can be achieved in the calculation of the area of curve by using the TLA method if the minimum number of steps is = 4 [17, 23].

Assuming a fixed channel width (w = 1μm) in Eq. (10), I_d can be expressed in the (Amp/μm) as:

$$I_d = (qt_{si}G_{BTBT} + I_{lea})f_{\text{fermi}} \quad (20)$$

where, [32] I_{lea} is the correction factor which is introduced to ensure zero I_d at V_{DS} = 0V in the output characteristics of the device; I_{lea} is the leakage current which is included in calculation of I_d by an empirical equation given by [33]:

$$I/ea = 1 \times 10^{-10}\exp(-\varnothing_{\text{FB,i}}/7V_{\text{T}}) \quad (21)$$

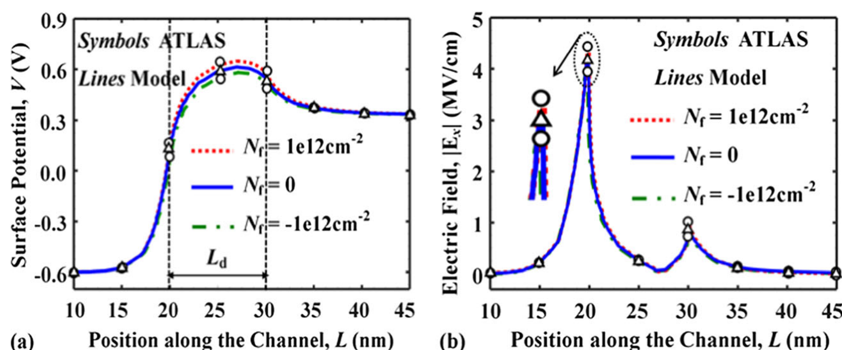

Fig. 6 (**a**) Variation of surface potential (**b**) and electric field along the channel for different N_f of DM-HGD DG-TFET at V_{GS} = 0.2 V, V_{DS} = 0.5 V

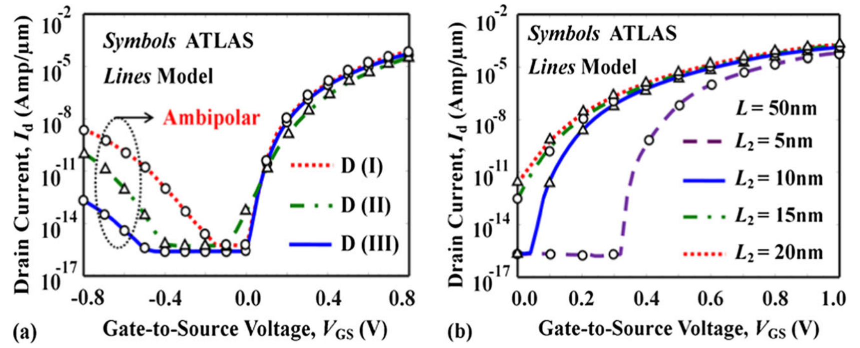

Fig. 7 (**a**) Comparisons of I_d against V_{GS} for different combinations of DM-HGD DG-TFET structures at constant V_{DS} = 0.5 V; (**b**) Variation of I_d against V_{GS} for different L_2 of DM-HGD DG-TFET at fixed L = 50 nm

2.7 Modeling of Threshold Voltage

Threshold voltage (say V_{th}) is an important parameter of any TFET device. It can be defined as the gate voltage at which the energy tunneling barrier tends to saturate [24]. We have used the concept of shortest tunneling path (L_t^{min}) extract of the device under study [25]. The L_t^{min} can be defined as the lateral distance from the source/channel junction (x = 0) to the point (x = L_t^{min}) where the surface potential is changed by E_g/q. Thus, L_t^{min} can be expressed as [18]:

$$L_t^{\min} = x\left(\psi_0 + E_g/q\right) - x(\psi_0) \tag{22}$$

When the surface potential at x = L_t^{min} reaches at the potential of $V_{DS} + V_T \ln(N_4/n_i)$ [24]; then the exponential function of I_d becomes a linear function of the applied V_{GS}; and the corresponding $V_{GS} = V_{th}$ is obtained by solving the following equation:

$$\psi_{s,i}\left(x = L_t^{\min}\right)|_{V_{GS}=V_{th}} = \psi_4 = V_{DS} + V_T \ln(N_4/n_i) \tag{23}$$

where, V_{DS}, N_4, and ψ_4 are the drain-to-source voltage, drain doping concentration and built-in-potential between drain/channel junction, respectively [18].

3 Results and Discussion

In this section, the model results of DM-HGD DG-TFETs are validated with the ATLAS™ TCAD simulation data. The Non-local, Trap-assist tunnelling (TAT), Shockley-Read-Hall recombination (SRH), Concentration and electric field dependent Lombardi (CVT), Auger recombination and bandgap-narrowing (BGN) models have been included in the simulation tool for characterizing the transport behaviour of the DM-HGD DG-TFET under consideration. The syntax *"Interface"* has been used to capture the fixed interface charges of the proposed device in TCAD simulation. The doping concentration of source, channel and drain are in the effective gate voltage of the devices $N_1 = 1\times10^{20}$ cm^{-3}, N_2 = N_3 1×10^{16} cm^{-3} and, $N_4 = 5\times10^{18}$ cm^{-3} with L_2 = 10nm, L_3 = 40nm, L = 50nm, t_{ox} = 2nm, t_{Si} = 12nm, respectively. The tunneling and auxiliary gate work function are taken as ϕ_1 = 4.2eV (M_o,IrO_2) and ϕ_2 = 4.6eV (Ta,W) for the maximum ON-to-OFF current ratio of the device [18]. First of all, we have calibrated the ATLAS™ TCAD tool by comparing the simulation data with the experimental results [34] of the HGD SOI-TFET in Fig. 4(a). The slight mismatching is attributed to the non-ideal parameters in the experimental devices. In other words, the reasonable matching confirms the validity of the TCAD simulator used in our study. Now, Fig. 4(b) shows the variation of L_t^{min} against V_{GS} for different N_f of DM-HGD DG-TFET. It is It is observed from the figure that Ltmin changes with N_f at low V_{GS} (i.e. V_{GS} V_{GS} < 0.4V) but becomes independent of N_f with the increase of V_{GS} due to the negligible localized interface potential, qN_f/C_1 (see Eq. (1)).

Figure 5(a) shows the variation of surface potential along the channel for different V_{GS}. It is observed from the figure that the surface potential is increased with the increase in V_{GS}. Further, when V_{GS} is increased more than a certain value, (i.e.,

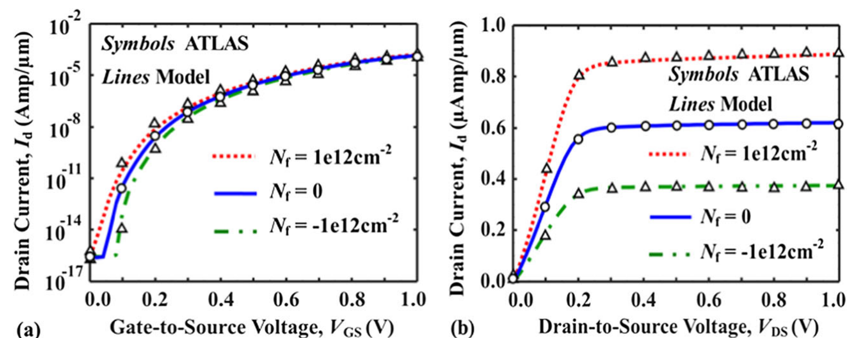

Fig. 8 (**a**) Variation of I_d against V_{GS} for different N_f of DM-HGD DG- TFET at constant V_{DS} = 0.5 V; (**b**) Variation of I_d against V_{DS} for different N_f of DM-HGD DG-TFET at constant V_{GS} = 0.4 V

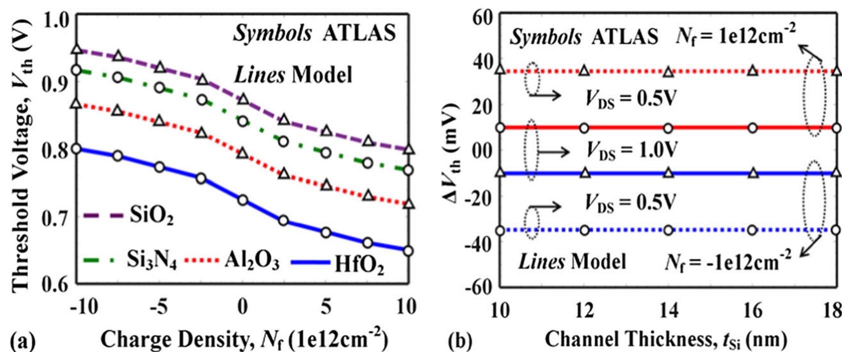

Fig. 9 (**a**) Variation of V_{th} against N_f for different combinations of gate dielectric constant (localized region) of DM-HGD DG-TFET; (**b**) Comparisons of ΔV_{th} against t_{si} for different N_f of DM-HGD DG-TFET

$V_{GS} > 0.8V$), the surface potential becomes insensitive to V_{GS}. The variation of surface potential with V_{GS} for different V_{DS} is shown in Fig. 5(b). It is observed that the surface potential varies linearly with low V_{GS} (i.e., gate-control regime). However, beyond a certain value of V_{GS}, the surface potential is screened from further bending (i.e., drain-control regime) due to the creation of a significant amount of mobile charge carriers in the channel [19]. A good matching between the TCAD and model results confirms the validity of the surface potential model of the DM-HGD DG-TFETs under study when the model includes the effect of mobile charge carriers in the channel. However, a considerable amount of mismatching between model and TCAD simulation results is observed when we model the surface potential without considering the mobile charge carriers (WTCMC). Clearly, the inclusion of mobile charge carriers in our model for proposed the DM-HGD DG-TFET is well justified.

The variations of surface potential and its corresponding electric field along the channel for different N_f have been plotted in Fig. 6(a) and (b) respectively. It is observed that both the surface potential and its corresponding electric field are increased (decreased) with the increase (decrease) in the positive (negative) values of N_f due to decrease (increase) in the effective flat band voltage.

Figure 7(a) shows the comparison of I_d versus V_{GS} plots for different DG-TFET device structures for a fixed V_{DS} =0.5 V where D(I), D(II) and D(III) represent the the I_d-V_{GS} plots for the DM DG-TFET with as the only gate oxide (i.e. with no SiO_2 region), single metal (with $\phi_M = 4.2eV$) gate based HGD DG-TFET, and DM-HGD DG-TFET structures respectively. The ambipolar drain current (due to negative V_{GS}) is observed to be the smallest in our proposed DM-HGD DG-TFET structure. The variation of I_d vs V_{GS} with for different tunneling gate length (L_2) of the DM-HGD DG-TFET is shown in Fig. 7(b) for a fixed channel length L_2 = 50nm. It is observed that L_2 = 10nm is possibly the best value for getting maximum ON-to-OFF drain current ratio. That is why, we have used L_2 = 10nm for calculating the model results of DM-HGD DG-TFET in the present manuscript.

In Fig. 8(a), we plotted I_d-V_{GS} characteristics of the DM-HGD DG-TFET for different values of N_f. The drain current, I_d, is observed to be more sensitive to for low (i.e. low V_{GS} (i.e., $V_{GS} < 0.4V$) due to localize interface charge (as seen in Fig. 4(b)) is more effective in this gate bias. The output characteristics of the DM-HGD DG-TFET for different N_f is shown in Fig. 8(b). It is observed from the figure that I_d is increased (decreased) with positive (negative) value of N_f due to the increase (decrease) in the number of charge carriers tunneled from the valance band of the source to conduction band of the channel owing to the decrease (increase) in the shortest tunneling path (See Fig. 4(b)) of the TFET.

Figure 9(a) shows the variation of V_{th} with N_f for different combinations of dielectrics in the localized charge region of the DM-HGD DG-TFET. The threshold voltage, V_{th} is decreased for higher dielectric constant based oxides due to the increased electric field at the source/channel junction [18]. The change in threshold voltage (ΔV_{th}) with t_{Si} for different values of N_f is shown in Fig. 9(b) to note that (ΔV_{th}) is

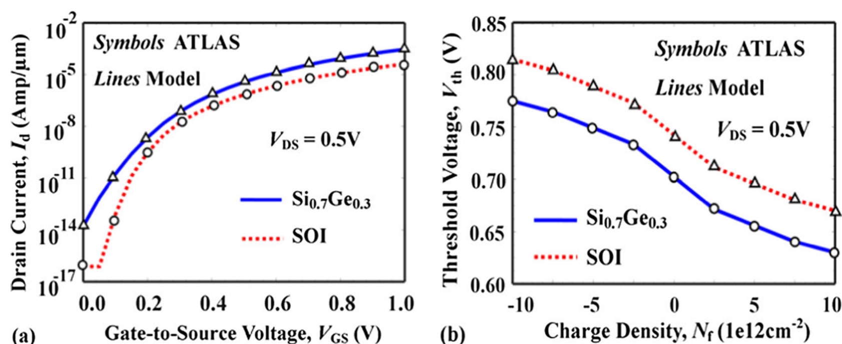

Fig. 10 (**a**) Variation of I_d against V_{GS} for different structures such as SiGe DM-HGD DG-TFET and DM-HGD SOI-TFET; (**b**) Variation of V_{th} against N_f for different structures SiGe DM-HGD DG-TFET and DM-HGD SOI-TFET at constant V_{DS} = 0.5 V

independent of t_{Si} but it is affected by N_f mainly for low V_{DS} values.

Finally, we will show the validity of our proposed model for the TFETs with different materials and different structures such as SiGe DM-HGD DG-TFET and SOI-based DM-HGD TFET. In Fig. 10(a), the I_d-V_{GS} characteristics of SiGe DM-HGD DG-TFET and DM-HGD SOI-TFET for a fixed $V_{DS} = 0.5$ V have been plotted. The variation of V_{th} with N_f for both the SiGe DM-HGD DG-TFET and SOI DM-HGD TFET structures is shown in Fig. 10(b). The good matching between the model and TCAD results confirms that our proposed model can also be extended for SiGe DM-HGD DG-TFET and SOI DM-HGD TFET structures.

4 Conclusion

The 2-D analytical modeling of the surface potential, drain current and threshold voltage characteristics of DM-HGD DG-TFET by taking the localized interface charges near the source/channel junction, mobile charges in channel region and charges in depletion regions at both source/channel and drain/channel junctions has been proposed in this paper. The TLA method has been used for obtaining the drain current model for both the forward gate bias and reverse gate bias (i.e. ambipolar regime of operation) of the device. The shortest tunneling path concept has been explored for obtaining the threshold voltage model of the DM-HGD DG-TFETs. The impacts of localized trap charges (due to high electric field near the source/channel junction) on the drain current and threshold voltage have been studied. The drain current is observed to be more sensitive to the localized charges at low gate bias while the threshold voltage is more sensitive to the localized charges at low drain bias. The validity of the model is established by showing a very good matching between the model results and commercially available ATLAS™ TCAD based simulation data of the proposed device.

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