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ORIGINAL PAPER

Analytical Modelling and Simulation of Si-Ge Hetero-Junction Dual Material Gate Vertical T-Shaped Tunnel FET

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Abstract

In this paper, a compact 2D analytical modelling of surface potential and simulation of Si-Ge hetero-junction Dual Material Gate Vertical t-shape T-FET is presented. In the proposed model, device is divided into two gate-metal work function named as tunneling gate and auxiliary gate. Both the biasing voltage of source and drain will have controlled effect on the device's surface potential which are used to access the depletion length of the tunneling junction. Therefore, the tunneling current will use the surface potential model as basic principle to drive the current model of the device. For solving the 2D Poisson equation with the necessary boundary conditions, parabolic approximation methods are employed. We test the reliability of surface potential on different parameters profile by varying it as a function of Si-Ge material mole-fraction, gate-source voltage, drain-source voltage, gate-oxide thickness, high k dielectric constant and different gate work function and various compound material used. Finally, we come out with the expression of the channel surface potential that will change in accordance with the drain and gate biasing voltage. The validity of the projected model has been confirm by showing agreement between the analytical findings and TCAD simulation results.

Keywords Dual material gate vertical t-shape tunnel FET (DMG V tT-FET) · Analytical modelling · 2-D Poisson equation · Band 2 band tunnelling (B2BT) · Electric field · Mobile charge · Subthreshold slope (SS) · Kane model

1 Introduction

With the advance period, the technology is growing faster at a rapid pace. The down scaling of device's dimension to the conventional becomes a major challenge in respect of reduction in the power dissipation and the charge leakage problem. Therefore, the nano-scale era has open the doors for further research analysis [1, 2]. From the half of the century, the MOSFET has been playing a role of back-bone in the era of the Integrated circuit, it is now the time come to propose the new model structures in the field of the nano-electronics, which operates at the high frequencies and consists of all the optimized scaling issues with less power consumption and device processing speed for circuit implementation [3–5]. Irrespective of all its excellent strengths, like steeper subthreshold-slope (SS), low subthreshold voltage (V_T) and high ratio current I_{ON}/I_{OFF} for super low power implementations, Tunnel FET has been strongly investigated. [6–8]. With the aforementioned advantages, TFET comes with its own kinds of issues, which involves the existence of the am-bipolarity and low I_{ON} current. This trigger increase in the OFF current which cannot be entirely extinguished because of leakage [9, 10]. As the TFET works with the principal of B2BT, so the factors like indirect bandgap tunneling and mass of high effective carrier will make the performance poor which causes the lower ON current [11]. Given these limitations, comprehensive studies have been conducted to increase the Silicon TFET I_{ON} value, including the use of lower bandgap hetero-junction material like Germanium, Indium-Arsenide and various high dielectric constant [12–14]. Simulated device scalability will also be improved by vertical channel transmission. With the help of the TCAD Sentaurus simulation tool, the different aspects of Vertical transmitted

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TFET has now been studied extensively [15, 16]. However, for effective circuit computation and for better understanding of the operating function still we require a compact analytical modelling. In comparison to the MOSFET device, the channel of the tunneling device must be centered with the electrostatics and carrier process transportation [16–18]. Earlier studies of TFET modeling of single metal gates, documented in the publication have some drawbacks. Previous works used series expansions for the single metal-gate to calculate the channel potential surface and that is relatively complex and computationally ineffective [19–21]. This DMG V tT-FET consist of two consecutive contact gates, first one near to the drain is auxiliary gate and second one to the source side is tunneling gate. The tunneling gate work function is kept less than that of auxiliary gate. This workfunction demonstrate the benefits of high-performance proposed device. The comprehensive TCAD simulation analyzed considering source and Si-Ge layer at the tunneling medium with different material and rest of channel and drain are of different material. However, a detailed analytical modelling of Dual Material Gate of Vertical t shape T-FET is required, taking into account of two separate cases of different workfuntions of two different material considering mole-fraction engineering of SiliconGermanium hetero-junction at the tunneling interface.

In this paper, using 2-D Pseudo Poisson equation, a compact 2-D analytical surface potential modelling of Si-Ge based hetero-junction Dual Material-Gate Vertical t-shape Tunnel-Field Effect Transistor is discussed. The development of this model is done by integrating Band 2 band tunneling generation rate which the consideration of Silicon germanium material bandgap at the source-channel interface and channel drain depletion range [9, 22]. To outcome with the drive current, Kane-model is used for the tunneling operation, considering that somehow the electrical field will remain constant at both source channel and channel drain junctions. In the next section, we will illustrate the authorization of our proposed analytical model results with our TCAD simulations.

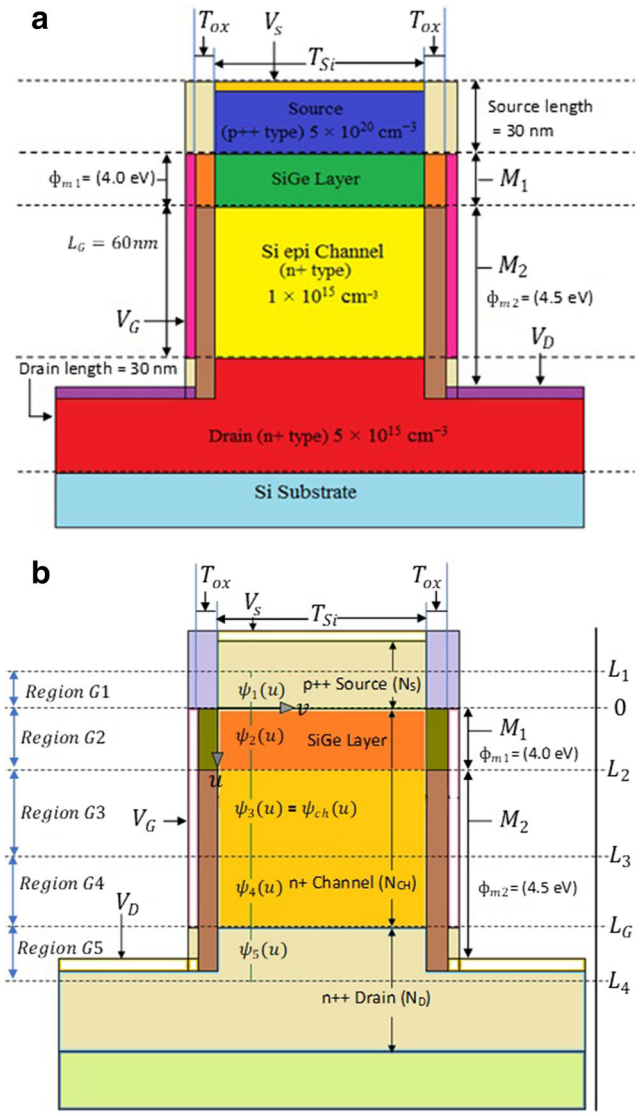

Fig. 1 **a**. Simulated schematic diagram of a Dual Material-Gate Vertical t-shape T-FET (DMG V tT-FET) with embedded Si-Ge Layer. 1 **b** Modeled schematic diagram of n-channel DMG V tT-FET, parted into five regions ($G1$, $G2$, $G3$, $G4$ and $G5$) with interfaces at L_0, L_1, L_2, L_3, L_G and L_4 and corresponding surface potentials $\psi_1(u)$, $\psi_2(u)$, $\psi_3(u)$, $\psi_4(u)$ and $\psi_5(u)$ respectively.

2 Surface Potential Model Development

The schematic simulated and modeled illustration of Dual Material Gate Vertical t-shape T-FET device shown in Fig. 1a, b added to this report, with following descriptions: Source side concentration (p++) (N_S) = $5 \times 10^{20}\ cm^{-3}$, channel doping concentration (n+) (N_{CH}) = $1 \times 10^{15}\ cm^{-3}$, (n++) drain side concentration (N_D) = $1 \times 10^{18}\ cm^{-3}$, with dielectric material HfO_2 as gate oxide thickness (T_{ox}) = 2 nm. The device scaling for SiliconGermanium layer is 10 nm and for the channel length is 60 nm via two work function of metal Gate ϕ_{m1} and ϕ_{m2} at M_1 and M_2 named as tunneling gate and auxiliary gate and optimize them at 4.00 eV and 4.5 eV respectively. Length of 30 nm is taken for both source and drain. The doping ratio from drain to source is kept low to maintain low I_{OFF} current. The value taken for silicon electron affinity is (χ_{Si}) = 4.05 eV and the silicon band-gap is (E_G) = 1.12 eV, whereas for Germanium (χ_{Ge}) = 4.0 eV and band-gap (E_G) = 0.70 eV. These are the standard attributes drawn via TCAD manual synopsis [23, 24]. Source channel and channel drain interface are kept instantaneous for ease. (V_G) and (V_D) are the applied input voltage and are fixed at 0.6 and 0.5 V whereas the source junction (V_S) is kept ground for the reference voltage. G1, G2, G3, G4 and G5 regions are defined for source channel and drain of the device respectively as shown in Fig. 1b, whereas G_{CH} represent the channel length. The source and drain depletion region were define by region G1 and G5,

while the channel area further sub-divided into three sub-G2, G3 and G4 regions, respectively. ϕ_{m1} material at M_1 is located correspondingly across the define Si-Ge layer. Formation of the depletion width at the source-channel and channel drain junction will define and calculated as L_1, L_3 & L_4 after the biasing voltage applied to the device. The resultant length L2 formed across the Si-Ge layer is considerably larger than the L1 and vice-versa for the channel-drain junction. The happen due to inversely-proportional relation between doping concentration and depletion width. A description of the specifications used to model and simulate the device is given below. (Table 1)

At Fig. 2, DMG V t shape T-FET device's energy band diagram is illustrating precisely the ON and OFF condition with inherit Si-Ge compound at the interface of source channel. The E_V and E_C are the device valance band and the conduction band respectively. The $Si_{1-x}Ge_x$ mole-fraction value is optimised at x = 0.8. The other affecting parameters like concentration of drain doping is taken to be 1×10^{18}, whereas the concentration of source doping is taken to be 5×10^{20} cm^{-3}. To operate the device, the applied biasing voltage taken at V_{GS} and V_{DS} is 0.5 and 0.6. For all these areas, it requires the essential boundary conditions to evaluate the 2D surface potential and the electric field of the device by using 2D Poisson equation. To calculate the depletion lengths relating to regions G1 & G4, we use the parabolic approximate method.

2.1 Proposed Surface Potential model method

As discuss, the full DMG Vertical t shape T-FET is classified into the 5 sub-divisions shown by Fig. 1b. The sub-divisions like G1 and G2 region specified for the generated depletion region at Si-Ge and Source-channel tunneling interface through first gate workfunction of value 4.0 eV, whereas for slightly doped intrinsic channel G3 division is considered with the gate workfunction value of 4.5 eV. Similarly, region G4 and region G5 are the drain-channel intersection depletion region.

Table 1 Description of Constraints used in Structure

CONSTRAINTS	STANDARDS
(p++) Source-Doping Conc. (N_S)	5×10^{20} cm^{-3}
(n+) Channel-Doping Conc. (N_{CH})	1×10^{15} cm^{-3}
(n++) Drain-Doping Conc. (N_D)	1×10^{18} cm^{-3}
Tunneling Gate Metal Work-function (ϕ_{m1})	4.0 eV
Auxiliary Gate Metal Work-function (ϕ_{m2})	4.5 eV
Gate oxide thickness (T_{ox})	2 nm
Source/Drain measurement	30 nm
length of the Channel (L_c)	60 nm
Gate Oxide Material	HfO_2

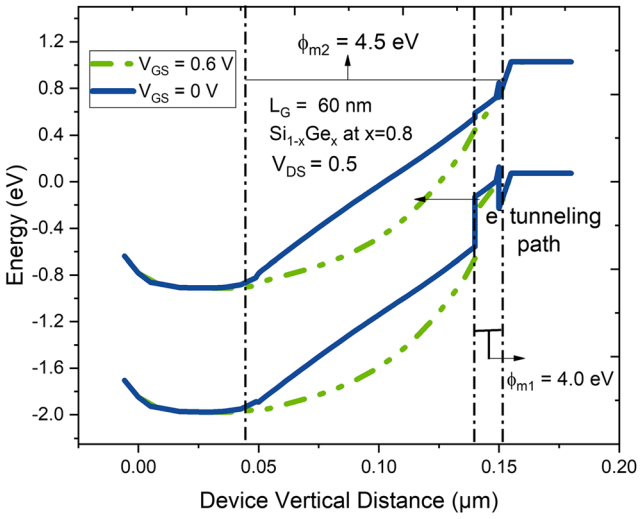

Fig. 2 TCAD Simulated energy-band diagram of Si-Ge inherited Dual Material Gate V tT-FET with operating V_{GS} = 0 V & 0.6 V as a ON and OFF state at V_{DS} = 0.5 V

To modeled the device surface potential, firstly we need to calculate the device boundary condition and via 2-D poisson equation [25, 26]. The band 2 band tunneling carrier generation rate is totally depends upon the device electric field generation at tunneling inter-junction. The electrostatic effect is not greatly influenced by the charge's mobility [27]. At the initial stage of transmission of device for OFF to ON state, the 2D Poisson equation can be express as:

$$\frac{\partial^2 \varphi_i(u,v)}{\partial u^2} + \frac{\partial^2 \varphi_i(u,v)}{\partial v^2} = \frac{qN_R}{\varepsilon_{si}} \tag{1}$$

Where $\varphi_1(u, v)$, signifies the M_1 region's electrostatic potential and $\varphi_2(u, v)$ for the rest of the device regions that is M_2. In this device, q represents the Coulomb charge, ε_{Si} represents the Silicon permittivity and ε_{SiGe} reflect the permittivity of Silicon-Germanium material and N_R represents the doped area. The second order polynomial parabolic approximation of the potential for the Dual material Gate for the region M1 and M2 is given by:

$$\varphi_1(u,v) = a_{01}(u) + b_{11}(u)v + c_{21}(u)v^2 \tag{2}$$

$$\varphi_2(u,v) = a_{02}(u) + b_{12}(u)v + c_{22}(u)v^2 \tag{3}$$

Where $a_{01}(u)$, $b_{11}(u)v$, $c_{21}(u)v^2$ and $a_{02}(u)$, $b_{12}(u)v$, $c_{22}(u)v^2$ are function coefficients of u which have to be calculated and obtained in v -axis form the boundary condition. Simple boundary conditions are established due to the continuity in device potential and displacement function of the electric field at body oxide interface at two regions: i) front-side (for region G1 and G2) ii) back-side (for region G3 and G4) [28].

1) Originally, the equation formed for the first boundary condition due to the potential difference arises at the semiconductor-oxide interface is equivalent to the defined surface potential $\varphi_1(u)$ for region M_1 and ii) $\varphi_2(u)$ for the region M_2 described as follows using (4) & (5):

$$\varphi_1(u,0) = \varphi_1(u,T_{si}) = \varphi_1(u) \tag{4}$$

$$\varphi_2(u,0) = \varphi_2(u,T_{si}) = \varphi_2(u) \tag{5}$$

The constant electric field across the oxide-semiconductor interface junction will give the relationship of second boundary condition as mention below:

$$\frac{\partial\varphi_1(u,v)}{\partial v} = -\frac{\varepsilon_{ox}}{\varepsilon_{si}T_{ox}}(V_{G1}-\varphi_1(u,0)) \tag{6}$$

$$\frac{\partial\varphi_2(u,v)}{\partial v} = -\frac{\varepsilon_{ox}}{\varepsilon_{si}T_{ox}}(V_{G2}-\varphi_2(u,0)) \tag{7}$$

$$V_{G1} = V_{GS}-V_{FB1} \tag{8}$$

$$V_{G2} = V_{GS}-V_{FB2} \tag{9}$$

$$V_{G1} = V_{GS}-\phi_{m1} + \chi_{SiGe} + E_{SiGe}/2 \tag{10}$$

$$V_{G2} = V_{GS}-\phi_{m2} + \chi + E_G/2 \tag{11}$$

In the above mention equation, the term C_{ox} represents the gate oxide capacitance (ε_{ox}/t), where ε_{ox} reflects the oxide permittivity. The effective gate oxide thickness is $t = T_{ox}$ for the division G2 and G3, while for the division G3 and G4 $t = T_{ox}/2$ is used, with respect to the field-fringing effect at the surface potential of the gate. Using eqs. (8) and (9) shown V_{G1} as the difference in potential between the gate source voltage V_{GS} and flat band voltage (V_{FB1}) to access further equation given as:

$$\frac{\partial\varphi_1(u,v)}{\partial v} = \frac{\varepsilon_{ox}}{\varepsilon_{Si}T_{ox}}(V_{G1}-\varphi_1(u)) \tag{12}$$

$$\frac{\partial\varphi_2(u,v)}{\partial v} = \frac{\varepsilon_{ox}}{\varepsilon_{Si}T_{ox}}(V_{G2}-\varphi_2(u)) \tag{13}$$

For the back-side of the surface potential, this condition is assessed at $v = T_{Si}$, where device body thickness is represented by T_{Si}.

2) The third limit conditions are arising with the zero-electric field at the position $v = T_{Si}/2$.The constants are derived by using these boundary conditions and outcome of the values after solving (2–13) given as:

$$a_{01}(u) = \varphi_1(u) \tag{14}$$

$$a_{02}(u) = \varphi_2(u) \tag{15}$$

$$b_{11}(u) = -\frac{C_{ox}}{\varepsilon_{Si}}(V_{G1}-\varphi_1(u)) \tag{16}$$

$$b_{12}(u) = -\frac{C_{ox}}{\varepsilon_{Si}}(V_{G2}-\varphi_2(u)) \tag{17}$$

$$c_{21}(u) = \frac{C_{ox}}{2\varepsilon_{Si}t_{Si}}(V_{G1}-\varphi_i(u)) \tag{18}$$

$$c_{22}(u) = \frac{C_{ox}}{2\varepsilon_{Si}t_{Si}}(V_{G2}-\varphi_2(u)) \tag{19}$$

In order to get the second order surface potential differential equation, we have to integrating all above constants back into equations [29]. At the interface, the above derived equation involves the effect of internal (C_{inf}) and external fringing capacitance (C_{outf}) and defined by following equations [30].

$$\frac{d^2\psi_1(u)}{du^2} - \frac{\psi_1(u)}{\omega_1^2} = -\frac{\left(V_{G1}-\frac{qN_aT_{Si}}{2C_f}\right)}{\omega_1^2} \tag{20}$$

$$\omega_1 = \sqrt{\frac{T_{si}\varepsilon_{Si}}{2C_f}} \tag{21}$$

Where,

$$C_f = C_{inf} + C_{outf} - \frac{\varepsilon_{ox}}{T_{ox}} \tag{22}$$

In addition, the inner fringing ability in region G3 is dependent on the device's surface potential whereas gate oxide thickness T_{ox} controls the outer fringing capacity. $\psi_1(u)$ represent the surface potential for the division G1 and similarly $\psi_2(u)$ for the division G2. It is done to prevent conflict with the programme's function and the procedure which is usually followed. Such definitions are as follows:

$$C_{inf} = C_{inf,max} exp\left| \frac{V_{Ge} - \frac{\varnothing_{dg}}{2}}{\frac{3\varnothing_{dg}}{2}} \right|^2 \tag{23}$$

And,

$$C_{inf,max} = \frac{2\varepsilon_{Si}}{\pi(T_{Si}/2)} \ln\left(1 + \frac{T_{Si}}{2T_{ox}}\right) \tag{24}$$

$$C_{outf} = \frac{2\varepsilon_{ox}}{\pi T_{ox}} \ln\left(1 + \frac{h_g}{T_{ox}}\right) \tag{25}$$

Where h_g is the height of the gate stack coming after conformal transformation. Now the tunneling junction boundary condition is required for obtaining the specific approach to the equation. For that we have taken the presumptions of depletion length L_1, L_2, L_3, L_4 for the sub-division G1, G2, G3 and G4 respectively. To address the solution for divisions G1 and G2, initially two boundary condition is used and that are:

$$\psi_1(-L_1) = -\varnothing_f \tag{26}$$

$$\frac{\partial\psi_1(u)}{\partial u} \approx 0 \tag{27}$$

This state is measured at $u = -L_1$. With regard to L_1 depletion length, we obtain the method in respect to find the surface potential for G1 region. The derived equation for the surface potential is given by:

$$\psi_1(u) = -\frac{qN_{seff}(u + L_1)^2}{2\varepsilon_{Si}} - \varnothing_f \tag{28}$$

Where,

$$N_{seff} = \frac{2\varepsilon_{Si}}{q}\left(\frac{qN_a}{2\varepsilon_{Si}} - \frac{C_{ox}V_{G1}}{\varepsilon_{Si}T_{Si}}\right) \tag{29}$$

And

$$\varnothing_f = V_{th} ln\left(\frac{N_a}{N_i}\right) \tag{30}$$

Similarly, for the region G2 surface potential will be extracted using same process containing Si-Ge layer of different metal workfunction at M1.

$$\psi_2(u) = V_{SiGe} - \left(V_{SiGe} - \varnothing_{dg}\right)\cosh\left(\frac{(u - L_2)}{\omega_{SiGe}}\right) \tag{31}$$

Where,

$$\omega_{SiGe} = \sqrt{\frac{T_{Si}\varepsilon_{SiGe}}{2C_{ox}}} \tag{32}$$

and V_{SiGe} consider as the difference in potential between gate source and respective flat band voltage. In consideration with the assumption of electron affinity at $(\chi_{SiGe}) = 4.0115$ eV at mole-fraction of 0.8.

$$V_{SiGe} = V_{GS} - V_{FB3} \tag{33}$$

The electron affinity (χ_{SiGe}), Band-Gap Energy (E_{SiGe}) and the assume permittivity (ε_{SiGe}) of $Si_{1-x}Ge_x$ material can find out using (34) by defining the value of the mole-fraction x. The (χ_{SiGe}), (E_{SiGe}) and (ε_{SiGe}) represent the SiliconGermanium's electron affinity, energy band gap and permittivity which can be determine using the linear relationship between molefration of $Si_{1-x}Ge_x$ material and express as follows:

$$E_{SiGe} = \begin{cases} 1.17 - 0.47x + 0.24x^2 & x < 0.85 \\ 5.88 - 9.58x + 4.43x^2 & x < 0.85 \end{cases} \tag{34}$$

$$\varepsilon_{SiGe} = 11.9(1 + 0.35x) \tag{35}$$

Because potential and electrical fields will remain constant at source-channel junction [27], Therefore to identify the two variables of L_1 and L_2, we can align the previously derived expression of surface potential in the section G1 and G2 at the position at $u = 0$.

$$\psi_1(u) = \psi_2(u) \equiv \varphi(0) \tag{36}$$

And,

$$\frac{\partial\psi_1(u)}{\partial u} = \frac{\partial\psi_2(u)}{\partial u} \tag{37}$$

This will be evaluated at $u = 0$, to locate the unknown. Where $\varphi(0)$ is defined as:

$$\varphi(0) = -\left(\left(V_{GS} - V_{FB1} - \varnothing_{dg}\right)^2 + 2(V_{GS} - V_{FB1})\varnothing + \varnothing^2\right)^{0.5} + (V_{GS} - V_{FB1} + \varnothing) \tag{38}$$

Where

$$\varnothing = \frac{qN_{seff}\omega_2^2}{\varepsilon_{Si}} \tag{39}$$

Which gives,

$$L_1 = \sqrt{\frac{2\varepsilon_{Si}(\varphi(0)-\varnothing_f)}{qN_{seff}}} \tag{40}$$

And,

$$L_2 = \omega cosh^{-1}\left(\frac{V_{GS}-V_{FB3}-\varphi(0)}{V_{GS}-V_{FB3}-\varnothing_{dg}}\right)$$

Using (33) it can be rewritten as

$$L_2 = \omega cosh^{-1}\left(\frac{V_{Ge}-\varphi(0)}{V_{Ge}-\varnothing_{dg}}\right) \tag{41}$$

In this section the channel region's surface potential (H) has been modeled in the continuation form with respect to the drain and source biasing which involves the dual transition modulation effect, which means the evolution control from the gate to the drain terminal. The H function the channel can be configured as:

$$H = \frac{1}{2}\left[V_{DS}+\varphi+\varphi_{chd}-\sqrt{(-V_{DS}-\varphi+\varphi_{chd})^2+\alpha^2}\right] \tag{42}$$

$$\varphi_{chd} = \frac{1}{2}\left(\sqrt{V_{GS}-V_{FB}+\frac{\gamma_1^2}{4}}-\frac{\gamma_1}{2}\right)^2 \tag{43}$$

And

$$\varphi = V_{th}ln\left(\frac{N_aN_i}{n_i^2}\right) \tag{44}$$

Also,

$$\gamma_1 = \frac{\sqrt{2\varepsilon_{Si}qN_{Si}}}{C_{ox}} \tag{45}$$

We consider α as a minor factor for each behavior, with value of 0.04 [22]. Lastly, $\psi_3 or\ \psi_{ch}$ are the obtained equation for the device's channel potential for the G3 region and expressed as:

$$\psi_{ch} = H + V_{th}ln\left(\frac{1}{V_{th}}\left(V_{th}+\frac{\sqrt{H}}{\sqrt{H}+\gamma_1}(V_{GS}-V_{FB}-H)+\frac{1}{2}\left(\frac{H}{\left(\sqrt{H}+\gamma_1\right)^2}-\frac{\gamma_1(H-2)}{2\left(\sqrt{H}+\gamma_1\right)^3}\right)(V_{GS}-V_{FB}-H)^2\right)\right) \tag{46}$$

To derive equation at the drain channel junction i.e. for the G4 and G5 region, identical approach has been used as that of source channel junction. However, excluding the effect of Si-Ge and value used for the workfunction at M2. This will result in the change of depletion length calculated via surface potential $\psi_4(u)$ and $\psi_5(u)$.

$$\psi_4(u) = V_{G2}-(V_{G2}-\varnothing_{dg})\cosh\left(\frac{(u-L_G+L_3)}{\omega_2}\right) \tag{47}$$

$$\psi_5(u) = -\frac{qN_{deff}(u-L_1-L_4)^2}{2\varepsilon_{Si}}-\varnothing_{f1} \tag{48}$$

Where,

$$\varnothing_{f1} = V_{th}ln\left(\frac{N_D}{N_i}\right) \tag{49}$$

And

$$N_{deff} = \frac{2\varepsilon_{Si}}{q}\left(\frac{qN_D}{2\varepsilon_{Si}}-\frac{C_{ox}V_{G2}}{\varepsilon_{Si}T_{Si}}\right) \tag{50}$$

Equations (4) and (5) are assessed at $u = L_G$ and equated with a reduction in equation length at the same boundary conditions as for region G1 and G2. The depletion length L_3 and L_4 are derived subsequently. The depletion length L_3 is greater than L_4 the because of light doped channel as compared to the drain.

In order to test the validity of the results obtained from the above eqs. 28, 31, 46, 49 & 50 for the G1, G2, G3, G4 and G5 regions, we need to compare our simulation results with the model once. In Fig. 3a, two of the curves drawn with divide region M1 and M2. Due to the workfunction applied in region M1 is lower than the M2 region and the lower band gap Si-Ge layer exists at the tunneling junction, the overall surface potential will get rises with respect to their original position. This happened due to the increase in percentage of the B2BT rate at tunneling interface. Our Forthcoming Fig. 3b showing the perfect match between the obtained result of surface potential from the sentaurus TCAD simulations with reference to

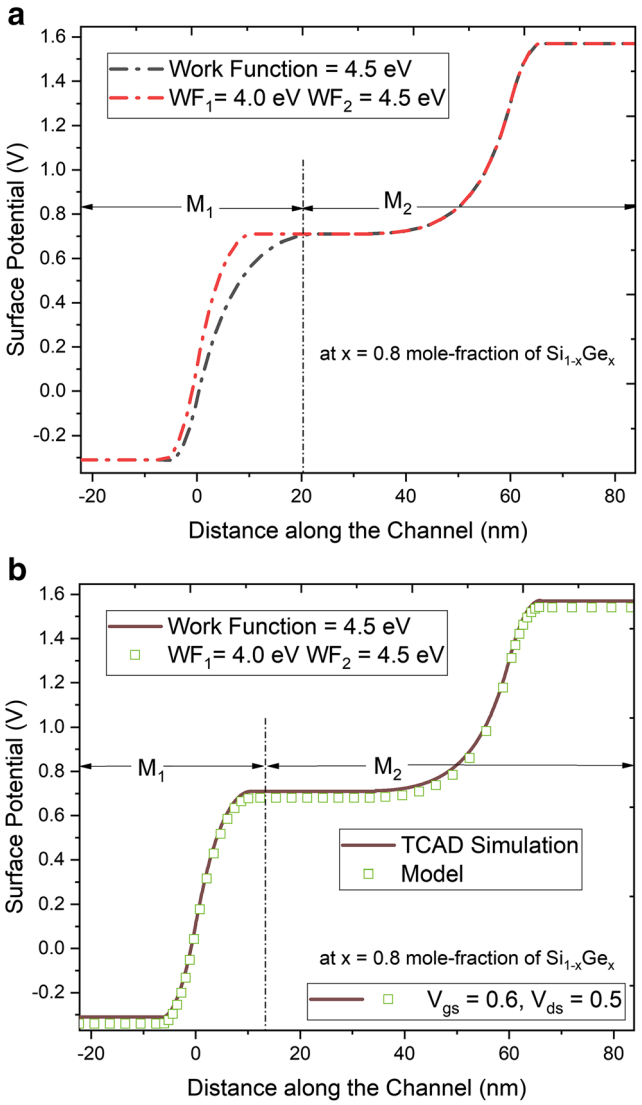

Fig. 3 **a** Surface potential variation as a function of Gate metal work function at region M1 along with device channel length at V_{GS}=0.6 V, V_{DS}=0.5 V through Si-Ge mole-fraction at x = 0.8 V. **b** Calibration to derived model results with the TCAD simulation

computation analysis. Moreover, the obtained potential is proportionally dependent on the gate biasing and get saturates for the drain biasing. This properties of the Dual material Gate Vertical tT-FET will come out with the higher output resistance and utilized for low power circuit analysis [5, 15].

2.2 Gate regulation in the channel surface potential

Figure 4 analyze the variation of channel surface potential with respect to gate bias voltage from 0.6 to 0.9 V at constant drain bias 0.5 V. The device surface potential for low gate voltage obtained the linear relationship with V_{GS}. The surface potential will therefore become saturated at the potential for high gate voltage $\varphi_{ch,sat}$ and becomes independent of the V_{GS}. The inversion charge mode would screen the surface potential

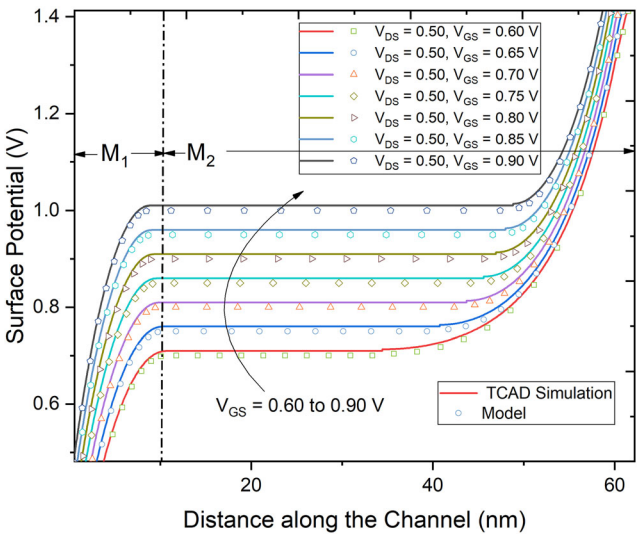

Fig. 4 Variance of channel surface potential as a function of gate biasing voltage for V_{DS} = 0.5 V and a comparison of TCAD simulation results with our model

from additional bending due to the identical nature of MOSFET's strong inversion mode.

It's quite different to measure band twisting with respect to DMG V tT-FET. Initially, the related value of inversion charges density N_{INV}, that is same as the channel doped concentration N_{CH}, is relatively low for effectively monitoring the gate-modulation when surface potential approaches because of low channel doping device $2\varphi fp$. φfp is well-defined possible difference among Fermi-intrinsic potential E_{fi} and Fermi-hole potential E_{fp} defined as $ln(N_{CH}/n_i)kT/q$. The surface potential would increase steadily, even after $\varphi chc = 2\varphi fp$, Unless and until ample voltage of the inversion charge exists that can effectively screen the gate modulation. The screening parameters for the modulation gate changes consequently from $\varphi_{ch,sat} = 2\varphi fp$ (MOSFET) to $\varphi_{ch,sat} = \phi$ (DMG Vertical t T-FET), in which ϕ represents the potential that needs ample of inversion charge in respect of tracking the gate-modulation.

$$\phi = \left(\frac{KT}{q}\right)\ln\left(\frac{N_{CH}N_{INV}}{n_i^2}\right) \tag{51}$$

Where n_i is the silicon intrinsic carrier concentration, N_{CH} is channel doping concentration, N_{INV} is inversion charges density.

By the method of homogeneous differential equation, this equation can be solved by the virtue of two boundary conditions of the source-channel region must be balanced and called for depletion width solution as L_1 and L_2. The surface potential needs to be calculated correctly, since the formula is generated to measure the device's drain current. This paper therefore includes both the biased voltages effect on gate drain terminal, referred to as dual modulation effect. The gate-

controlled inversion charge layer consider to be marginal in respect of associating the surface potential to the field as

$$\varphi_{ch,sat} = \left[\sqrt{V_{GS}-V_{FB}+\frac{\gamma^2}{4}}-\frac{\gamma}{2}\right]^2 \quad (52)$$

The concluded research with the help these equations produced efficient results with respect to the TCAD simulation results.

2.3 Drain regulation in the channel surface potential

The surface saturation potential depends upon the drain-bias, however, the equation described hereafter provides migration of the device control from gate to drain, whereby γ represents the body-factor and termed as $\sqrt{2E_{si}qN_{ch}/C_{ox}}$ where, V_{FB} is a flat band voltage.

$$V_{TR} = V_{FB} + V_{DS} + \phi + \gamma\sqrt{V_{DS}+\phi} \quad (53)$$

Once this voltage reached by V_{TR}, the channel will be control by the drain biasing regulation. Figure 5 illustrates, the drain difference in respect to surface potential. From figure, the device surface potential is linearly associated with V_{DS} (drain-bias voltage) fluctuating range of 0.45 V to 0.70 V at constant V_{GS} (gate bias voltage) of 0.8 V. Furthermore, with the increase in the range of V_{DS} voltage, the transition condition will get fulfilled and device will get more projected by the gate voltage and thus control by the gate terminal. Therefore,

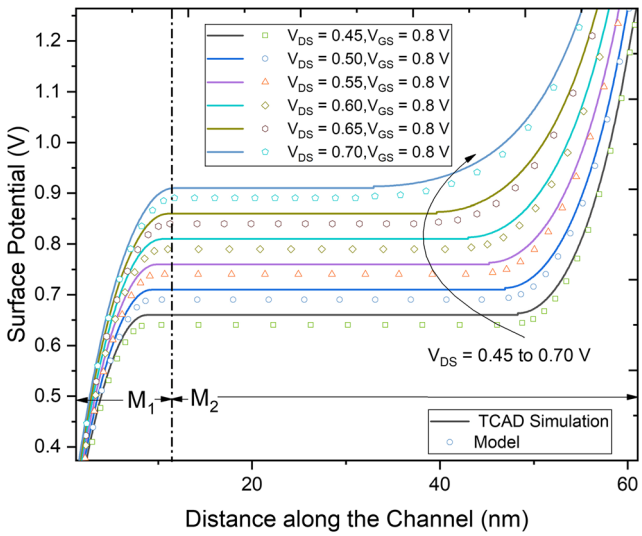

Fig. 5 Variance in channel surface potential as a function of drain-source voltage for fixed V_{GS} = 0.8 V and a comparison of TCAD simulation results with our model

the device surface potential is becoming independent of drain biasing.

Therefore, the device's potential become saturated with output of tunneling width and the device current. As a consequence of the changeover from drain to gate control, the drain-saturation voltage can be express as:

$$V_{DSs} = \left[\sqrt{V_{GS}-V_{FB}+\frac{\gamma^2}{4}}-\frac{\gamma}{2}\right]^2 - \phi \quad (54)$$

From the above discussion, it can be inferred that the surface potential of the system is alternatively regulated by V_{GS} (gate-source voltage) and V_{DS} (drain-terminal voltage) in the gate-drain control regime correspondingly. This changes from one region to another must be handled carefully and this whole setup of device potential via two terminal voltage is called the dual-modulation effect DMG V tT-FET device. Transition point inversion charges cannot fully monitor the gate modulation, hence the device's potential slightly upsurges, as revealed by slight slope increase in the result.

2.4 Derived model results validation

Additionally, observations were obtained by evaluating other parameters like variation in mole-fraction, gate oxide thickness, metal gate workfunction along with different dielectric constants. Such improvements are part of dual gate metal workfunction and material engineering community to enhance ON current of the system. The outcomes of the resultant model are approximately in good alignment to the TCAD simulated one. Firstly, test the molefaction consequence (x) of $Si_{1-x}Ge_x$ in device's potential using (34) and (35) with different gate metal workfunction M_2 considering all parameters identical excluding subsequent values of Electron affinity, Energy Band Gap and permitivity of Si-Ge represent by (χ_{SiGe}), (E_G) and (ε_{SiGe}). In Table 2, relevant parameters derived using different mole-fraction. Figure 6 demonstrates that the Germanium percentage will rise proportionally with the increase in Si-Ge's mole-fraction as a result of which the efficient energy bandgap will decrease. The results proportionally

Table 2 Values for different mole-faction (x) of $Si_{1-x}Ge_x$ material

Mole Fraction x	χ_{SiGe}	ε_{SiGe}	E_{SiGe}
0.4	4.036	13.576	1.0205
0.5	4.029	13.968	0.9860
0.6	4.024	14.389	0.9734
0.7	4.019	14.834	0.9576
0.8	4.011	15.241	0.9385

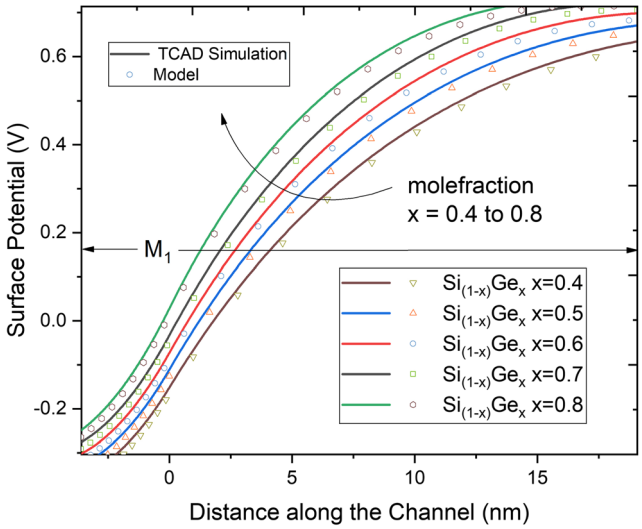

Fig. 6 Channel Surface Potential variability due to variability in Si- mole-fraction *x*-imposed material for V_{GS} = 0.8 V and also showed a comparison of TCAD simulation results with our model

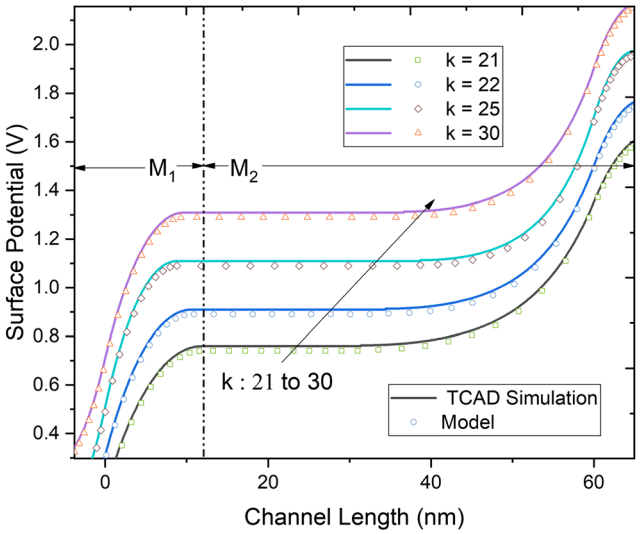

Fig. 8 Channel surface potential variation as a function of dielectric for V_{GS} = 0.6 V, V_{DS} = 0.5 V and a comparison of TCAD simulation results with our model

increases the device potential at the source channel interface. The bandgap deceases from 1.0205 to 0.9385 eV for the 0.4 to 0.8 mol-fraction.

In Fig. 7, device's potential shows the gate oxide (HfO_2) thickness variation from 5 nm to 2 nm. The oxide generated capacitance shows the inverse relation regarding the device's oxide thickness (T_{ox}) according to the analyzes performed. This result concludes the overall performance better with decrease in oxide thickness.

Analysis of channel surface potential as a function dielectric constant, considering all the parameters of the device remain unchanged. With the outcome results shown in Fig. 8, the dielectric constant can be clearly shown to be related exponentially to the surface potential of the device [10]. High k dielectric constant comes with their own advantage. The equivalent oxide thickness decreases without actual reduction of the oxide width thickness. We have taken HfO_2 as an oxide thickness material for implementation. However, after some extinct it cannot be reduced to avoid direct tunneling.

In the subsequent study, as we increase metal gate working function, the device tends to convert p-type. Therefore, if the workfunction for the n-type device will increase linearly, then output of the n-DMG V tT-FET will inhabited and this will lead to a reduction in surface potential of the device [28]. Two

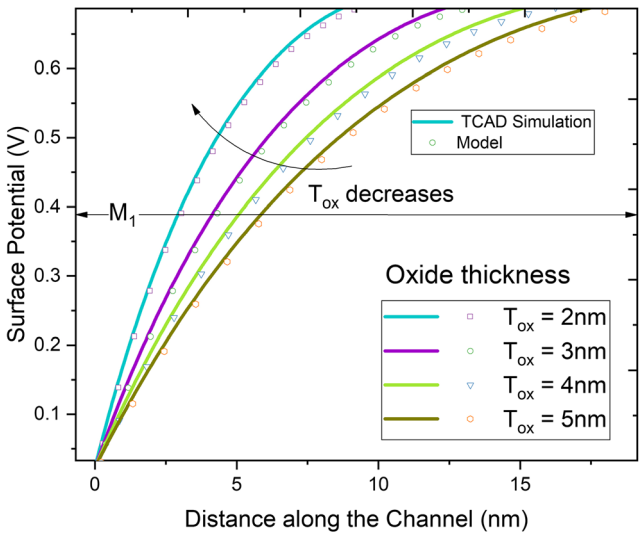

Fig. 7 Channel surface potential variation as a function of gate oxide thickness for V_{GS} = 0.6 V, V_{DS} = 0.5 V and a comparison of TCAD simulation results with our model

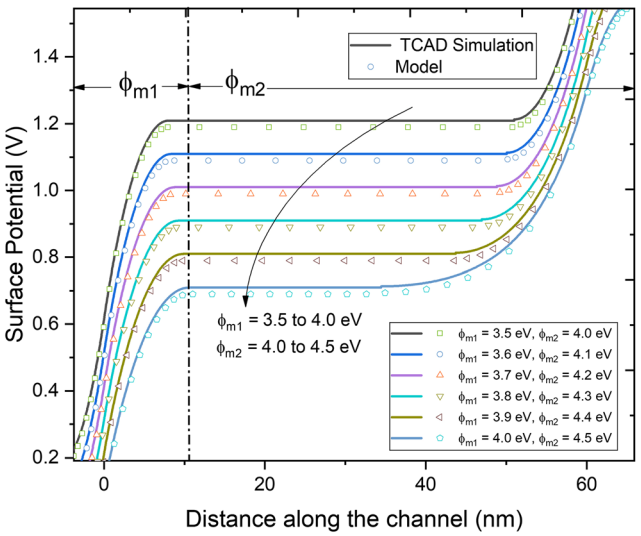

Fig. 9 Variation of channel surface potential as a function of dual workfunction at M1 and M2 for V_{GS} = 0.6 V, V_{DS} = 0.5 V and a comparison of TCAD simulation results with our model

metal gate workfunction ϕ_{m1} and ϕ_{m2} at M_1 and M_2 named as tunneling gate and auxiliary gate are optimize at 4.00 eV and 4.5 eV respectively. Increasing M_1 from 3.5 to 4.0 eV and M_2 from 4.0 to 4.5 eV will cause the device properties consisting of a greater number of hole charges which will impede the tunneling interface at source-channel junction and in the vice-versa condition, the surface potential will get increase as there are a greater number of charges carries. In Fig. 9 below, the TCAD simulation and model plot are assembled and viewed as a reference.

In nanoelectronics era, the silicon material widely used as a compound for the fabrication of the various evaluated device. But still there is lot more to improvement required in the field of TFET to enhance the ON-state current. So, in this particular order many of the semiconductor compound has been investigated to overall minimize the band gap occur at the tunneling junction. However, there some consequently effect to the device which increase the OFF current as well which causes the leakage current. In order to come out with a solution to this trade-, one has look forward for the composite mixture of two or three elements which are called binary compounds. In our proposed model, we have introduced the Si-Ge compound material at the tunneling junction with different gate metal workfunction which will enhance the device characteristics. We have also consequently proposed and modeled the device with different material like GaAs, InGaAs and InAs. Among all mention compunds, the InAs of the DMG V tT-FET device is found to be the highest tunneling medium as it consists of the lowest bandgap values of 0.35 eV and can be utilize for the further research [14, 19]. The reason behind using these compounds is the direct bandgap tunneling as compared to the silicon which consist of the indirect band gap tunneling. The compared relation with the modeled plot of the different material with the TCAD simulation is shown in Fig. 10.

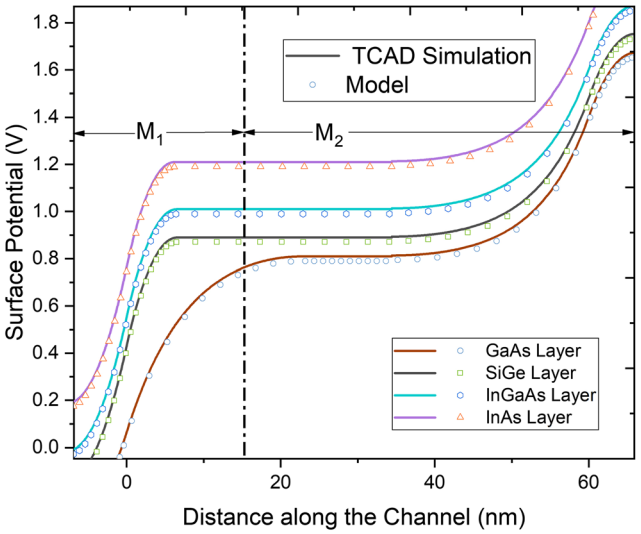

Fig. 10 Channel surface potential variation as a function of different compound material for V_{GS} = 0.6 V, V_{DS} = 0.5 V and a comparison of TCAD simulation results with our model

3 Derived Drain Current MODELLING

The derived current modeling of Si-Ge built DMG V tT-FET is based on the principal of the band 2 band tunneling process. The flowing current I_{DS} is transmitted form the source's valance band to the conduction band of the channel. The generated current will involve the effect of the different metal workfunction with introduced Si-Ge layer. The Kane model is used for calculating the tunneling generation rate (G_{B2BT}) [30]. The accumulated drain current is calculated by the band 2-band generation rate per unit volume of the device being implemented.

Hence,

$$I_{DS} = \mathrm{q}\iint G_{B2BT}\,dudv \tag{55}$$

The Kane Model is used to measure the generation rate of tunnels (G_{B2BT})

$$G_{B2BT} = A\frac{|E|^{2.5}}{\sqrt{E_{SiGe}}}exp\left[-B\frac{E_G^{3/2}}{|E|}\right] \tag{56}$$

Where E_{SiGe} with a mole fraction of 0.8 is the energy bandgap for Si-Ge material. The magnitude of the electrical field is defined as $|E| = \sqrt{E_u^2 + E_v^2}$ and the variables A and B are the configuration parameters taken as an default values of $A = 4.0 \times 10^{14}\ cm^{-3}\ s^{-1}$ and $B = 1.90 \times 10^7$ V/cm respectively [23]. Distribution of electric field along with channel length

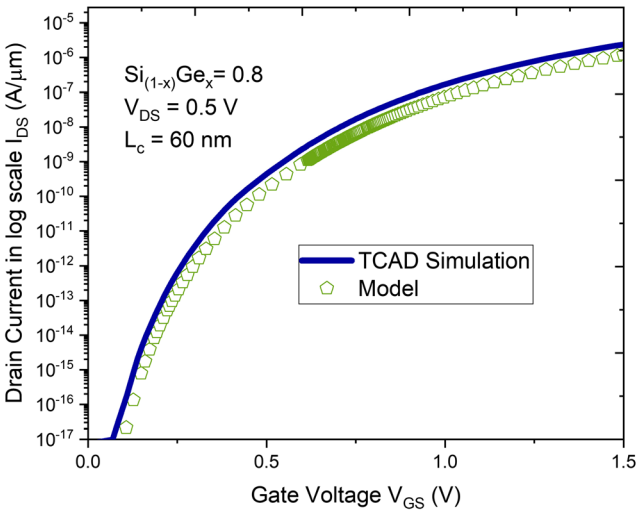

Fig. 11 Transmission curve of drain current $log(I_{DS})$ vs gate voltage (V_{GS}) for TCAD simulation and compared model consisting of channel length 60 nm at V_{GS} = 0.6 V and V_{DS} = 0.5 V

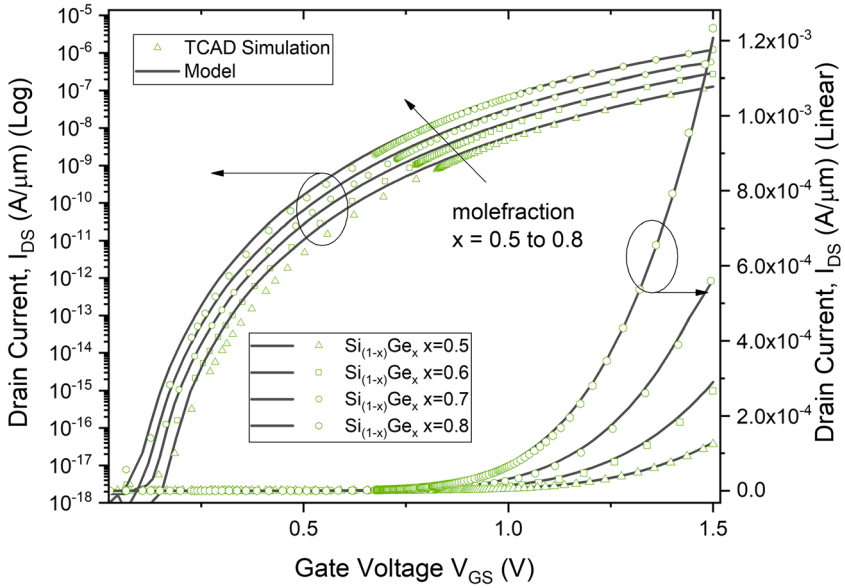

Fig. 12 Variation in the drain current $log(I_{DS})$ versus gate voltage (V_{GS}) of DMG V tT-FET at V_{DS} = 0.5 V for different mole-fraction of the Si-Ge Material for TCAD simulation and compared model

can be obtained through the differentiation of the surface potential. The vertical electric field E_u and lateral electric field E_v are given by

$$E_u(u,v) = -\frac{\partial \varphi_i(u,v)}{\partial u} \tag{57}$$

$$E_v(u,v) = -\frac{\partial \varphi_i(u,v)}{\partial v} \tag{58}$$

Figure 11 shows the characteristics of the drain current $logI_{DS} - V_{GS}$ derived by proposed model using (55) with V_{DS} = 0.5 V and V_{GS} = 0.6 V. The device's Subthreshold Voltage (V_{th}) is drive via constant current method and reported to be 0.262 V. In the next, Fig. 12 shows the variation of drain current characteristics with respect to the Si-Ge mole-fraction x from 0.50 to 0.80. Such statistics also provide a contrast between simulated outcome and analytical method. It must be said that the obtained drain current result from the derived model are in well correlation with the TCAD Simulation one.

4 Conclusion

A compact 2D analytical modelling and simulation of Si-Ge hetero-junction Dual Material Gate Vertical t- shape T-FET is introduced in this paper. The proposed model is in the good agreement between the results obtained from the TCAD simulation as a function of gate bias and drain bias voltage. All the derived equation and depletion length obtained from the above model is optimized at the 0.8 mol-fraction of Si-Ge material at V_{GS} = 0.6 V, V_{DS} = 0.5 V. Dual material concept is introduce to the device in respect to improve the device performance. The divided region of M1 is known to be tunneling gate which is kept lower than M2 as an auxiliary gate. The depletion length L_2 (Si-Ge layer) of tunneling interface will get reduced from 27.01 nm to 10.55 nm as compared to silicon device. The depletion length L_1, L_2, L_3 and L_4 is calculated to be 6.49, 10.55, 25.75 and 6.02 nm for the region G1, G2, G4 and G5 respectively. The initiation of the energy band reduces from 1.1 eV to 0.7 eV with the development of the Silicon-Germanium mole-fraction along with the use of the specified metal gate workfunctions. Thus, the ON-state current will get increase along with device's surface potential due to the increase in the B2B tunneling generation rate. Finally, we come out with the expression of Si-Ge embedded channel surface potential which will vary in accordance with the gate and drain biasing. Kane model is therefore used for driving the drain current under the assumption that the electric field will remain constant throughout the tunneling path. The model results are found to be in good agreement with the TCAD simulation results.

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