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ORIGINAL PAPER

# Growth and Characterization of Undoped Polysilicon Thick Layers: Revisiting an Old System

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## Abstract

Thick layer of polycrystalline silicon (poly-Si) grown by Atmospheric Pressure Chemical Vapor Deposition (APCVD) is still a reference material in a number of applications, despite the high thermal budget of this technique. This work presents a material study of undoped poly-Si layers of different thicknesses, using different characterization techniques such as secondary electron microscope in backscattered detection configuration, electron backscattering diffraction imaging, secondary ion mass spectrometry and spreading resistance profiling. The poly-Si layers, grown at 1000 °C by APCVD on thermal oxide, were found to have a columnar microstructure with [110] main orientation. By correlating layer purity, grain size and electrical resistivity, no straightforward relation between grain size and resistivity could be found. The layers resistivity is found almost independent on thickness and thus grain size. The possible reasons for such difference with previous other works are discussed taking into account the grain size determination uncertainty and the electrical characterization limitations.

**Keywords** Silicon · Polycrystalline material · CVD · Microstructure · Resistivity · Backscattered Electron

## 1 Introduction

Polycrystalline silicon (poly-Si) is a mature material, fully compatible with Si technology and thus, is used in a variety of electronic applications such as photovoltaics [1, 2], the well-established transistor industry [3, 4] or in MEMS [5]. For all these applications, poly-Si grain size, microstructure and grain crystallographic orientation are of importance [6–8].

For applications needing defined-grain, poly-Si can be obtained by annealing of an amorphous deposit or by a direct deposition of a polycrystalline layer. The latter process is preferentially performed by chemical vapor deposition (CVD) as it is well controlled, leading to high purity layers and offering high growth rate [9]. Moreover, if the deposition temperature is high enough (like for atmospheric pressure (AP) CVD), grain size evolution during subsequent high-temperature processing steps such as thermal oxidation, dopant diffusion annealing or even metal contacting, should be avoided [10, 11].

Deposition of doped or undoped polysilicon by CVD has been extensively studied in the last 40 years for obtaining material with controlled resistivity [9, 12]. For undoped materials, the resistivity was shown to depend essentially on grain size [13, 14]. However, the high resistivity ($> 10^4$ Ω.cm) of these grown layers induces difficulties in characterizing them. For instance, using standard van der Paw configuration for Hall effect measurement is not straightforward for such highly resistive materials [15]. Also, charging under scanning electron microscope (SEM) is important and can be detrimental to resolution. Nowadays, in-depth resistivity measurement using Spreading Resistance Profiling (SRP)

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[16] has become an industry standard, while the SEM apparatus have considerably evolved with the possibility of having crystal orientation contrast using backscatter electron (BSE) configuration [17] or even imaging the crystalline orientation at the surface using electron backscattering diffraction (EBSD) [18, 19]. After a study of the growth of undoped polycrystalline layers on $SiO_2$/Si by APCVD, the present work will focus on both surface and cross-section poly-Si deposit characterization using updated and improved SEM and EBSD techniques for deeper insight, for instance on the layer texture and its relation with material purity and resistivity.

## 2 Experimental

Polysilicon layers were deposited by APCVD in a cold-wall, vertical reactor configuration using up to 10 sccm of $SiH_4$ diluted in up to 16 slm $H_2$ carrier gas. Substrates were standard n-type Czochralski Si(100) wafers with 400 nm thermal $SiO_2$ on top. They were placed on a SiC-coated graphite susceptor and loaded inside the reactor through an argon filled load-lock. Prior to Si deposition, the substrates were in-situ cleaned under $H_2$ at 1000 °C for 5 min. This step etches only slightly the oxide layer allowing thus to start the poly-Si deposition on such amorphous material, by just adding silane to the gas phase. Most of the depositions were performed at 1000 °C, while few of them were performed at lower or higher temperature, in the 760–1300 °C range. For temperatures >1000 °C at which $SiO_2$ etching may be aggressive, the temperature was first decreased down to 850 °C for depositing a ~160 nm thin buffer layer before fast increase of the temperature (6 °C/s) to the targeted deposition plateau.

The as-grown poly-Si surface morphology was characterized by SEM (Zeiss Merlin Compact) and Atomic Force Microscopy (AFM) using Nano-Observer apparatus in resonant mode (CSI Instruments). Qualitative analysis of grain orientation were acquired on polished poly-Si deposit (both on the surface and cross-section), using SEM Backscattered Electron Detector (BSE-SEM). For that, the samples were polished by standard chemico-mechanical polishing with abrasive powder of grain size down to 1 μm and silica finish for the last polishing step. The BSE-SEM images were acquired with 15 kV and 10 kV acceleration voltage respectively for surface-polished ~8 μm poly-Si deposit (pixel size of 5 nm) and cross-section polished poly-Si deposit (pixel size of 20 nm for ~8 μm deposit and pixel size of 40 nm for ~16 μm deposit). Quantitative EBSD analysis was performed on top of the same, ~8 μm surface-polished poly-Si deposit, using Nordlys detector from Oxford Instruments. The texture map was acquired with 10 kV acceleration voltage, 329.9 Hz acquisition speed and 20 nm step size, which resulted in 70.4% indexing rate. Obtained texture maps were denoised and analyzed with Tango component of HKL Channel 5 software. The denoising procedure consisted in wild spikes removal, zero solution extrapolation and grain fill with average orientation. Global poly-Si deposit texture was verified by Powder X-ray diffraction (XRD) from PANalytical X'pert. The layer resistivity was measured by Spreading Resistance Profiling (SRP) technique with depth resolution of ~160 nm while conductivity type was determined by hot-point-probe technique.

## 3 Results

The growth kinetics as a function of temperature was firstly studied in order to estimate the growth regime governing the deposition process in the used APCVD system. As shown in Fig. 1, the two classical growth regimes can be easily identified: the surface-reaction limited regime at low temperature with activation energy ($E_A$) of 2.28 eV/atom and the mass-transport limited regime at high temperature with $E_A$ of 0.35 eV/atom. All these results are in agreement to the reported for Si deposition from the $SiH_4$ source [20, 21]. The transition between the two regimes was extrapolated at ~860 °C. Since most of the deposition experiments were performed above 880 °C, the polysilicon layers grown in this work are essentially governed by the mass transport of $SiH_4$ through the boundary layer.

The growth temperature of 1000 °C, which is clearly in the mass-transport limited regime, was chosen for subsequent analysis of poly-Si grains size as a function of layer thickness. Typical as-grown morphologies for three different thicknesses are shown in Fig. 2. The deposits are polycrystalline and composed of a dense network of grains which do not display obvious faceting. The lateral grain size enlarges when

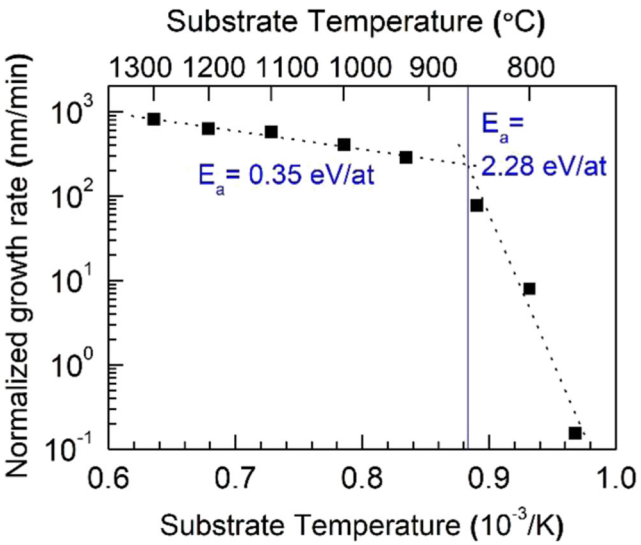


**Fig. 1** Evolution of poly-Si growth rate as a function of temperature using 5 sccm of SiH4. The dotted lines are guidance for eye

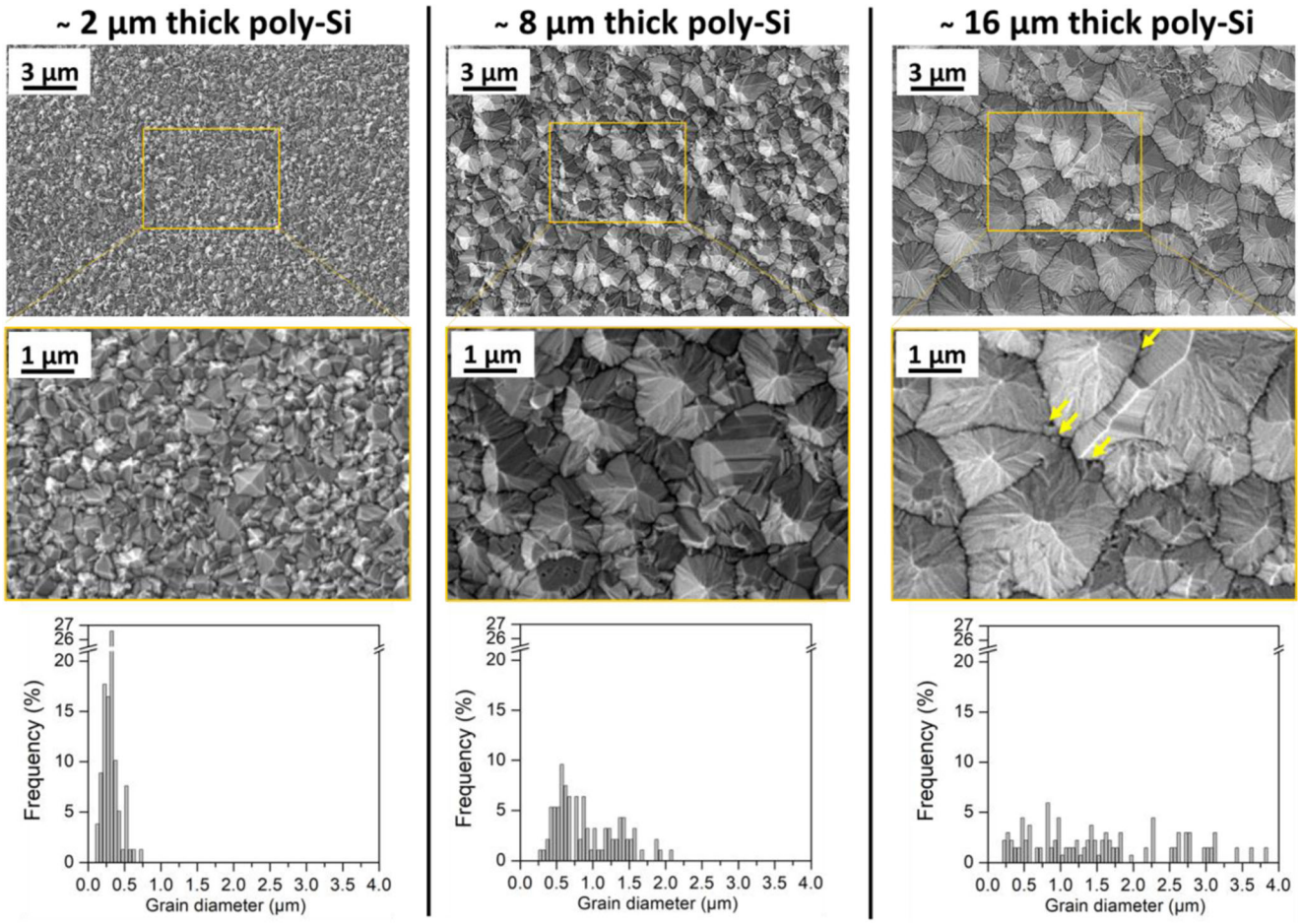


**Fig. 2** SEM images of as-grown poly-Si layer surface morphologies for three different layer thicknesses: 2, 8 and 16 µm. The histograms below are the corresponding populations of grains (with 50 nm resolution) calculated from these images. The arrows on 16 µm layer image show small grains presumably originating from secondary nucleation and contributing to the low values of the grain diameter histogram

increasing layer thickness. This trend is better illustrated in Fig. 3a. Increasing film thickness increases also the dispersion of the grain size (see grain diameter distribution histograms of Fig. 2). The orientation texture of such microstructure was analyzed by XRD. To avoid the response from the (100) oriented substrate and thus have a reliable estimation of the amount of (100) crystallization inside the poly-Si layer, a standard layer was deposited on unconventionally oriented Si(1011) wafer. The XRD spectrum recorded on such layer is shown in Fig. 4. The polycrystallinity of these layers is

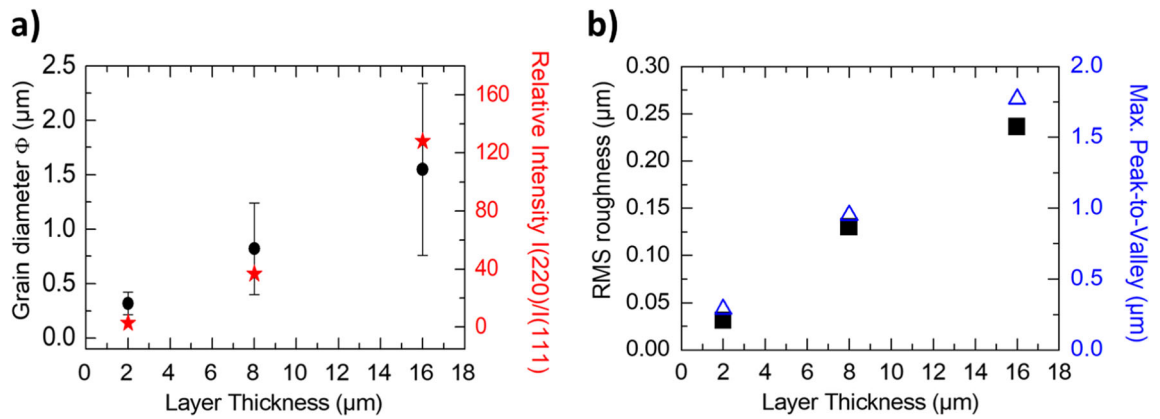


**Fig. 3** Grain dependent parameter variation for increasing polysilicon deposit thickness for (**a**) correlation of grain size and relative intensity of (220) to (111) XRD peaks; and (**b**) correlation of RMS roughness with maximum detected Peak-to-Valley

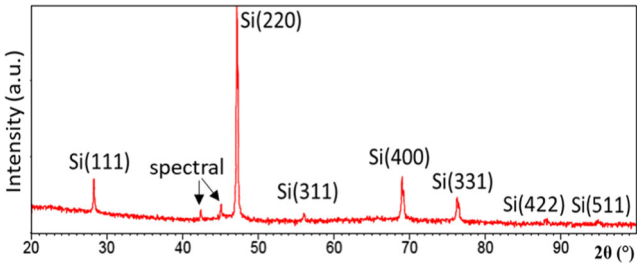


**Fig. 4** X-ray diffractogram of ~5 μm poly-Si deposited at 1000 °C on Si(1011) wafer

confirmed with the presence of the common peaks usually obtained for poly-Si. One can see the predominance of {110} peak together with equally intense {100} and {111} ones, similarly to [22] . Considering the usual (100) oriented wafers for which the (100) signal from the layer is overshadowed, we will assume that the relative intensity of (220) over (111) XRD peaks is an acceptable estimation of polycrystalline texturing of the layer. It was found that, with increasing film thickness, the poly-Si layers are getting mostly {110} textured, as can be seen from Fig. 3a. Such predominance of the {110} grains orientation with increasing thickness is a rather usual feature [22, 23] which shows that our growth conditions are standard. The grain size increase with layer thickness leads to an increase in surface roughness as shown in the Fig. 3b.

In order to have a deeper insight on layers microstructure and grain evolution with thickness, ~8 μm and ~16 μm thick poly-Si layers have been cross-section polished and observed by BSE-SEM technique, see Fig. 5a, b respectively. Both layers show similar microstructures composed of small grains close to the oxide interface, which progressively enlarge when moving to the surface (as indicated for thicker deposit, by the dashed guiding lines). Considering above XRD results, this gradual grains enlargement suggests a progressive <110> texturing of the layers with increasing thickness. Nevertheless, each grain contains a very high density of elongated crystalline defects (probably stacking faults and microtwins) almost parallel to the growth direction, as reported previously [22]. Note that the orientation contrast obtained from BSE observation is rather different from grain to grain, which suggests that the <110> oriented grains are probably in-plane rotated one to each other, which is expected from a random nucleation on an amorphous material. Additionally, one can appreciate a good feature resolution which is usually obtained in transmission electron microscopy imaging alike in [2].

EBSD mapping can give complementary and quantitative analyses of the deposit's microstructure. To obtain an information corresponding to ~8 μm thick poly-Si, the surface of an equivalent sample of ~10 μm thick poly-Si layer was mirror polished, with a ~2 μm thickness removal. This will not necessarily lead to the exact same microstructure as for the as-grown ~8 μm thick poly-Si deposit but it will be an interesting point of comparison. BSE-SEM images taken on such polished surface (Fig. 6a) displayed very clear orientation-induced contrasts from grain to grain, with additional contrast lines inside the grains which are caused by the extended crystalline defects. It thus allowed more accurate determination of the grains size. The mean value of the grains size was now found to be 1.19 ± 0.61 μm which is in fact higher than the value of 0.82 ± 0.42 μm found for as-grown surface and corresponds to the reported values for similarly thick polysilicon layers grown by APCVD [2, 22]. Our surface polishing step was also found good enough for EBSD imaging (see Fig. 6b). As a first conclusion from this figure, it is clear that (110) is the main crystalline orientation of the grains. We limited the texture detection to (110), (100) and (111) orientations, with information on their misorientation up to 20% compared to the growth direction. Looking at the corresponding inverted pole figure in Fig. 6c, one can clearly see an important misorientation or even scattering of data points corresponding to grains. This can be assigned to the presence of other planes, such as (311) and (331) planes

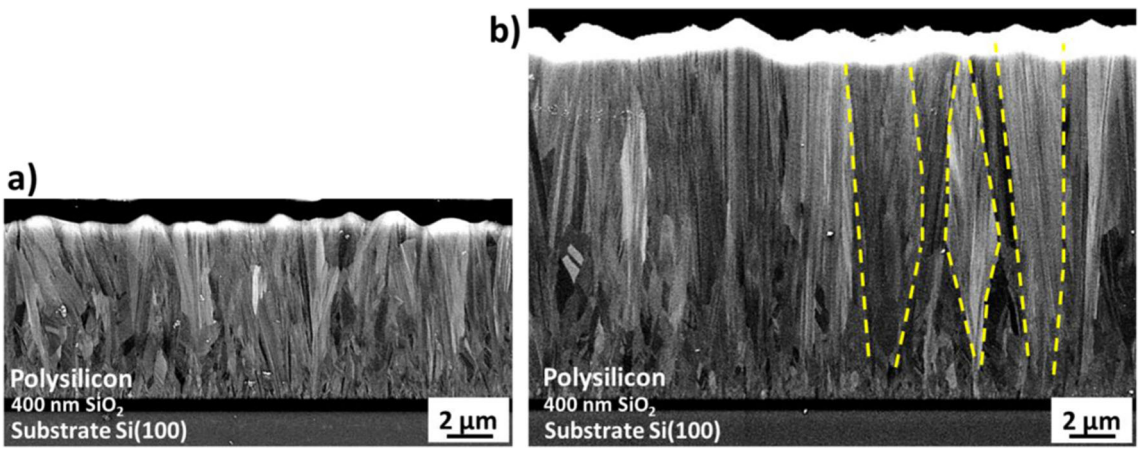


**Fig. 5** BSE-SEM cross-sectional image of (**a**) ~8 μm and (**b**) ~16 μm polysilicon deposit. The dashed line are guidance for eye of the grain progressive enlargement

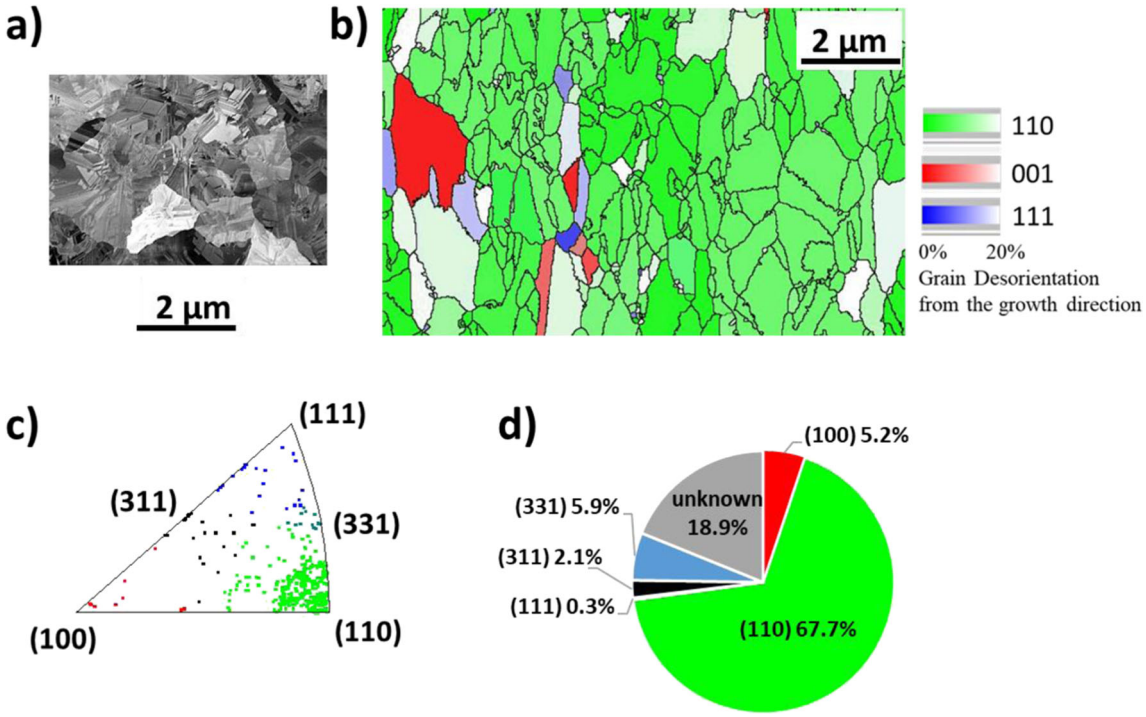


**Fig. 6** (**a**) BSE-SEM observation of ~8 µm poly-Si polished surface; (**b**) denoised EBSD orientation mapping of the same sample but in another area with corresponding (**c**) Inverted Pole Figure with visible 20° grain misorientation. (**d**) Additionally, the grain size area distribution calculated from crystallographic plane with misorientation narrowed to 10° is shown. The color-code corresponds to crystal direction perpendicular to the polysilicon surface

that can be also seen in XRD diffractogram. Indeed, when the misorientation detection from the growth orientation is limited to 10°, the total area can be divided into additional orientations (Fig. 6d). The box chart drawn in Fig. 7 shows the grain size population in the same inspected sample but obtained using different characterization techniques. Since grains are not circular, each grain size corresponds to the diameter of a circle having the same area as the grain. Clearly, EBSD mapping gives lower values of grain size compared to manual counting on SEM in secondary electron detection configuration (SE-SEM) or BSE-SEM images. Since EBSD takes into account the local crystal orientation, the resulting grain size values should be considered as closer to the reality, even for denoised EBSD orientation map, where the grain diameter increases but still remains in a lower range.

Analyses of the data recorded in Fig. 6b allowed determination of the misorientation between the grains and thus determination of the type of boundary between them. As can be seen from EBSD map and corresponding graphical representation in Fig. 8, the most frequent misorientation is at ~60° which corresponds to Σ3 (111) twin boundary, which is in accordance with the numerous reports for highly-twinned poly-Si [19, 24]. Other small peaks are appearing at 38.5° and 49.5° which probably correspond to Σ9 and Σ11 respectively. The presence of higher level Σ9 boundary is expected since it is created when two Σ3 boundaries meet at a triple

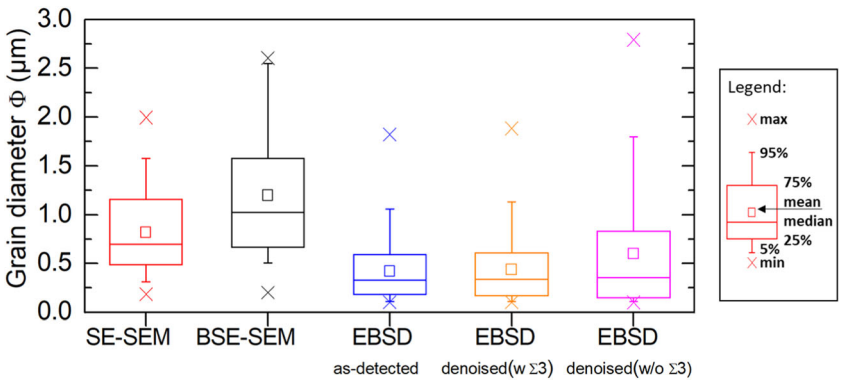


**Fig. 7** Box plot of grain diameter calculated at the surface of ~ 8 µm thick poly-Si for different surface preparation and imaging methods. For SEM secondary electron detection (SE-SEM) and BSE-SEM the grain diameter was detected manually and for EBSD, where the critical misorientation for defining the grain size was set to 10°

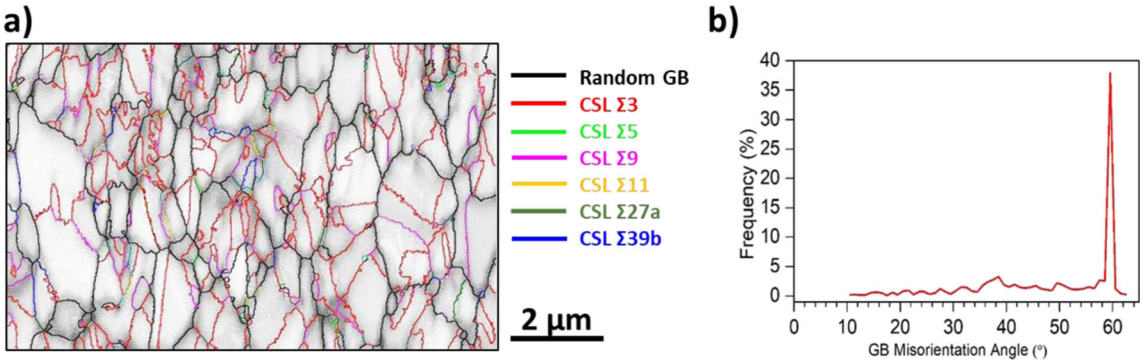


**Fig. 8** (**a**) Distribution of high-angle grain boundaries in the EBSD map shown in and (**b**) corresponding graphical representation with respect to the detected misorientation angle between the adjacent grains

junction. Note, that many intra-grain extended defects seen in BSE-SEM image of Fig. 6a were not detectable during EBSD imaging, which can be simply due to resolution difference of 5 nm and 20 nm respectively.

Coming now to the electrical properties of the polysilicon layers, Fig. 9 shows a typical resistivity depth profile obtained by SRP on a 16 µm thick poly-Si layer. One can clearly separate the contribution from the substrate (low resistivity $<10^2$ Ω.cm, right), the thermal oxide (high resistivity $>10^6$ Ω.cm, centre) and the polysilicon layer (left). The resistivity of the layer does not vary significantly along its depth and it is in the mid-$10^4$ Ω.cm range. P-type conductivity was found for the entire poly-Si layer, which is a common feature for its undoped form. According to previously reported data [13, 23], poly-Si resistivity in the mid-$10^4$ Ω.cm range should be doped in the mid-$10^{16}$ at.cm$^{-3}$ range. In order to check for possible non-intentional dopant incorporation during deposition, SIMS analysis was performed on 8 µm thick poly-Si layer. As shown in Fig. 10, the poly-Si layers are very pure since, the concentration of all the targeted impurities, i.e. B, P, N, C, O and H, inside the layer was found to be below the

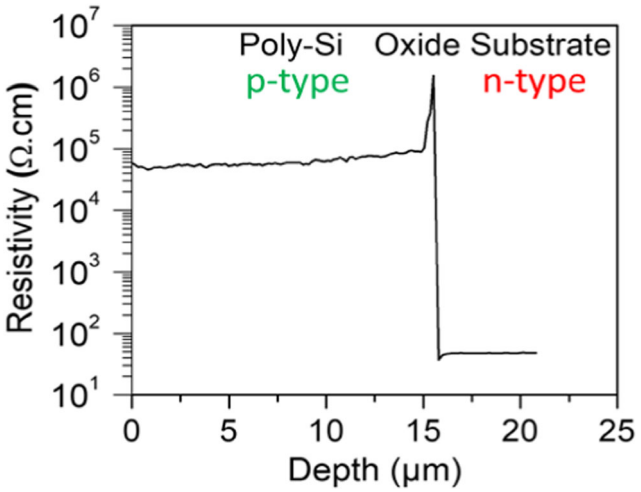


**Fig. 9** SRP profile showing resistivity evolution along thickness for a ~16 µm thick poly-Si layer grown in this study

detection limit of the apparatus. The concentration of the possible dopants B, P and N, are therefore all below $1 \times 10^{16}$ at.cm$^{-3}$ which does not correlate well with the literature. Note that the concentrations found inside the thermal oxide for all these elements are probably false due to different matrix effect.

## 4 Discussion

All the polysilicon layers deposited in this work have preferential {110} orientation, which is rather typical for APCVD growth and used growth conditions. This orientation selection should not come from the nucleation on the oxide which is supposed to be random. Due to the higher Si growth rate toward [110] direction, the grains with this orientation grow faster and thus enlarge at the expense of the others [22]. But the low angle conical shape of the grains along thickness suggest that this enlargement is not fast, so that very thick layers would be necessary to completely overgrow the other orientated grains. Note that the [110] oriented big grains (≥1 µm diameter) usually contain a high density of extended defects such as SFs, multiple microtwins and dislocations, which are dividing the effective crystalline grain size into segments of not more than 300 nm (see contrast at the BSE-SEM image in Fig. 6a), similarly to the TEM analysis shown in [22]. They may appear due to the stress accommodation in such columnar poly-Si microstructure.

However, despite following the usual growth trends, the values of the resistivity for poly-Si layers grown in this paper differ from literature. It is generally admitted that poly-Si resistivity depends both on layer purity and on the density of grain boundaries (and hence on the grain size) it contains [13, 23]. In our case, direct correlation with grain size is not straightforward since layers resistivity shows only an asymptotic decrease from the bottom ($8 \times 10^4$ Ω.cm) to the top ($5 \times 10^4$ Ω.cm) of the layer while grain size increases by a factor of ~4.5 from ~2 to ~16 µm thickness (Fig. 3a). Furthermore, the high purity of our layers, for the selected impurities, suggests

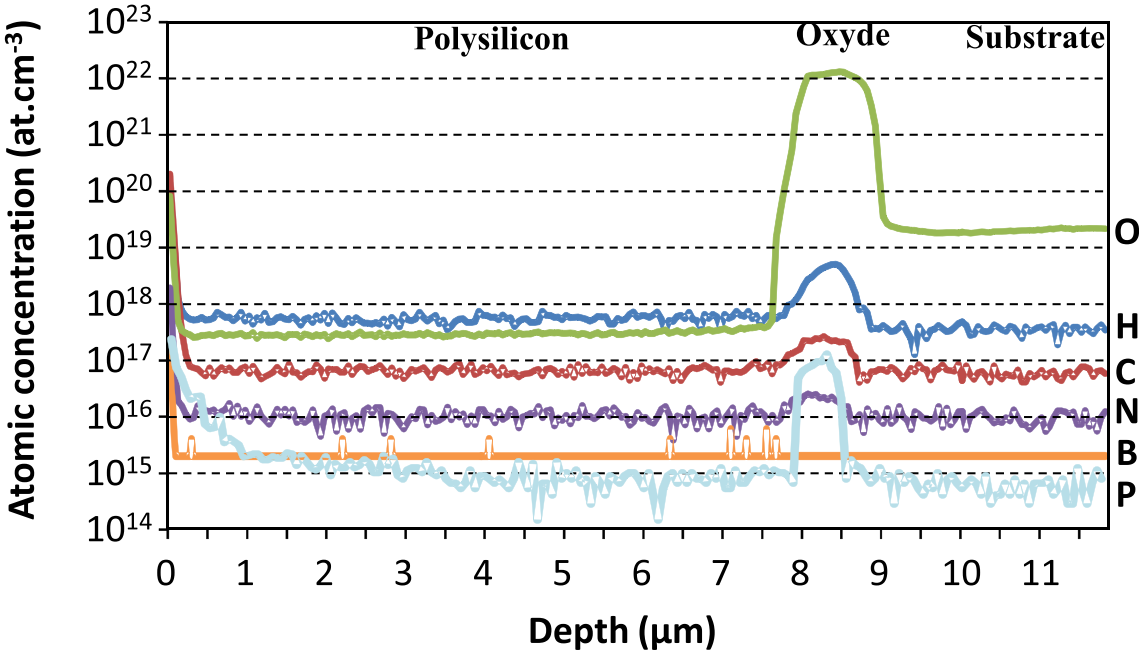


**Fig. 10** SIMS depth profiles for impurities (from bottom to top curve) P, B, N, C, H and O inside a ~8 µm thick poly-Si layer. All verified elements are below the detection limit of used SIMS apparatus. Note that the apparent concentrations of all these elements inside the thermal oxide should be considered with precaution due to different matrix effect

that any non-intentional doping induced effect could be neglected, even if, one cannot exclude an effect from another impurity than investigated ones. But, assuming no impurity-induced effect, the weak evolution of the layer resistivity with thickness is probably due to the fact that the effective grain size, as measured from surface morphology, is overestimated. BSE-SEM images and EBSD mapping revealed the frequent crystallites twinning caused by the presence of high density of intra-grain extended defects, such as higher order CSL boundaries and random grain boundaries, which led to smaller effective grain size, particularly at the surface of the thick layers. This could partially level off the resistivity value along the thickness. Our study suggests also that the grain size differs strongly as a function of detection technique and hence, drawing a correlation of resistivity with mean grain size can vary between the reports.

Another difference with literature is the mean value of resistivity achieved here which is lower of at least one decade compared to early reports mentioning values as high as $10^6$ Ω.cm [13, 23]. Again, assuming no impurity induced effect, such resistivity difference is difficult to understand unless coming from the measurements themselves. SRP technique is well suited for moderately resistive materials up to mid $10^4$ Ω.cm so that some errors can arise for more resistive materials. On the other hand, the electrical measurements reported in the literature, were usually performed using conventional Hall measurement in van der Pauw configuration. Recently, F. Werner suggested that such conventional Hall measurement, using a simple field-reversal technique, is often unsuited to obtain reliable results on low mobility materials such as polycrystalline ones [15]. The identified potential sources of error are the presence of the grain boundaries and the occurrence of multi-carrier conduction, both of which might yield low apparent Hall mobilities significantly underestimating the actual ones and thereby overestimating the resistivity values. We thus speculate that the difference in resistivities with literature could be due to uncertainties generated by both SRP and Hall effect measurement techniques.

## 5 Conclusion

In this paper, undoped poly-Si layers deposited on $SiO_2$/Si by APCVD were revisited for extensive appreciation of their microstructure and electrical properties. Using updated characterization techniques, it was found that determination of one of the most frequently discussed poly-Si parameters i.e. its grain size, is not as straightforward as previously reported due to the frequent material twinning. The mean grain diameter, which varies significantly depending on the characterization technique used, should not be shown separately from its variance. The nominally undoped layers grown in this study exhibit resistivity of a magnitude lower than the previously published values measured with Hall effect technique in van der Pauw configuration. Since no effect of non-intentional impurity incorporation was found, we speculate that this difference can originate from the measurement technique used. Moreover, given the grain size determination uncertainty, the frequently reported resistivity correlation with grain diameter should be considered with care.

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## Compliance with Ethical Standards

**Conflict of Interest** The authors declare no conflict of interests of any sort.

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