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ORIGINAL PAPER

Effect of Temperature on Reliability Issues of Ferroelectric Dopant Segregated Schottky Barrier Tunnel Field Effect Transistor (Fe DS-SBTFET)

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Abstract
This paper addresses reliability issues associated with temperature of Ferroelectric Dopant Segregated Schottky Barrier Tunnel Field Effect Transistor (Fe DS-SBTFET). The simulated results are compared with Dopant Segregated Schottky Barrier TFET (DS-SBTFET). This is achieved by varying the operating temperature from 300 to 500 K. DC parameters such as I_{ON}/I_{OFF} ratio, drain current characteristics and subthreshold swing (SS) for a range of temperature have been highlighted. Moreover, the influence of temperature on various RF figure of merits such as gate capacitance (C_{GG}), intrinsic delay, cutoff frequency (f_T) etc. have been investigated. The device linearity has been analyzed by considering the effect of temperature variation on linearity parameters like g_{m2}, g_{m3}, 1-dB compression point, VIP_2, VIP_3 and IIP_3. The device characteristics get upgraded by the increase in cut-off frequency and reduction in intrinsic delay at elevated temperature.

Keywords Schottky barrier tunnel FET (SB-TFET) · Dopant segregated (DS) · Schottky barrier height (SBH) · Negative capacitance (NC) · SS

1 Introduction

The obstacles associated with miniaturization of MOSFET have enforced the investigation of novel devices that operate on Band to band tunneling (BTBT) mechanism rather than thermionic emission [1–3]. In this regard, Tunnel Field Effect Transistors (TFETs) have gained the interest of the researchers due to the unique properties of such as sub-60 mV/decade subthreshold swing (SS), low I_{OFF}, and immunity against short channel effects. However, one of the major drawback of these BTBT based devices is low ON current (I_{ON}). In recent years Schottky Barrier (SB) Tunneling FETs (TFETs) have emerged as a strong candidate in the field of mixed mode and high performance applications [4–6]. To solve the issue of high source/drain (S/D) series resistance, doped (S/D) has been replaced by metal S/D [7]. These devices offer low thermal budget and have increased immunity to process variation. Moreover, the low contact resistivity of Metal S/D junctions have minimized the short channel effects [8]. To reduce the SB height (SBH) which limits the ON current, devices with dopants at metal-semiconductor interface also known as Dopant-Segregated Schottky FETs have become suitable candidates for low power applications. The presence of heavily doped Dopant Segregated Layer (DSL) at the S/D contact and channel interface improves the device performance by modifying the SBH and the tunneling width [9, 10]. To further upgrade the switching characteristics, Ferroelectric field effect transistors (FeFETs) with negative capacitance (NC) effect have been reported in literatures [11, 12]. The electric field at the tunneling junction enhances by the NC effect of the ferroelectric gate oxide. Various ferroelectric materials such as Strontium Bismuth Tantalate (SBT) [13], Barium Titanate ($BaTiO_3$) [11], Lead Zirconate Titanate (PZT) [14] have been analyzed recently. These materials have compatibility issues with silicon and their high dielectric constants put constraint on the scaling limit. HfO_2 doped with silicon have better interface properties with silicon and also have low dielectric constant.

For considering the reliability issues associated with temperature and to meet the requirements of devices with low-

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and high-temperature tolerance, the study of temperature affectability over the device performance is necessary. Moreover, to realize the transistors in circuits, analysis of RF performance is essential.

This paper reports a detailed analysis of temperature affectability on DC, RF and linearity performance of Ferroelectric Dopant Segregated Schottky Barrier (Fe DS-SB) TFET. A comparative study of various electrical parameters between Fe DS-SBTFET and DS-SBTFET without ferroelectric layer is presented. The rest of the paper is organized as follows. The design of the device structure and the simulation setup are described in section II. The outcomes of the work are discussed in section III and finally, section IV concludes the work.

2 Device Structure and Simulation Setup

The simulated structure of Fe DS-SBTFET is depicted in Fig. 1. The silicon channel doping concentration is 1×10^{17} cm^{-3}. The doping specifications of the source and drain ends are: P^+ DSL (1×10^{20} cm^{-3}) and N^+ DSL (5×10^{18} cm^{-3}) respectively. DSL layer length at both the ends is 2 nm. Negative capacitance effect has been considered to improve SS by implementing Si:HfO_2 ferroelectric oxide layer of thickness 6 nm. The various ferroelectric properties associated with 6 nm thickness of Si:HfO_2 film have been shown in Table 1. Various ferroelectric parameters considered for film thickness of 6 nm are as follows: Remanent Polarization (P_r) = 10.3 μC/cm^2, Saturation Polarization (P_s) = 10.5 μC/cm^2, Coercive Field (E_c) = 1.14 MV/cm and ϵ_r = 33.4. These parameters are chosen as per the experimental data for HfO_2 doped silicon film reported in [15, 16]. To reduce lattice mismatch, defects and leakage currents, a buffer (HfO_2) layer is sandwiched between silicon and ferroelectric oxide. Interdiffusion problems across both the materials is avoided by high quality interface provided by the buffer layer. By reducing the semiconductor/ferroelectric interface defects, buffer layer rules out the chemical reactions which leads to degradation of ferroelectric oxide and semiconductor properties [13, 17]. All the simulations have been performed using TCAD simulator [18]. To encompass carrier statistics, Fermi-Dirac distribution model have been employed using TCAD

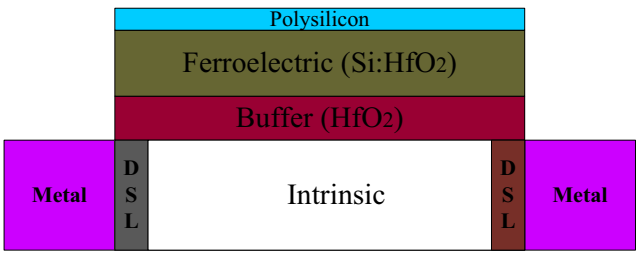

Fig. 1 2D structure of Fe DS-SBTFET

Table 1 Various ferroelectric properties of Si:HfO_2 film

Thickness (nm)	P_r (μC/cm^2)	P_s (μC/cm^2)	E_c (MV/cm)	ϵ_r
6	10.3	10.5	1.14	33.4

simulator. High doping concentration narrows the bandgap in a semiconductor. Thus, bandgap narrowing model (OldSlotBoom) has been invoked. Doping dependent mobility model has been activated, to signify the impact of different doping concentrations on carrier mobility. The significance of polarization effect in ferroelectric oxides has been considered by employing ENormal mobility model. By employing Hydro dynamic model, the impact of temperature variation on device performance has been analyzed. To handle interband tunneling, Schenk's band-to-band tunneling (BTBT) model has been activated. Shockley Read Hall (SRH) recombination model has also been employed. The proposed structure has no floating metal between the ferroelectric and the dielectric layer. Therefore, it is a distributed ferroelectric structure. The calibrated graph against the experimental models of source pocket device described in [19] has been depicted in Fig. 2. The model has been validated by considering identical doping parameters as in [19] with 0.1 μm channel length and gate length of 0.2 μm.

3 Result and Discussion

3.1 Temperature Affectability on DC and RF Performance

Figure 3 shows the effect of temperature on drain current of both FE DS-SBTFET and DS-SBTFET. It can be observed that drain current rises with temperature in both the devices. The superiority of SRH recombination at lower gate voltage results in large variation of drain current with temperature compared to the super threshold regime [20]. At lower gate voltage SRH recombination is exponentially related to

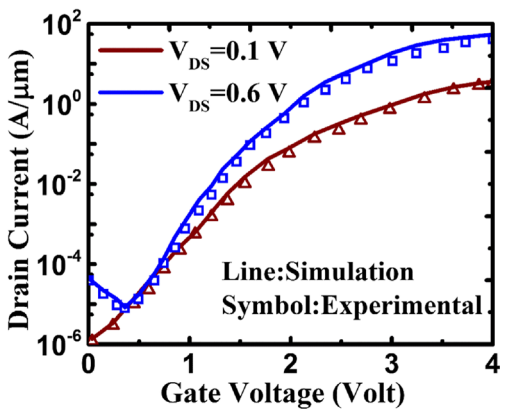

Fig. 2 Calibration of simulated graph against the models reported in [19]

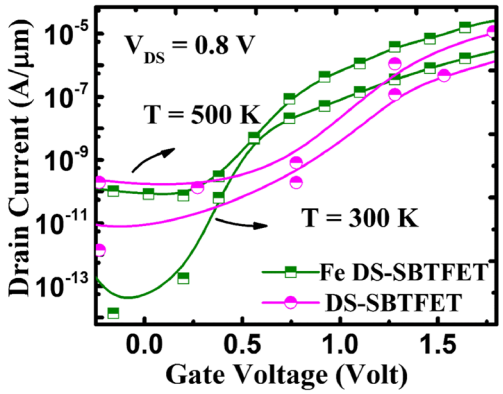

Fig. 3 I_D-V_{GS} characteristics of the proposed Fe DS-SBTFET and DS-SBTFET at $V_{DS} = 0.8$ V

temperature as [20]

$$R_{SRH} = \frac{pn - n_i^2}{\tau_p\left[n + n_i \exp\left(\frac{E_{TRAP}}{kT_L}\right)\right] + \tau_n\left[p + n_i \exp\left(-\frac{E_{TRAP}}{kT_L}\right)\right]} \quad (1)$$

Where the electron and hole lifetimes are ($\tau_p = 10^{-7}$ s) and ($\tau_n = 10^{-7}$ s) respectively, E_{TRAP} is the variation of intrinsic fermi level from trap energy and the lattice temperature in degree Kelvin is T_L.

However, there is a weak dependence of TFET on temperature due to BTBT conduction mechanism. At high temperature bandgap narrowing results in high tunneling current [21]. Bandgap (Eg) is related to temperature as

$$E_g(T) = E_g(300) - \frac{\alpha T^2}{T + \beta} \quad (2)$$

where $\alpha = 4.73 \times 10^{-4}$ eV/K and $\beta = 636$ K and Eg (300) = 1.08 eV for Silicon.

It is evident from Fig. 3 that FE DS-SBTFET provides high I_{ON} and low I_{OFF} compared to DS-SBTFET. In FE DS-SBTFET, Si:HfO_2 as ferroelectric layer amplifies the gate voltage which enhances the electric field and decreases the barrier width at the tunneling junction. Thus, the negative capacitance effect improves the ON current in the proposed ferroelectric device. The I_{ON} of Fe DS-SBTFET is 3.8×10^{-6} A/μm whereas for DS-SBTFET it is 1.2×10^{-6} A/μm at 300 K. The proposed device provides better results even at high temperature. The comparison of I_{ON}/I_{OFF} ratio and subthreshold swing (SS) of both the devices at various temperatures is shown in Table 2. The negative capacitance effect results in reduction of SS in ferroelectric devices which improves the device performance. SS is related to temperature as (SS = 60 T/300), where T is the temperature in Kelvin. [22]. Thus, SS increases with the rise in temperature as depicted in Table 2. The lowest SS achieved for the proposed structure at 300 K is 23 mV/dec. The energy band diagrams of the

Table 2 Effect of temperature on electrical properties

Temperature (K)	FE DS-SBTFET		DS-SBTFET	
	I_{ON}/I_{OFF}	SS (mV/dec)	I_{ON}/I_{OFF}	SS (mV/dec)
300	1.2×10^9	23	2.4×10^6	55
400	5.7×10^7	93	7.6×10^5	149
500	3.8×10^5	127	7.5×10^4	164

proposed Fe DS-SBTFET and conventional DS-SBTFET at ON state is shown in Fig. 4. It is observed that the presence of ferroelectric layer reduces the tunneling barrier width of Fe DS-SBTFET. The amplified internal voltage caused by the negative capacitance effect results in high electric field. Thus, the tunneling probability increases and the proposed device provides high ON-state current. The I_D-V_{GS} sweep of the proposed device has been shown in Fig. 5. Memory window signifies the total number of dipoles (MW ~ 2Ec x d) where Ec is the ferroelectric coercive field and and d is the thickness of the ferroelectric film [23]. Fe DS-SBTFET with ferroelectric thickness of 6 nm provides memory window of 0.5 V. Figure 6 shows the polarization versus electric field plot of Fe DS-SBTFET. Due to the hysteresis behavior of the characteristics, it is possible to obtain subthreshold swing (SS) below 60 mV/decade [11].

The variation of total gate capacitance (C_{GG}) of FE DS-SBTFET with temperature is depicted in Fig. 7. C_{GG} increases with gate bias as at fixed drain voltage and low gate bias, inversion layer forms near the drain side which gets extended towards the source on further increasing the gate bias. With the increase in temperature C_{GG} increases. Reduction of energy barrier at high temperature increases the of inversion charge carrier concentration at the surface of the semiconductor. To balance these charge carriers gate charge increases leading to high gate capacitance.

The comparison of transconductance ($g_m = \partial I_D/\partial V_{GS}$) at 300 K of both the structures is depicted in Fig. 8a. The ON current of FE DS-SBTFET is more compared to DS-SBTFET

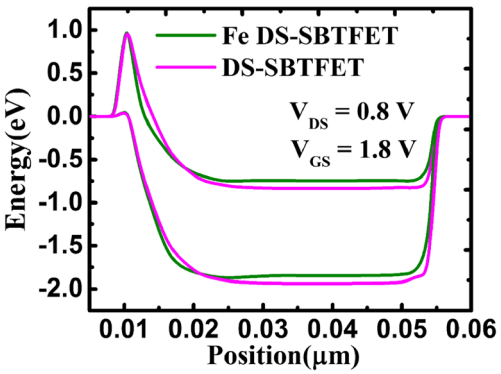

Fig. 4 Energy band diagram of the proposed Fe DS-SBTFET and DS-SBTFET at $V_{DS} = 0.8$ V

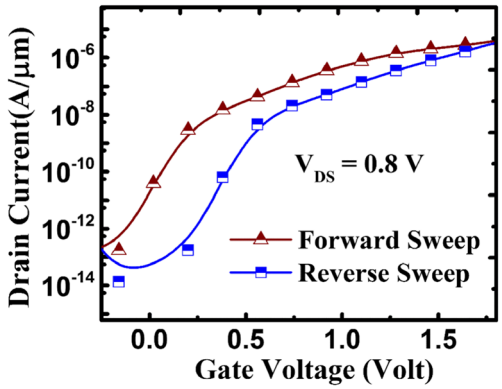

Fig. 5 I_D-V_{GS} characteristics with forward and reverse sweep of the Fe DS-SBTFET $V_{DS} = 0.8$ V

as observed in Fig. 3. The high drain current due to negative capacitance boosts up g_m of FE DS-SBTFET.

Figure 8b depicts the variation of transconductance, g_m for a range of temperature. Owing to the positive temperature coefficient of the drain current, g_m enhances with the rise in temperature. It is evident from Fig. 8 that g_m enhances with increase in gate bias. This is due to the enhancement in the tunneling of electrons through the source-channel tunneling junction caused by the improved electrical coupling of gate and tunneling region. More band to band tunneling of electrons at high temperature leads to high drain current and high g_m.

The comparison of an important RF parameter i.e. cut-off frequency (f_T) of both the devices and its dependence on temperature has been shown in Fig. 9a and (b) respectively. Short circuit current gain becomes unity at f_T. It is related to total gate capacitance (C_{GG}) and to transconductance (g_m) as [22].

$$f_T = \frac{g_m}{2\pi C_{GG}} \tag{3}$$

The device with higher g_m and lower C_{GG} is of interest for high value of f_T. The variation of f_T with gate voltage is similar to g_m due to the insignificant variation of denominator ($2\pi C_{GG}$). It can be observer from Fig. 9a that the proposed

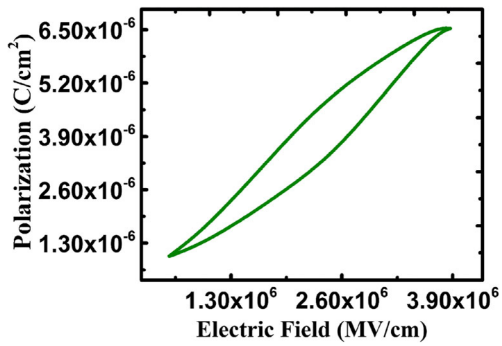

Fig. 6 Plot of polarization versus electric field for Fe DS-SBTFET at $V_{DS} = 0.8$ V and ferroelectric thickness of 6 nm

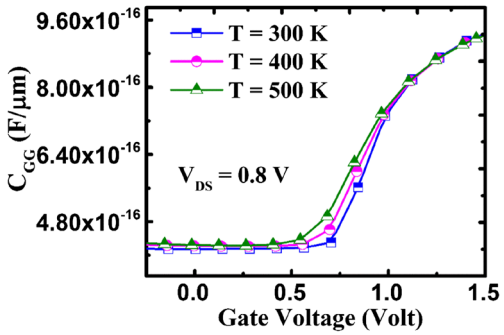

Fig. 7 Plot of dependencies of total capacitance (C_{GG}) on temperature for Fe DS-SBTFET

FE DS-SBTFET device provides higher f_T compared to DS-SBTFET At high temperature, BTBT rate of electrons enhances leading to high drain current which results in high transconductance of the device. Hence, f_T of the proposed device increases with the rise of temperature. Moreover, a high f_T of GHz range is shown by the proposed device making it suitable for high frequency applications.

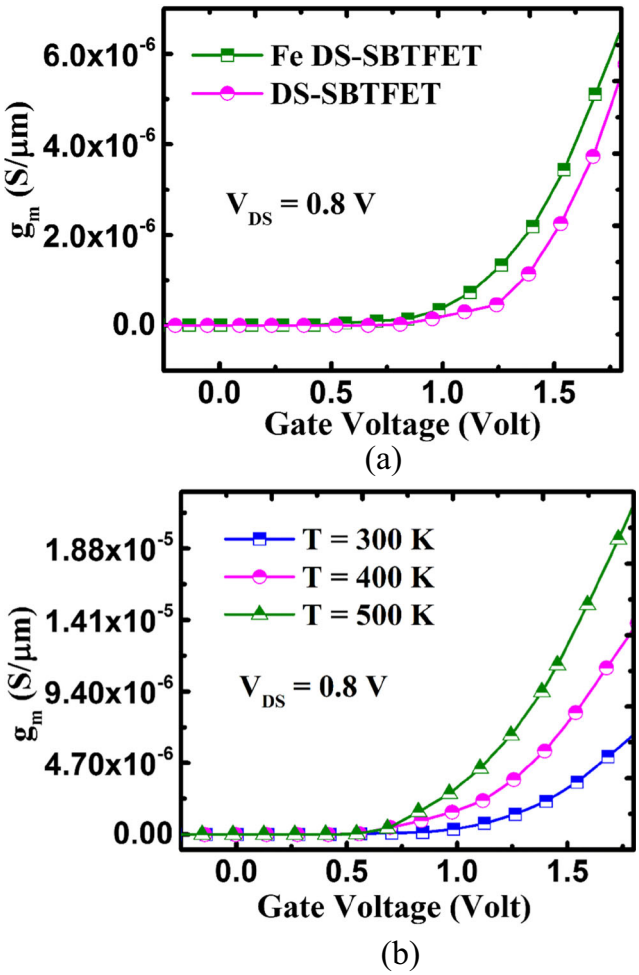

Fig. 8 Plot of **a** comparison of transconductance (g_m) of both the devices **b** dependencies of transconductance on temperature for Fe DS-SBTFET

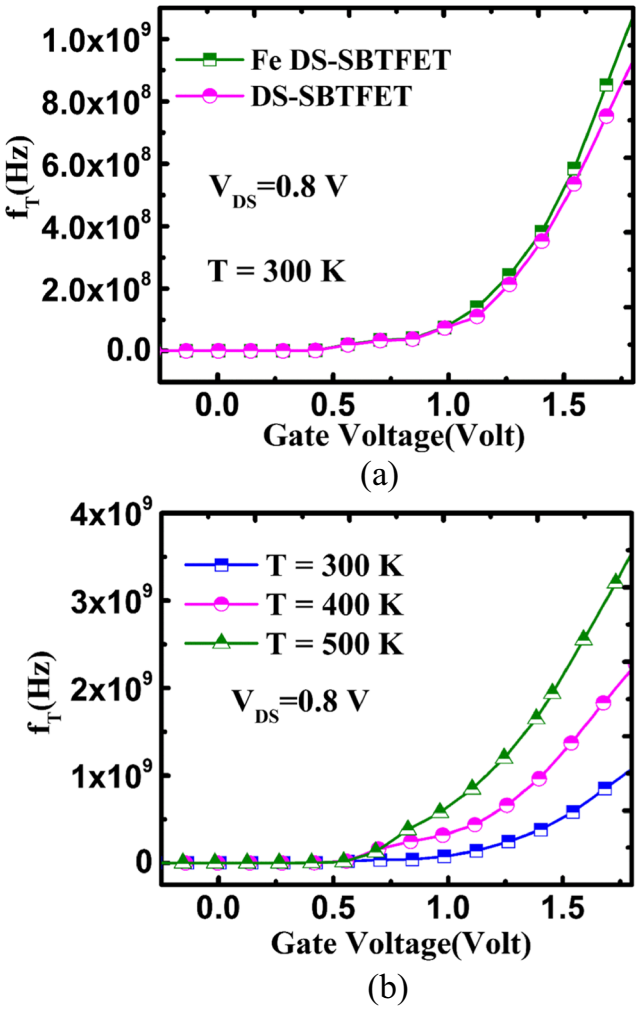

Fig. 9 Plot of **a** comparison of cut-off frequency (f_T) of both the devices **b** dependencies of f_T on temperature for Fe DS-SBTFET

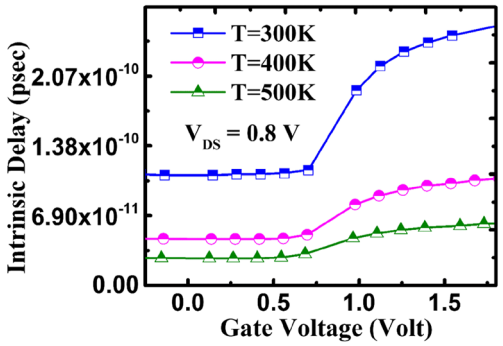

Fig. 10 Plot of dependencies of intrinsic delay (τ) on temperature for Fe DS-SBTFET

An essential RF figure of merit for circuit applications is intrinsic delay. It is enumerated as [24].

$$(\tau = ((C_{GG}V_{DD})/I_{on})) \quad (4)$$

Where, V_{DD} = 0.8 V is the drain bias voltage.

The temperature affectability on τ is depicted in Fig. 10. The inverse relation of drain current with temperature results in the reduction of τ with enhancement of temperature. τ is a crucial parameter for digital logic applications. The power consumption and switching speed characteristics are determined by the parasitic capacitances of the device.

The impact of temperature on device efficiency i.e. transconductance generation factor ($TGF = {}^{g_m}/_{I_{DS}}$) is shown in Fig. 11. It is evident that the variation of TGF with temperature is more at low gate bias and it is almost comparable at high gate bias. Moreover, TGF reduces with the rise in temperature. This is due to the inverse dependence of TGF on drain current as at high temperature drain current enhances in Fig. 3. The proposed device provides high efficiency a low temperature to convert power into speed and at high temperature the efficiency reduces.

Figure 12 shows the influence of temperature variation on transconductance frequency product ($TFP = g_m f_t/I_D$) of the device which is a significant parameter for high-speed application [5–7]. Similar to g_m and f_T, TFP also rises with temperature [25–27]. It rises linearly before the formation of inversion region.

To estimate the overall device performance, a significant RF parameter is used known as gain, transconductance, and frequency product,($GTFP = (g_m/g_d) \times (g_m/I_D) \times f_t$), where g_d is the output conductance [22]. The alteration of GTFP with temperature is depicted in Fig. 13. It enhances with the rise in temperature similar to transconductance (g_m) and cut-off frequency (f_T). It establishes a trade-off among cutoff frequency, intrinsic gain and TGF.

3.2 Temperature Affectability on Linearity Performance

To infer the capability of the device, linearity analysis is necessary. The higher order harmonics of I_D-V_{GS} characteristics

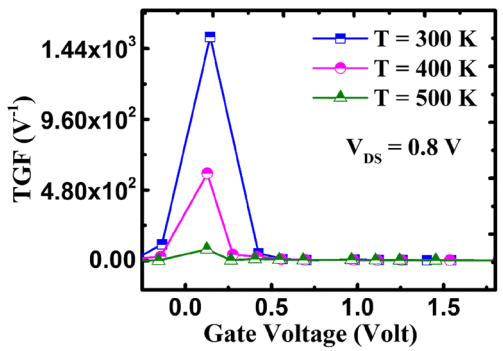

Fig. 11 Plot of dependencies of TGF on temperature for Fe DS-SBTFET

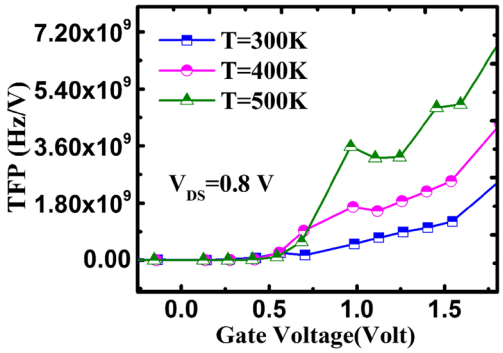

Fig. 12 Plot of dependencies of TFP on temperature for Fe DS-SBTFET

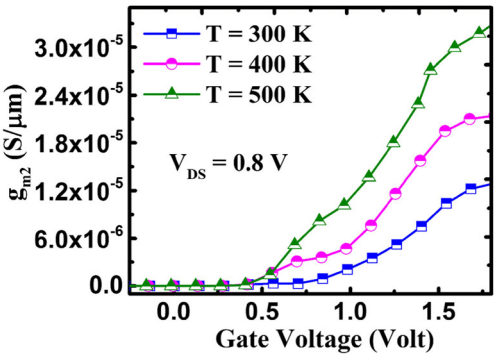

Fig. 14 Plot of dependencies of g_{m2} on temperature for Fe DS-SBTFET

versus gate bias such as second-order and third-order derivatives of drain current, I_D with respect to gate bias V_G i.e. g_{m2} and g_{m3} respectively are considered to measure the non-linearity of the device. This work investigates the effect of temperature on linearity parameters like g_{m2}, g_{m3}, and 1-dB compression point.

The variation of higher order derivatives (g_{m2}, g_{m3}) with temperature is depicted in Figs. 14 and 15. g_{m2} and g_{m3} are expressed as [28, 29].

$$g_{m2} = \frac{\partial^2 I_D}{\partial V_G^2} \tag{5}$$

$$g_{m3} = \frac{\partial^3 I_D}{\partial V_G^3} \tag{6}$$

It can be observed that both g_{m2} and g_{m3} increases indicating linearity characteristics degradation with the rise in temperature. This is attributed to degradation of DC characteristics with rise in temperature as mentioned in Table 2. For better linearity performance of the device the amplitudes of g_{m2} and g_{m3} must be low. However, there is negligible variation in zero crossover point with temperature.

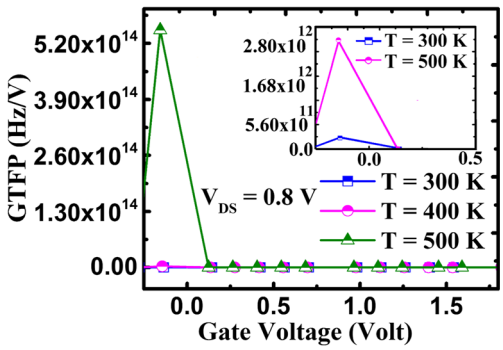

Fig. 13 Plot of dependencies of GTFP on temperature for Fe DS-SBTFET

High values of linear parameters indicate lesser distortion at the output. The 1-dB compression point is one of the vital parameter which measures the upper limit of linear operation [28]. This is defined as the input power where output power deviates from linearity by 1 dB. It is expressed as

$$1\,dB\,compression\,point = 0.22\sqrt{g_m/g_{m3}} \tag{7}$$

The influence of temperature on 1-dB compression point is shown in Fig. 16. It can be evident that at low temperature the proposed structure shows higher values of 1-dB compression point and it reduces with the rise in temperature. Thus, at low temperature the device shows better linearity performance. For amplifier applications, the ability of high input power enhances.

The extrapolated input gate voltage where the fundamental signal voltage level becomes equal to the second order harmonic signal voltage level is referred as VIP_2. The first order tone amplitude will govern the distortion beyond this critical voltage. VIP_3 indicates the extrapolated input gate voltage at which the fundamental signal voltage level and the second order harmonic signal voltage level are similar.

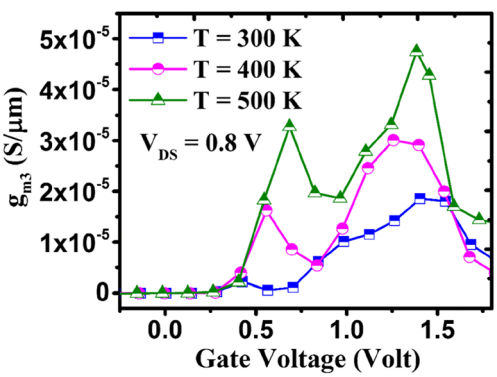

Fig. 15 Plot of dependencies of g_{m3} on temperature for Fe DS-SBTFET

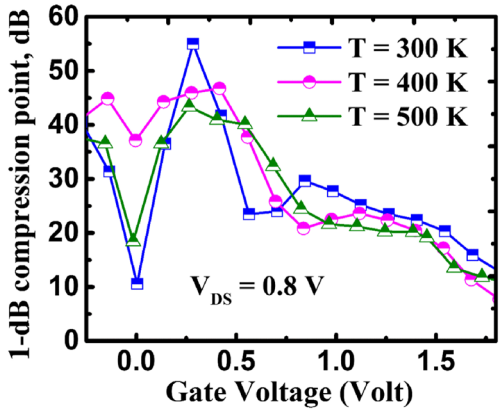

Fig. 16 Plot of dependencies of 1-dB compression point on temperature for Fe DS-SBTFET

VIP2 and VIP3 are expressed as [22].

$$VIP_2 = 4\left({}^{g_m}/_{g_{m2}}\right) \tag{8}$$

$$VIP_3 = \sqrt{24\left({}^{g_m}/_{g_{m3}}\right)} \tag{9}$$

Figures 17 and 18 depict the dependency of VIP_2 and VIP_3 respectively on temperature. At low temperature, the peak values of VIP_2 and VIP_3 increase due to the reduction of g_{m2} and g_{m3}. This signifies better linear performance of the proposed device at low temperature.

The affectability of temperature on IIP_3 is shown in Fig. 19. The extrapolated input power where the fundamental signal power becomes equal to the third order harmonic power is IIP_3. It is expressed as [22].

$$IIP_3 = \left({}^{2}/_{3}\right)\left({}^{gm}/_{g_{m3}R_S}\right) \tag{10}$$

Where, R_S is 50 Ω.

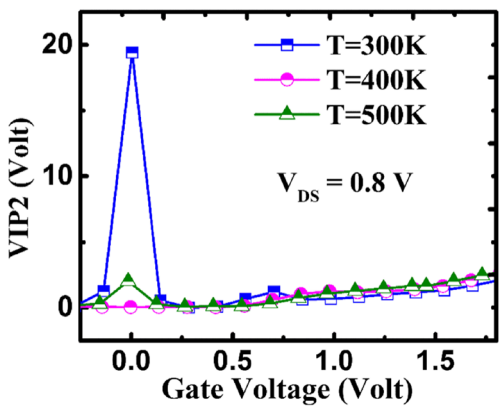

Fig. 17 Plot of dependencies of VIP_2 on temperature for Fe DS-SBTFET

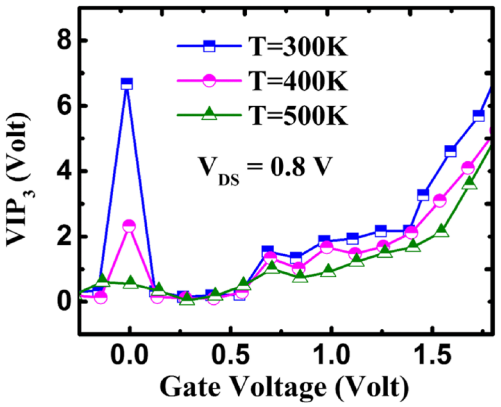

Fig. 18 Plot of dependencies of VIP_3 on temperature for Fe DS-SBTFET

The highest peak of IIP_3 at low temperature of 300 K indicates improved linearity characteristics at low temperature. Higher the peak of IIP_3 better the performance of the device.

4 Conclusion

An investigation of temperature dependency on various DC, RF and linearity parameters has been reported for Fe DS-SBTFET and DS-SBTFET. The presence of ferroelectric layer enhances the ON current and reduces the SS in Fe DS-SBTFET due to negative capacitance effect. With the rise in temperature both I_{ON} increases due to bandgap narrowing. Highest I_{ON}/I_{OFF} ratio and minimum SS of 1.2×10^9 and 23 mV/dec respectively have been achieved for Fe DS-SBTFET at 300 K. High cut-off frequency of 10^9 Hz makes the proposed device worthy for high frequency applications. Low intrinsic delay indicates improved performance in terms of speed at high temperature. The device shows better linearity performance at low temperature.

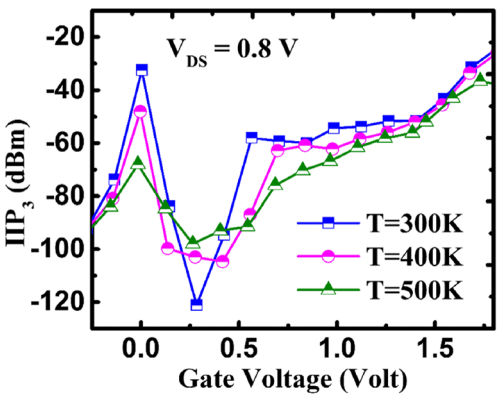

Fig. 19 Plot of dependencies of IIP_3 on temperature for Fe DS-SBTFET

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