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ORIGINAL PAPER

A Study on the Electronic Properties of SiO_xN_y/p-Si Interface

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Abstract

In this study, we investigated the electrical properties of *Sn/*SiO_xN_y*/p-Si* metal-insulator layer-semiconductor (*MIS*) structure. Silicon oxynitride (SiO_xN_y) thin film was grown on chemically cleaned *p-Si* substrate by the plasma nitridation process. The chemical composition and surface morphology of the thin film were analyzed using X-ray photoelectron spectroscopy (*XPS*) and atomic force microscopy (*AFM*). Electrical measurements of the devices (e.g. current-voltage (*I-V*), capacitance-voltage (*C-V*), capacitance and conductance-frequency characteristics (*C*-f and *G-f*)) were performed at room temperature. The characteristic parameters of the SiO_xN_y*/p-Si* interface such as energy position, interface state density and relaxation time constant were obtained from admittance measurements over a wide range of frequencies (from 1 to 500 kHz) for the values of the forward bias between $0.0\ \mathrm{V} \leq \mathrm{V} \leq 1.1\ \mathrm{V}$. The values of the interface state density and their relaxation time constant changed from $3.684 \times 10^{13}\ \mathrm{cm^{-2}\ eV^{-1}}$ to $3.216 \times 10^{12}\ \mathrm{cm^{-2} eV^{-1}}$ and from 1.770×10^{-5} s to 6.277×10^{-7} s, respectively. The obtained values of the interface state density were compared to those of the oxides grown by the other techniques. The experimental results clearly show that the density and location of interface states has a significant effect on electrical characteristics of the *MIS* structure.

Keywords Silicon oxynitride · Metal–insulator–semiconductor structure · Schottky barrier · Interface states · Series resistance · X-ray photoelectron spectroscopy

1 Introduction

Metal-insulator-semiconductor (*MIS*) structures constitute a significant part of many semiconductor devices used in various microelectronic applications. The performance and reliability of these devices are dependent on the properties of the insulator. In recent years, silicon oxynitride films (SiO_xN_y) have been extensively examined as a promising alternative to conventional thermal silicon oxide (SiO_2) since they satisfy the requirement of electrical reliability as gate dielectrics for metal-oxide-semiconductor field-effect transistors (*MOSFET*s) [1–10]. The band gap energy of SiO_xN_y can be adjusted between 5 and 9 eV depending on the $[O]/[N]$ ratio which gives rise to potential applications of heterostructures [4]. The chemical and electrical properties of silicon oxynitride films grown on silicon by different methods such as rapid thermal nitridation, chemical vapor deposition, low pressure chemical vapor deposition (*LPCVD*) and pure N_2O or *NO* plasma have been investigated by some researchers [1–6, 11–13]. *SiON* thin films have been deposited by RF magnetron sputtering from a pure silicon target in various $Ar{:}O_2{:}N_2$ atmospheres [12]. The electrical measurements of these layers have been carried out on samples with a Pt-SiO_xN_y-Pt sandwich configuration. Capacitance-voltage (*C-V*) measurements have been used to characterize electrical contact. The results of current-voltage (*I-V*) characteristics have been discussed in relation to the structure change of SiO_xN_y thin films [12]. In the case of the silicon nitrides, their higher dielectric constant permits the use of physically thicker films while retaining the same *C-V* performance as that of thinner oxide layers [13].

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Generally, the electrical characteristics of *MIS* devices are controlled by the quality of the interfacial layer formed by various methods between the semiconductor and metal [14–17]. For this reason, the study of interface states is important for the understanding of the electrical properties of such devices. There are a number of methods used for determining of characteristic interface parameters such as energy position, density and relaxation time constant. Terman used the high frequency capacitance method for determining interface state capacitance [18]. Cowley and Sze developed a technique to determine the density of interface states on the basis of barrier height data obtained from an analysis of the barrier height with different metallization as a function of the metal work function [19]. Card and Rhoderick used current voltage characteristics to estimate the density of the interface states of metal/insulator/semiconductor structures [20]. Chattopadhyay and Raychaudhuri developed a capacitance technique to determine the interface state density of metal-semiconductor contacts (Schottky barrier diodes-*SBDs*) by considering series resistance and the interfacial oxide layer [21].

Tseng and Wu discussed the occupation of interfacial states as a function of applied voltage and extracted the density distribution of the interface states from the nonideal *I-V* characteristics [22]. Pandey and Kal attempted a theoretical approach related to the *C-V* characteristics for nonideal *Al/n-Si/p-Si SBDs* taking into account series resistance [23]. They compared experimental and theoretical results obtained at low and high frequencies and found them to be in close agreement with the results obtained by both methods. Szatkowsks and Sieranski showed that the nonideality of the C^{-2}-V relation can be entirely explained on the basis of the assumption that only some of the interface states follow the applied ac signal [24]. Cova and Singh resolved the controversy between the role of the interface states and deep level bulk traps by regarding the electrical characteristics $Ni/n\text{-}CdF_2$ *SBD*s [25].

The purpose of this work is to investigate the electrical properties of the SiO_xN_y/*p-Si* structure formed by thin film grown on chemically cleaned *p-Si* substrate by the plasma nitridation process. The chemical composition of the thin film grown on chemically cleaned *p-Si* was characterized using *XPS*. The values of the ideality factor (n) and the barrier height of the device (Φ_b) were found by using the forward bias *I-V* characteristics at room temperature. The characteristic parameters of the SiO_xN_y/*p-Si* interface such as energy position, density and relaxation time constant were obtained from admittance measurements as a function of frequency. Furthermore, the obtained values were compared to those of the oxides grown by the other techniques.

2 Experimental Procedure

A *p*-type *Si* wafer, one side polished, with (100) orientation and 5–10 Ω-cm resistivity was used in the fabrication of a *MIS* device. The wafer was chemically cleaned using the RCA cleaning procedure (i.e., a 10 min boil in $NH_4 + H_2O_2 + 6H_2O$ followed by a 10 min boil in $HCl + H_2O_2 + 6H_2O$). Before ohmic contact formed on the *p-Si* substrate, the samples were dipped in dilute $HF{:}H_2O$ (1:10) for about 30 s to remove any native thin oxide layer on the surface, the wafer was then rinsed by deionized water (purity up to 18.2 MΩ-cm). The wafer was dried with high-purity nitrogen and then it was inserted into the deposition chamber immediately after cleaning. Ohmic contact was made by evaporating *Al* (99.999%) on the back of the substrate, followed by temperature treatment at 570 °C for 3 min in flowing N_2 in a quartz tube furnace. The insulator layer was formed by plasma nitridation on the back of the sample with the ohmic contact. The plasma nitridation process was performed by using DC pulsed plasma with a pulse frequency 50 kHz and pulse width 1.6 μs at 500 °C for 1 h in NH_3 atmosphere. The average thickness of the oxide layer was measured to be 10.7 nm by using the profilometer. After the plasma nitridation process, the wafer was cut into two pieces by using a diamond saw with the faces perpendicular to the (100) direction. One of them was used for the analysis of *XPS* measurements. The other sample was inserted into the evaporation chamber for the formation the gate electrode. Sn (99.99%) as dots with a diameter of about 1 mm was evaporated through a *Mo* mask on the insulator layer. The evaporated film thickness was monitored using a quartz oscillator and the metal films had a thickness of 130 Å. All evaporation processes were carried out in a vacuum coating unit at about 10^{-6} Torr.

The *XPS* spectra for the oxidized sample were recorded using a SAGE 100 system equipped with an Mg $K\alpha$ source and *Ar* ion bombardment system. The surface morphology of the oxidized sample was investigated using *AFM*. The current-voltage (*I-V*), capacitance-voltage (*C-V*), capacitance-frequency (*C-f*) and conductance-frequency (*G-f*) measurements of the device were carried out using a VEE Pro program HP 4140B picoamperemeter and a HP 4980A LCR meter, respectively, at room temperature and in the dark.

3 Results and Discussion

3.1 XPS and AFM Measurements

Figure 1a–c shows the measured and fitted high-resolution $Si\ 2p$, $N1s$ and $O1s$ *XPS* spectra for the SiO_xN_y film.

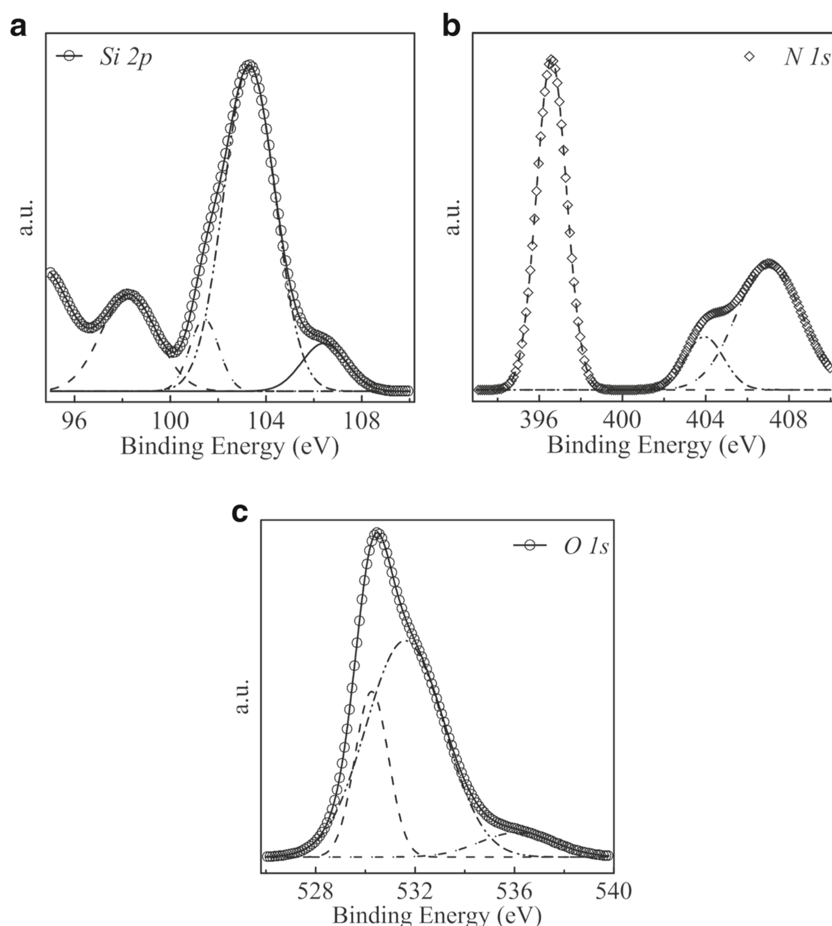

Fig. 1 The *XPS* spectra of **a** *Si 2p*, **b** *N 1s* and **c** *O 1s* core levels on the plasma-nitrided *Si* surface

All XPS results shows that a thin film successfully grown on substrate and bonding properties shows that a film composition was a SiO_xN_y.

As shown in Fig. 1a, the *Si* 2*p* peak was deconvoluted into multiple peaks. The binding energies of intermediate *Si* oxidation states (Si°, Si^{+1}, Si^{+2}, Si^{+3}) are found between 98.27 and 106.42 eV. The *Si* 2*p* *XPS* spectrum shows four peaks at 98.27, 101.42, 103.30 and 106.42 eV. The peak at 98.27 eV can be assigned to elemental silicon [26–28], the second peak at 101.42 eV to Si_3N_4 [28–31], the peak at 103.30 eV to *O*-rich SiO_x [28–31], and the unidentified peak at 106.42 eV. It is well known that the peaks for the SiO_xN_y depending on the nitrogen content are known to vary between the peak positions for SiO_2 and Si_3N_4 [28]. This binding energies indicate that SiO_xN_y film is oxygen rich (peak is close to the SiO_x binding energy) and normalized N/O ratio is approximately 0.87 [28]. The chemical shift between the *Si* 2*p* substrate peak and the oxidized silicon in the *SiON* over layer is 3.7 eV, which is significantly smaller than the 4.2 eV shift reported for pure SiO_2 layers grown on *Si* [32].

The *N* 1*s* *XPS* spectrum of the plasma-nitrided sample is shown in Fig. 1b. The spectrum has a peak at a value of 396.59 eV and was deconvoluted into two components using binding energy data with binding at 403.94 and 407.05 eV. The lowest binding energy peak at 396.59 eV can be assigned to the chemical environment of *N* similar to that in *N*-Si_3 bonding in a SiO_xN_y matrix [33]. In the *N 1s* spectrum, the binding energy for *Si-N* bonds in SiO_xN_y have found a broad peak centered around 396–399 eV [34–36]. While the *N 1s* peak position and its width seem to strongly depend on sample preparation methods and film thickness, very few have tried to systematically measure the relevant core levels for different samples with a conclusive spectroscopic resolution, as reported in the literature [35].

The other two peaks in the spectrum can be assigned to *NO* at 403.94 eV [35–37] and NO_3 at 407.05 eV [37]. In particular, a recent *XPS* finding suggested that an oxynitride film made by N_2O nitridation has a very different nearest-neighbor configuration of the interface species from those of *NO*-treated ones [35]. As reported by Chang, the varying thickness of the *SiON* films could have resulted in the different binding energies of a similar spectral feature due to the different core-hole screening [36].

As shown in Fig. 1c, the spectrum of the *O* 1*s* was deconvoluted into three components with binding energy at

530.25, 531.60, and 536.09 eV. The peak at 530.25 eV can be assigned to elemental oxygen [38] (possibly absorbed from sample environment and only exist on surface), the second peak at 531.60 eV to SiO_x [38, 39], the peak at 536.09 eV to *NO* [39]. For stoichiometric SiO_2, the O 1s binding energy is reported to be 532.5 eV [39]. The shift of the O 1s signal to a lower binding energy could be attributed to the incorporation of nitrogen atoms in the SiO_2 [40].

As is known, the surface roughness of the thin film grown on the semiconductor plays an important role in determining the electrical properties of device. Figure 2 shows the *AFM* image of the SiO_xN_y film grown on *p-Si*. As shown in Fig. 2, the surface morphology of the SiO_xN_y thin film is fairly smooth with a mean root mean square (*RMS*) roughness of 3.506 nm which it is a quite low value and in expectable range for the device applications.

3.2 Electrical Properties of the *MIS* Structure

Figure 3 shows the experimental semi-log forward and reverse bias *I-V* characteristics of the five *Sn/*SiO_xN_y*/p-Si MIS* structures at room temperature. As can be seen from the figure, the forward bias I-V characteristics of the device are linear on a semi-logarithmic scale at low forward bias voltage but deviate from linearity when the applied bias voltage is increased. These characteristics include the effects of the presence of the insulating layer between the metal and semiconductor, variation of the semiconductor surface charge population or population of the interface states with applied voltage, series resistance R_s, variations in the effective contact area with depletion layer width, and traps within the depletion region apart from the voltage-dependent image-force lowering of the effective barrier height which is most important in the reverse bias range [41–47].

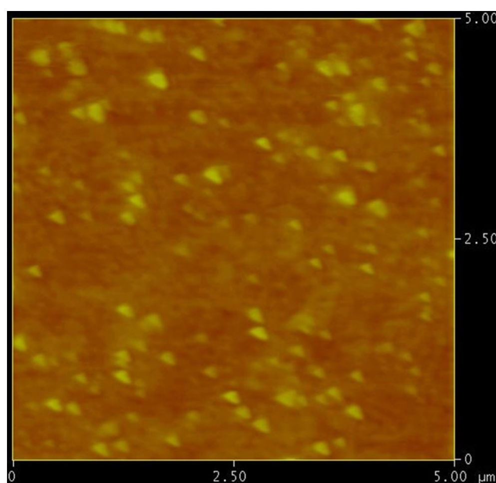

Fig. 2 The *AFM* image of the SiO_xN_y film grown on *p-Si*

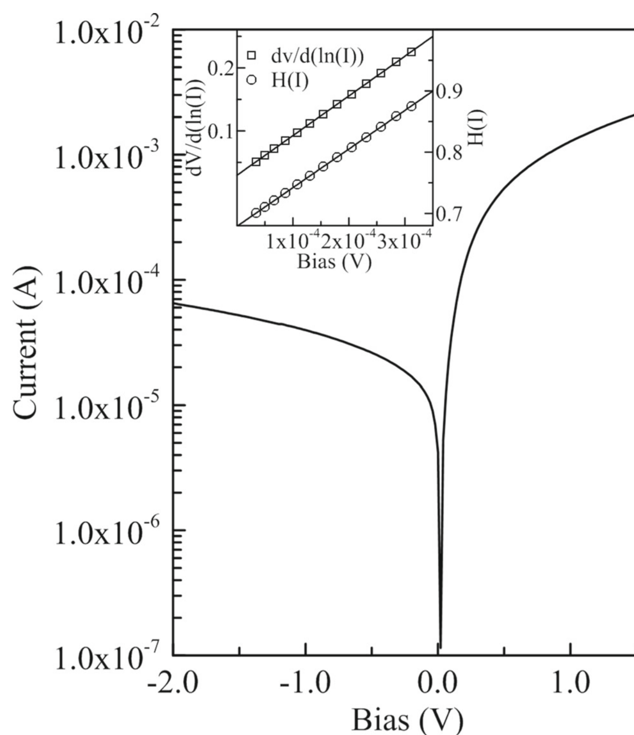

Fig. 3 The experimental semi-log forward and reverse bias *I-V* characteristics of one of the five *MIS* structures at room temperature

When metal/semiconductor contact with an insulator layer is considered, the forward current-voltage relationship due to the thermionic emission theory is given by [47]

$$I = I_o \left[\exp\left(-\frac{q(V - IR_s)}{nkT} \right) - 1 \right] \tag{1}$$

where I_o is the saturation current and is expressed as

$$I_o = AA^*T^2 \exp\left(-\frac{q\Phi_{b0}}{kT} \right) \tag{2}$$

where the quantities A, A^*, T, Φ_{b0}, k, V, n are the diode area, the effective Richardson constant which equals 32 $\mathrm{Acm^{-2}K^{-2}}$ for *p-Si*, the temperature in Kelvin, the effective or apparent barrier height, the Boltzmann constant, the applied voltage and the ideality factor which is a measure of the conformity of the diode to pure thermionic emission, respectively. The characteristic diode parameters such as barrier height and ideality factor are calculated by fitting the forward bias region with the *I-V* expression according to the thermionic emission theory. The fitting parameters were summarized in Table 1. The effective barrier height values ranged from 0.588 to 0.603 eV, and the ideality factor values n ranged from 1.856 to 2.118 for the investigated structures. As can be seen from Table 1, the values of barrier height and ideality factor from *I-V* characteristics vary from diode to diode even if they are prepared in the same way. The variation in the obtained

Table 1 The values of diode parameters obtained from the forward bias *I-V* characteristics of the Sn/$SiOxNy/p$-Si *MIS* structures at room temperature

MIS diodes ↓	*I-V*		*dV/dlnI*		*H(V)*	
	n	Φ_b *(eV)*	*n*	R_s (Ω)	Φ_b *(eV)*	R_s (Ω)
D1	1.856	0.603	3.408	873.055	0.586	902.919
D2	2.073	0.588	3.337	868.301	0.584	897.111
D3	2.118	0.594	2.748	868.429	0.578	880.642
D4	1.878	0.606	3.411	872.718	0.583	901.624
D5	1.959	0.595	3.193	826.708	0.579	845.363
Average value	1.977	0.597	3.219	861.842	0.582	885.532
Standard deviation	0.104	0.065	0.249	17.683	0.003	21.599

diode parameters can be attributed to inhomogeneities of thickness and to the composition of the layer, non-uniformity of the interfacial charges, and the presence of a thin insulating layer between the metal and semiconductor [41–46].

As well-known, the downward curvature region in the forward bias *I-V* curves at high bias voltage arises from the series resistance, R_S, of the neutral region of the semiconductor bulk between the depletion region, interfacial layer and ohmic contact. The series resistance values was calculated using Cheung and Cheung functions obtained from the following forward bias thermionic emission current equation given [43]. As can be seen from Table 1, the R_S values of SiO_xN_y/p-Si devices ranged from 826.708 to 873.055. The large value obtained for R_S can be attributed to the silicon oxynitride layer grown on the semiconductor surface plus to the neutral region series resistance.

Figure 4 shows the *C-V* characteristics of one of the five *MIS* Schottky diodes as a function of applied bias voltage with frequency as a parameter at room temperature. As can be seen in Fig. 4, the *C-V* characteristics have an anomalous peak. The peak value of the capacitance has decreased with increasing frequency. It is well known that the capacitance of *MIS* structure is extremely sensitive to the interface properties. This occurs because of the interface states that respond differently to low and high frequencies.

Figures 5 and 6 show the measured *C-f* and *G-f* of one the five *MIS* structures as a function of forward bias with bias voltage as a parameter which changes from 0.0 mV to 1.1 V at room temperature. It is seen from these curves that the values of the measured capacitance are significantly higher in the lower frequency range and tends to converge to an almost constant value at frequencies below 1 MHz and beyond.

In the case of the *MIS* structure, the electrically active interface states and the charges in the insulating layer (SiO_xN_y) cause a bias dependent potential drop across the interface. The higher values of capacitance at low frequencies are due to the excess capacitance resulting from the interface states in equilibrium with the *p-Si* substrate that can follow the ac signal. The low frequency equivalent circuit of the *MIS* structure with a distribution interface state level consisting of the insulator layer/oxide capacitance C_{ox} is in series with the parallel combination of the interface state capacitance C_{ss} and the depletion capacitance C_{sc}. At

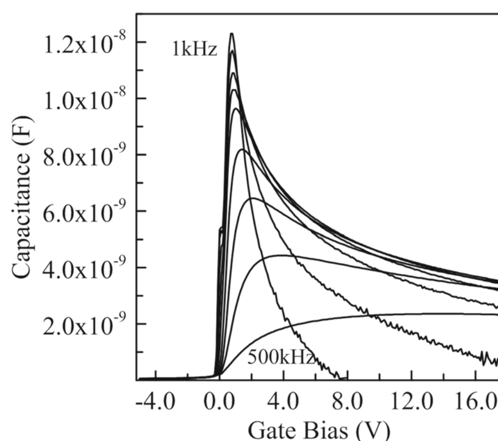

Fig. 4 The experimental capacitance plot as a function of voltage with frequency as a parameter of one of the five *MIS* structures at room temperature

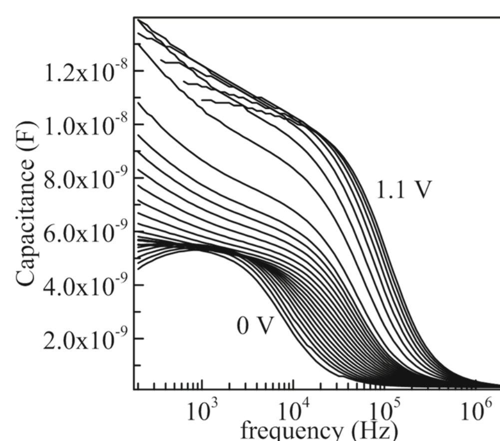

Fig. 5 The experimental capacitance plot as a function of frequency with bias voltage as a parameter of one of the five *MIS* structures at room temperature

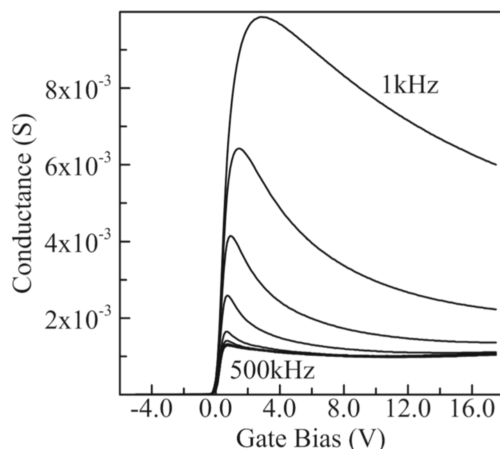

Fig. 6 The experimental conductance plot as a function of frequency with bias voltage as a parameter of one of the five *MIS* structures at room temperature

high frequencies, the interface states cannot respond to ac excitation, so they do not contribute to the total capacitance directly, but a stretch-out in the *C-V* curve occurs, as stated in the literature [48]. The variation of measured conductance with an applied bias is mainly due to the variation of capacitance with bias. In fact, both G and C magnitudes are influenced by the filling and/or emptying of interface states. Both phenomena cause energy loss due to holes in the valence band being trapped at the interface states and changes in the charge stored therein. The energy loss is demonstrated by conductance changes, while the charge storage affects the capacitance. The modulation frequency (w) dependence of the capacitance and conductance gives information on N_{ss}values and on characteristic times for interface states charging and discharging [48].

The conductance technique developed by Nicollian and Goetzberger is generally considered to be the best method to investigate interface states due to its high sensitivity, accuracy, and ability to measure the capture cross sections over a considerable energy range [48]. According to Nicollian and Goetzberger, the interface state conductance for a *MIS* structure can be described as

$$G_{ss} = \frac{AqN_{ss}}{2\tau} \ln(1 + \omega^2\tau^2) \tag{3}$$

where ω is the angular frequency, τ is the time constant which presents the characteristics time required to fill and empty the interface states at various energy levels and can be written as

$$\tau = \frac{1}{\mathrm{v_{th}}\ \sigma\ \mathrm{N_a}} \exp\left(\frac{\mathrm{qV_d}}{\mathrm{kT}}\right) \tag{4}$$

where σ, v_{th} and N_{a} are the cross section of the interface states, the thermal velocity of the carrier and the doping concentration, respectively. The conductance of the interface states G_{ss} obtained from experimentally measured admittance is given by [48]

$$G_{ss} = \frac{C_{ox}^2 G_m}{(C_{ox} - C_m)^2 + (G_m/w)^2} \tag{5}$$

where G_m, C_m and C_{ox} are the measured conductance, the measured capacitance and the oxide capacitance, respectively. The value of C_{ox} was found to be 59 pF from the accumulation region of the high frequency (500 kHz) capacitance-voltage characteristic of the *MIS* structure.

Furthermore, the energy of the interface states E_{ss} with respect to the top of the valence band at the surface of the p-type semiconductor is given by

$$E_{ss} - E_v = q(\Phi_e - V) \tag{6}$$

where Φ_e is the effective barrier height and related with the bias dependent ideality factor [25, 47, 49].

The quantity G_{ss}/ω shown in Fig. 7 was calculated from the *C-f* and *G-f* curves (Figs. 5 and 6) with the help of Eq. 5. As can be seen from Fig. 7, the peak values of G_{ss}/ω decrease with increasing bias voltage and the corresponding frequency moves to a higher value. This variation can be explained by the presence of an almost continuous distribution of interface state energy levels. For a distribution of interface states over the silicon band gap, transitions occur between the majority carrier band and interface states in an energy interval a few kT wide about the Fermi level. The interface states are defects located at the *SiO_xN_y/p-Si* interface and they can interact either with the conduction or with the valence bands by capturing or emitting electrons or holes, respectively, resulting in a change of their occupancy. The changes in occupancy are produced by varying the applied bias [22]. The capture and emission of interface state charges behave like a capacitor paralleled to the depletion layer capacitance, resulting in an increase of the total capacitance. Each interface state level

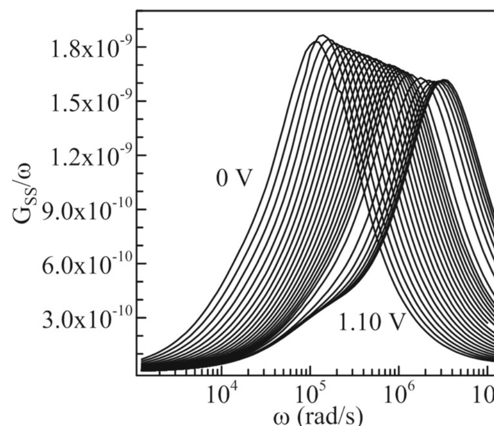

Fig. 7 G_{ss}/ω versus w characteristics obtained from the experimental forward bias conductance as a function of frequency measurements of one of the five *MIS* structures at room temperature

in this energy interval contributes a different energy loss depending on its distance in energy from the Fermi level. As a result, each interface state level in this energy interval has a different time constant. The curves in Fig. 7 go through maxima at $\omega\tau = 1.98$ with values of $(G_{ss}/\omega)_{\max=}$ $0.4e^2 N_{ss}$ [48, 50]. The ordinates and frequencies of the maxima in the G_{ss}/ω versus $ln(\omega)$ curve yield the density of the interface states, N_{ss}, and their time constants, τ. The dependence of N_{ss} and τ on the bias voltage was converted to a function of E_{ss} using Eq. 6. Figure 8 depicts the energy distribution of the interface states and their time constant determined from the experimental G_{ss}/ω versus $ln(\omega)$ curves of the *MIS* structure at room temperature. It can be seen from Fig. 8 that both the N_{ss} and τ show decreases with decreasing energy from the midgap toward the bottom of the valence band. The interface state density N_{ss} and time constant τ varied from 3.684×10^{13} cm^{-2}eV^{-1} and 1.770×10^{-5} s at 0 V bias to $3.216.06 \times 10^{12}$ cm^{-2}eV^{-1} and 6.277×10^{-7} s at 1.1 V bias, respectively.

Some techniques such as jet vapor deposition (JVD), atomic layer deposition (ALD), sputtering, as well as chemical vapor deposition techniques PECVD, LPCVD, direct plasma enhanced CVD (DPECVD), atmospheric pressure CVD (APCVD), plasma-assisted CVD and electron cyclotron resonance (ECR) plasma enhanced chemical vapor deposition (PECVD) etc. have been successfully used to deposit dielectric materials on substrates. These CVD techniques focused on enhancing the interface quality between the Si substrate and thin film.

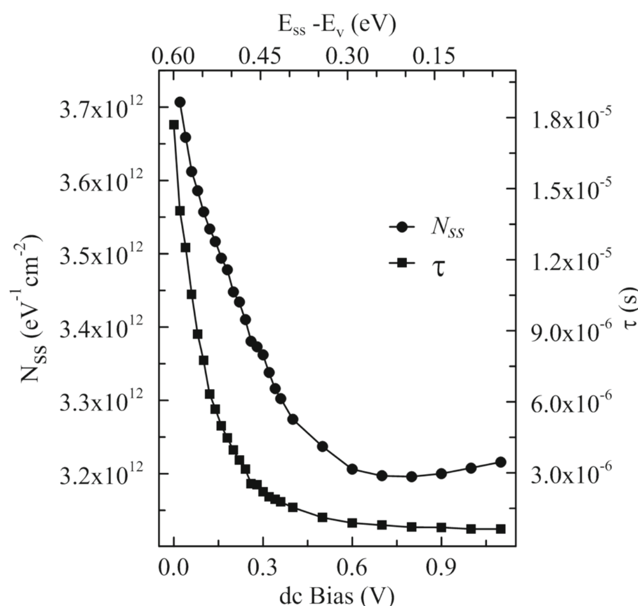

Fig. 8 The energy distribution curves of the interface states and their time constants obtained from the experimental G_{ss}/w versus w characteristics of one of the five *Sn/SiO$_x$N$_y$/p-Si* structures at room temperature

The interface state density of *SiO_xN_y/ n-type Si(111)* structures with films prepared by low-pressure chemical vapor deposition (*LPCVD*) was obtained in the low 10^{11} eV^{-1}cm^{-2} range at mid band gap [51]. The interface state density for *SiO_xN_y/ p- Si*(111) structure with silicon oxynitride (SiON) films fabricated at a low temperature using nitrogen plasma generated by an inductively coupled plasma system was found to be 3–4 $\times$ 10^{13} eV^{-1}cm^{-2} at mid band gap [34]. As mentioned in the literature, the higher N_{ss} observed may be due to nitrogen plasma induced damages resulting in a strained or broken silicon bonds at the interface [5, 34, 52].

In another study, Albertin and Pereyna have found that the interface state density values were function of nitrogen concentration in the films deposited by the plasma enhanced chemical vapor deposition (*PECVD*) technique from silane, nitrous oxide and nitrogen gaseous mixtures [53]. A variation in the interface state density with the films nitrogen concentration has been observed, the smallest value has been obtained for the silicon nitride dielectric layer.

In another work, SiON layers were deposited by electron cyclotron resonance (ECR) plasma enhanced chemical vapor deposition (PECVD) [54]. Fabricated devices interface state density was increases from about 10^{11} eV^{-1}cm^{-2} to 10^{12} eV^{-1}cm^{-2} when the layer composition changes from pure SiO_2 to pure Si_3N_4. Remote PECVD technique and rapid thermal annealing methods used to deposit silicon oxynitride films [55]. Devices has a very low N_{ss} values ($\sim 10^{11}$ eV^{-1}cm^{-2} at the midgap).

Our results clearly indicate that the N_{ss} values obtained from the *G-f* characteristics of the *MIS* structure are lower than or comparable to the given values in the literature above with reported values for silicon oxynitride films formed by different methods [5, 34, 35, 52]. Difference between the obtained results may be due to the properties of *SiOxNy* film depend on the nitridation system, nitridation process and/or quality of the used Si substrate.

4 Conclusions

We investigated the electrical properties of the *Sn/SiO_xN_y /p-Si MIS* structure. The thin *SiO_xN_y* insulating layer between metal and semiconductor was grown on $p-$Si substrate with the plasma nitridation process. The chemical composition of the thin film grown was characterized using *XPS*. The measured $N1s$ binding energy of 396.59 eV indicates *N-Si_3* bonding in a *SiO_xN_y* matrix. The binding energies of 98.27, 101.42, and 103.30 eV in the *Si* $2p$ *XPS* spectrum suggest elemental silicon, *Si_3N_4* and O-rich *SiO_x*, respectively. It is well known that the peaks for the *SiO_xN_y* depending on the nitrogen content are known to vary between the peak positions for *SiO_2* and *Si_3N_4*.

The forward *I-V* characteristics of the devices were analyzed on the basis of the thermionic emission theory. The barrier height and ideality factor values were calculated to be 0.597 ± 0.065 eV and 1.977 ± 0.104, respectively. On the other hand, Cheung functions combined with conventional forward *I-V* characteristics were used to obtain diode parameters such as Φ_b, n and R_s. The values of Φ_b, n and R_s were found to be 0.582 ± 0.003 eV, 3.219 ± 0.249, 861.842 ± 17.683 Ω, respectively. The interface characteristics of the SiO_xN_y/p-Si structure were evaluated by the *C-V*, conductance and capacitance via small ac signal admittance measurements at frequencies ranging from 1 to 500 kHz. It has been experimentally determined that the peak positions in the *C–V* plot shift toward lower voltages and the peak value of the capacitance decreases with increasing frequency. The interface state densities N_{ss} varied from 3.216×10^{12} cm^{-2}eV^{-1} to 3.684×10^{13} cm^{-2}eV^{-1} depending on the applied dc bias. The calculated density of the interface states is promising for *MISFET* construction. On the other hand, experimental results show that the density and locations of interface states between SiO_xN_y/p-Si have a significant effect on electrical characteristics of *MIS* structures. It seems that a buffer layer is a necessary condition to avoid high density of interface states.

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References

1. Sobolewski MA, Helms CR (1989) Studies of barrier height mechanisms in metal silicon-nitride silicon Schottky-Barrier diodes. J Vac Sci Technol B 7(4):971–979. https://doi.org/10.1116/1.584589
2. Ikeda A, Elnaby MA, Fujimura T, Hattori R, Kuroki Y (2001) Oxynitridation of silicon with nitrogen plasma for flash memory applications characterized by high frequency capacitance–voltage measurements. Thin Solid Films 385(1):215–219
3. El-Oyoun MA, Inokuma T, Kurata Y, Hasegawa S (2003) Temperature dependence of the structural properties of amorphous silicon oxynitride layers. Solid State Electron 47(10):1669–1676
4. Balland B, Glachant A (1999) Chapter 1 Silica, silicon nitride and oxynitride thin films. Instabilities Silicon Devices 3:3–144. https://doi.org/10.1016/S1874-5903(99)80007-x
5. Perera R, Ikeda A, Hattori R, Kuroki Y (2003) Effects of post annealing on removal of defect states in silicon oxynitride films grown by oxidation of silicon substrates nitrided in inductively coupled nitrogen plasma. Thin Solid Films 423(2):212–217
6. Konofaos N, Evangelou E, Aslanoglou X, Kokkoris M, Vlastou R (2003) Dielectric properties of CVD grown siON thin films on Si for MOS microelectronic devices. Semicond Sci Tech 19(1):50
7. Kim HS, Han SW, Jang WH, Cho CH, Seo KS, Oh J, Cha HY (2017) Normally-Off GaN-on-Si MISFET using PECVD SiON gate dielectric. IEEE Electron Device Lett 38(8):1090–1093
8. Cheng X, Marstein ES, Haug H, Di Sabatino M (2016) Double layers of ultrathin a-Si:H and SiNx for surface passivation of n-type crystalline Si wafers. Energy Procedia 92:347–352. https://doi.org/10.1016/j.egypro.2016.07.094
9. Walsh LA, Mohammed S, Sampat SC, Chabal YJ, Malko AV, Hinkle CL (2017) Oxide-related defects in quantum dot containing Si-rich silicon nitride films. Thin Solid Films 636:267–272. https://doi.org/10.1016/j.tsf.2017.06.022
10. Soman A, Antony A (2017) Broad range refractive index engineering of SixNy and SiOxNy thin films and exploring their potential applications in crystalline silicon solar cells. Mater Chem Phys 197:181–191. https://doi.org/10.1016/j.matchemphys.2017.05.035
11. Or DC, Lai P, Sin J (2003) Optimization of plasma nitridation for reliability enhancement of low-temperature gate dielectric in MOS devices. Solid State Electron 47(11):2049–2053
12. Rebib F, Tomasella E, Aida S, Dubois M, Cellier J, Jacquet M (2006) Electrical behaviour of SiOxNy thin films and correlation with structural defects. Appl Surf Sci 252(15):5607–5610. https://doi.org/10.1016/j.apsusc.2005.12.129
13. Ma Y, Yasuda T, Lucovsky G (1993) Fixed and trapped charges at oxide–nitride–oxide heterostructure interfaces formed by remote plasma enhanced chemical vapor deposition. J Vac Sci Technol B: Microelectron Nanometer Struc Process Meas Phenom 11(4):1533–1540
14. Mönch W (2001) Semiconductor surfaces and ınterfaces. Springer, New York
15. Altındal S, Kanbur H, Yucedag I, Tataroglu A (2008) On the energy distribution of interface states and their relaxation time and capture cross section profiles in Al/SiO2/P-Si (MIS) Schottky diodes. Microelectron Eng 85(4):1495–1501. https://doi.org/10.1016/j.mee.2008.02.001
16. Çetin H, Ayyildiz E, Türüt A (2005) Barrier height enhancement and stability of the Au/n-InP Schottky barrier diodes oxidized by absorbed water vapor. J Vac Sci Technol B: Microelectron Nanometer Struc 23(3):2436. https://doi.org/10.1116/1.2126675
17. Kar S, Varma S (1985) Determination of silicon-silicon dioxide interface state properties from admittance measurements under illumination. J Appl Phys 58(11):4256–4266
18. Terman LM (1962) An investigation of surface states at a silicon/silicon oxide interface employing metal-oxide-silicon diodes. Solid State Electron 5(5):285–299
19. Cowley A, Sze S (1965) Surface states and barrier height of metal-semiconductor systems. J Appl Phys 36(10):3212–3220
20. Card HC, Rhoderick EH (1971) Studies of tunnel MOS diodes I. Interface effects in silicon Schottky diodes. J Phys D: Appl Phys 4(10):1589
21. Chattopadhyay P, Raychaudhuri B (1993) Frequency-dependence of forward capacitance voltage characteristics of Schottky-barrier diodes. Solid State Electron 36(4):605–610. https://doi.org/10.1016/0038-1101(93)90272-R
22. Tseng H-H, Wu C-Y (1987) A simple interfacial-layer model for the nonideal IV and CV characteristics of the Schottky-barrier diode. Solid State Electron 30(4):383–390
23. Pandey S, Kal S (1998) A simple approach to the capacitance technique for determination of interface state density of a metal-semiconductor contact. Solid State Electron 42(3):943–949. https://doi.org/10.1016/S0038-1101(97)00267-0
24. Szatkowski J, Sierański K (1992) Simple interface-layer model for the nonideal characteristics of the Schottky-barrier diode. Solid State Electron 35(4):1013–1015
25. Cova P, Singh A, Masut RA (1997) A self-consistent technique for the analysis of the temperature dependence of current-voltage and capacitance-voltage characteristics of a tunnel metal-insulator-semiconductor structure. J Appl Phys 82(10):5217–5226. https://doi.org/10.1063/1.366386

26. Morgan WE, Van Wazer JR (1973) Binding energy shifts in the x-ray photoelectron spectra of a series of related Group IVA compounds. J Phys Chem 77(4):964–969
27. National Institute of Standards and Technology (2012) http://srdata.nist.gov/xps/. Accessed 2017
28. Cubaynes F, Venezia V, Van der Marel C, Snijders J, Everaert J, Shi X, Rothschild A, Schaekers M (2005) Plasma-nitrided silicon-rich oxide as an extension to ultrathin nitrided oxide gate dielectrics. Appl Phys Lett 86(17):172903
29. Du H, Tressler RE, Spear KE (1989) Thermodynamics of the Si-N-O system and kinetic modeling of oxidation of Si3N4. J Electrochem Soc 136(11):3210–3215
30. Dupuie JL, Gulari E, Terry F (1992) The low temperature catalyzed chemical vapor deposition and characterization of silicon nitride thin films. J Electrochem Soc 139(4):1151–1159
31. Kohli S, Theil JA, Dippo PC, Ahrenkiel RK, Rithner CD, Dorhout PK (2005) Chemical, optical, vibrational and luminescent properties of hydrogenated silicon-rich oxynitride films. Thin Solid Films 473(1):89–97
32. Tao Y, Lu Z, Graham MJ, Tay S (1994) X-ray photoelectron spectroscopy and x-ray absorption near-edge spectroscopy study of SiO_2/Si (100). J Vac Sci Technol B: Microelectron Nanometer Struc Process Meas Phenom 12(4):2500–2503
33. Delfino M, Fair J, Salimian S (1992) Thermal nitridation of silicon in a cluster tool. Appl Phys Lett 60(3):341–343
34. Liao J-H, Hsieh J-Y, Lin H-J, Tang W-Y, Chiang C-L, Lo Y-S, Wu T-B, Yang L-W, Yang T, Chen K-C (2009) Physical and electrical characteristics of silicon oxynitride films with various refractive indices. J Phys D: Appl Phys 42(17):175102
35. Kim YK, Lee HS, Yeom H, Ryoo D-Y, Huh S-B, Lee J-G (2004) Nitrogen bonding structure in ultrathin silicon oxynitride films on Si (100) prepared by plasma nitridation. Phys Rev B 70(16):165320
36. Chang J, Green M, Donnelly V, Opila R, Eng J Jr, Sapjeta J, Silverman P, Weir B, Lu H, Gustafsson T (2000) Profiling nitrogen in ultrathin silicon oxynitrides with angle-resolved x-ray photoelectron spectroscopy. J Appl Phys 87(6):4449–4455
37. Datta M, Mathieu H, Landolt D (1984) Characterization of transpassive films on nickel by sputter profiling and angle resolved AES/XPS. Appl Surf Sci 18(3):299–314
38. Aygun G, Atanassova E, Alacakir A, Ozyuzer L, Turan R (2004) Oxidation of Si surface by a pulsed Nd: YAG laser. J Phys D: Appl Phys 37(11):1569
39. Lai Y-S, Chen K-J, Chen J-S (2002) Effects of plasma prenitridation and postdeposition annealing on the structural and dielectric characteristics of the Ta2O5/Si system. J Electrochem Soc 149(4):F63–F68
40. Pashutski A, Folman M (1989) Low temperature XPS studies of NO and N2O adsorption on Al (100). Surf Sci 216(3):395–408
41. Song YP, Vanmeirhaeghe RL, Laflere WH, Cardon F (1986) On the difference in apparent barrier height as obtained from capacitance-voltage and current-voltage-temperature measurements on Al/P-Inp Schottky barriers. Solid State Electron 29(3):633–638. https://doi.org/10.1016/0038-1101(86)90145-0
42. Tung RT (1992) Electron-transport at metal-semiconductor interfaces - general-theory. Phys Rev B 45(23):13509–13523. https://doi.org/10.1103/PhysRevB.45.13509
43. Cheung SK, Cheung NW (1986) Extraction of schottky diode parameters from forward current-voltage characteristics. Appl Phys Lett 49(2):85–87. https://doi.org/10.1063/1.97359
44. Çetin H, Şahin B, Ayyıldız E, Türüt A (2004) The barrier-height inhomogeneity in identically prepared H-terminated Ti/p-Si Schottky barrier diodes. Semicond Sci Tech 19(6):1113–1116
45. Werner JH (1988) Schottky-barrier and Pn-junction I/V plots - small-signal evaluation. Appl Phys a-Mater 47(3):291–300. https://doi.org/10.1007/Bf00615935
46. Wittmer M, Freeouf JL (1992) Ideal Schottky diodes on passivated silicon. Phys Rev Lett 69(18):2701–2704. https://doi.org/10.1103/PhysRevLett.69.2701
47. Rhoderick EH, Williams RH (1988) Metal-semiconductor contacts. Clarendon, Oxford
48. Nicollian EH, Goetzberger A (1967) The Si-SiO2 ınterface: electrical properties as determined by the metal-ınsulator-silicon conductance technique. Bell Syst Tech J 46(3):1055–1133
49. Depas M, Van Meirhaeghe RL, Laflère WH, Cardon F (1994) Electrical characteristics of Al/SiO2/n-Si tunnel diodes with an oxide layer grown by rapid thermal oxidation. Solid State Electron 37(3):433–441. https://doi.org/10.1016/0038-1101(94)90009-4
50. Nicollian EH, Brews JR (1982) Mos (Metal Oxide Semiconductor) physics and technology, vol 1. Wiley-Interscience, New York
51. Novkovski N (2002) Breakdown and generation of interface states in oxynitride thin films on silicon. Semicond Sci Tech 17(2):93
52. Ikeda A, Elnaby MA, Hattori R, Kuroki Y (2001) Effect of nitrogen plasma conditions on electrical properties of silicon oxynitrided thin films for flash memory applications. Thin Solid Films 386(1):111–116
53. Albertin K, Pereyra I (2005) Study of PECVD SiO_xN_y films dielectric properties with different nitrogen concentration utilizing MOS capacitors. Microelectron Eng 77(2):144–149
54. Hernandez MJ, Garrido J, Martinez J, Piqueras J (1997) Compositional and electrical properties of ECR-CVD silicon oxynitrides. Semicond Sci Tech 12(4):927
55. Ma Y, Lucovsky G (1994) Deposition of single phase, homogeneous silicon oxynitride by remote plasma-enhanced chemical vapor deposition, and electrical evaluation in metal–insulator–semiconductor devices. J Vac Sci Technol B: Microelectron Nanometer Struc Process Meas Phenom 12(4):2504–2510. https://doi.org/10.1116/1.587792