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ORIGINAL PAPER

Electrical and Dielectric Characterizations of $Cu_2ZnSnSe_4$/n-Si Heterojunction

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Abstract
$Cu_2ZnSnSe_4$ (CZTSe) thin film has been synthesized onto silicon substrates by liquid phase epitaxial growth for the first time in which Au/CZTSe/n-Si/Al heterojunction was successfully fabricated by this technique. The crystal structure and morphology of the CZTSe film were characterized by field emission scanning electron microscopy (FE-SEM) and X-ray diffraction (XRD). The I-V characteristics of the CZTSe/n-Si heterojunction in the dark have been studied at different temperatures ranged from 298 to 398 K to determine the diode parameters such as the rectification ratio, series and shunt resistances (RR, R_s and R_{sh} resp.), the effective barrier height (ϕ_b) and the diode ideality factor (n). The CZTSe/n-Si heterojunction shows an excellent rectification behavior. The ideality factor n, series resistance R_S, and shunt resistance R_{Sh}, were decreased with increasing the temperature. The photovoltaic constants such as V_{OC}, J_{SC}, fill factor and the efficiency of CZTSe/n-Si heterojunction have been calculated from the I-V characteristics under illumination. The CZTSe/n-Si heterojunction exhibits efficiency about 3.42% at room temperature. The dielectric measurements proved that the CZTSe/n-Si heterojunction device shows the behavior of two forward biased Schottky diodes.

Keywords $Cu_2ZnSnSe_4$ · Liquid phase epitaxial growth · Diode ideality factor · Series resistance · Dielectric characterization

1 Introduction

Kesterite semiconducting materials gained increasing attention because of their interesting properties and its potential applications in solar cells, light emitting diodes, supercapacitors and memory devices [1, 2]. The $Cu_2ZnSnSe_4$ (CZTSe) is an important member of the Kesterite materials has an important application in thin-film solar cell due to it is stable [3], nontoxic [4], inexpensive [5], has a suitable band gap about 1.13 eV [6, 7] and has a high absorption coefficient of visible light more than 10^4 cm^{-1} [8, 9]. The previous studies concentrate on the preparation of CZTSe thin film solar cells by two categories: vacuum and non-vacuum techniques. The vacuum techniques include thermal evaporation, sputtering, etc. The preparation of CZTSe thin film solar cell by a vacuum technique reaches to efficiency about 11.6% [10]. The non-vacuum techniques include electrodeposition, spray pyrolysis, etc. The efficiency of CZTSe thin film solar cell by the non-vacuum technique by Guo et al. is about 7% [11]. Cu2ZnSnSe$_4$ thin films have been formed by different techniques such as vacuum evaporation [12], electrodeposition [13], sputtering [14] and spray pyrolysis [15] technique.

In the present study work, CZTSe/ n-Si heterojunction was fabricated by liquid phase epitaxy, and this attempt is considered, the first time for preparing the CZTSe on silicon substrates by liquid phase epitaxial growth technique, despite large mismatch between the lattice constant of Si and CZTSe. Thinking about epitaxy as a method of preparation of optoelectric devices has a merit of reducing the number of interface states resulting from film annealing in other methods. Epitaxy fuses different components into a more or less single crystal-like structure that combines with the semiconductor creating a single unit device. The newly made device has electrical and dielectric properties that depend on the crystal structure's stoichiometry.

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The electrical properties of the CZTSe/ n-Si heterojunction have been measured by The I-V characteristics and Dielectric investigation. The I-V characteristics have been measured to determine the diode and photovoltaic parameters of our heterojunction. Dielectric investigation of the device allows us to determine its abilities as series resistance, conductivity range, etc. and the effect of frequency, dc bias voltage and temperature on different dielectric parameters. Allowing us to decide the use of the device and the proper mix for future work to form single or even multi-function devices.

2 Experimental Details

2.1 Preparation of CZTSe Thin Film by LPE

$Cu_2ZnSnSe_4$ epitaxial layers were grown in a conventional horizontal graphite sliding-boat system with the following ambient of high-purity hydrogen in a quartz reactor tube. The starting materials were (6 N) pure Cu, Zn, Sn, Se and n-type crystalline Si wafers with (100) orientation and sized up to 10 mm^2. The wafer was chemically cleaned by CP4 solution consists of (HF: HNO_3: CH_3COOH in the ratio 1:6:1) composition for 10 min [16, 17]. Then the wafer was washed by acetone and isopropanol, respectively, and finally dried in an argon atmosphere. For fabricating $Cu_2ZnSnSe_4$ structure, the LPE technique was employed. The detailed growth process is as follows: first, to remove oxide and other surface contaminants a standard procedure for cleaning of Cu, Zn, Sn and Se metal was performed before setting them into the boat. The temperature of the furnace was increased to nearly 1050 °C and was kept at this temperature for 1 h to make homogeneity within the supersaturated solution of $Cu_2ZnSnSe_4$. Next, the supersaturated substrate solution of $Cu_2ZnSnSe_4$ was moved. The source for the $Cu_2ZnSnSe_4$ film, the Cu, Zn, Sn, and Se were mixed and heated again up to 1050 °C during 1 h in order to homogenize. Next, the substrate was moved under a supersaturated solution, the temperature of the ramp was lowered down at a constant cooling rate of 0.3 °C/min. Once the temperature began to decrease, the melt for the $Cu_2ZnSnSe_4$ layer was pushed onto the surface of the substrate at a temperature of 950 °C. Finally, the substrate was slid away from the melt after 30 min. and the quartz reactor was drawn out the furnace.

Al electrode of thickness 150 nm was deposited onto the lower and upper surface of the n-type Si wafer. Then Au electrode of thickness 150 nm was deposited onto the $Cu_2ZnSnSe_4$ layer in the shape of a grid to make a collection for a photon. The fabrications of Al and Au electrodes were performed by a thermal evaporation technique type (Edward 306 A). The Au/$Cu_2ZnSnSe_4$/n-Si/Al heterojunction was presented in Fig. 1a. The liquid phase epitaxial growth technique was shown in Fig. 1b.

2.2 Characterizing Techniques

The structural properties of the CZTSe thin film grown onto n-Si have been studied by X-ray diffraction measurement, scanning electron microscopy and EDAX analysis. The X-ray diffraction measurement was done by an X-ray diffractometer, type (Philips X'Pert) to study the crystal structure of the grown CZTSe films with radiation of Cu Kα (1.5418 Å). The surface morphology of the CZTSe film was characterized by SEM (Quanta FEG 250). The electrical and photovoltaic properties of the CZTSe/n-Si heterojunction were studied by I-V characteristics measurements in the dark and under illumination conditions using high impedance electrometers (Keithley 614). Dielectric measurements were performed on a broadband spectrometer having a wide frequency range from 3 μHz −20 MHz, Novo control, Germany.

3 Results and Discussion

3.1 Structural Characterization

The crystallographic analysis of the CZTSe thin film grown on Si wafer was studied by X-ray diffraction (XRD) pattern as represented in Fig. 2a. From this figure, the peaks were observed at the positions of 36.32°, 65.93° and 69°. The first two peaks correspond to the preferred crystal orientations of (400), (008), CZTSe, respectively and matched with the PDF cards 52–0868 with tetragonal structure. The third peak corresponds to the (004) Si substrate. The surface morphologies of the CZTSe thin film was studied by Field emission scanning

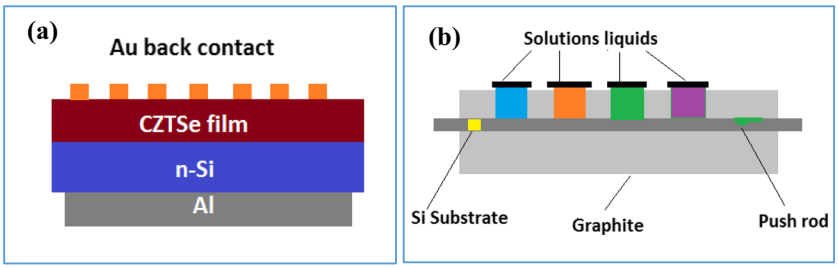

Fig. 1 **a** & **b**: **a** Schematic diagram of Au/$Cu_2ZnSnSe_4$/n-Si/Al heterojunction device, **b** liquid phase epitaxial growth technique

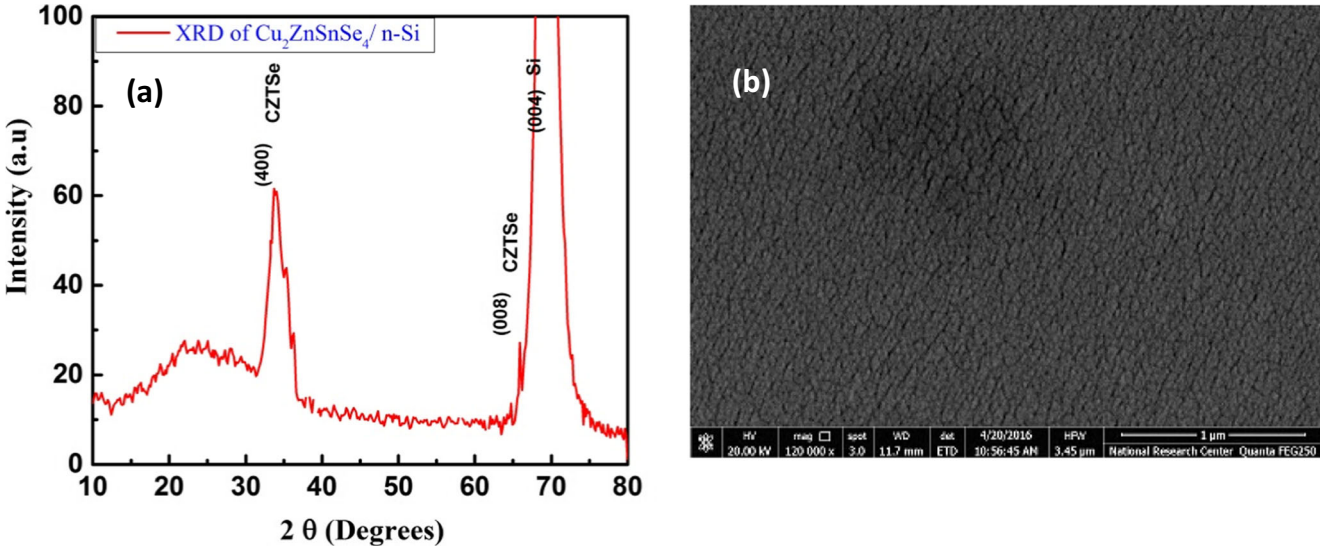

Fig. 2 **a** & **b**: **a** X-ray diffraction patterns for the $Cu_2ZnSnSe_4$ thin film grown onto n-Si wafer, **b** The FE SEM micrographs of $Cu_2ZnSnSe_4$ thin film

electron microscopic (FESEM) as shown in Fig. 2b. It is clear that a CZTSe thin film has a continuous and uniform granular structure with no detectable cracks. Such microstructure and surface morphology are suitable for the fabrication of heterojunction devices.

3.2 I-V Characteristics of the CZTSe /n-Si Heterojunction

Figure 3a shows the current-voltage characteristics of the $Cu_2ZnSnSe_4$ /n-Si heterojunction in the dark at different temperatures (298–398 K). From this figure, the $Cu_2ZnSnSe_4$ /n-Si heterojunction exhibits a rectifying behavior. Figure 3b illustrates the energy band diagram for the Au/$Cu_2ZnSnSe_4$/n-Si/Al heterojunction. The rectification ratio RR, of this heterojunction, was calculated as the ratio of forward and reverse current at a certain applied voltage (±2) [18]. The values of the rectification ratio (RR) for the $Cu_2ZnSnSe_4$ /n-Si heterojunction at different temperatures were recorded in Table 1 which shows that the values of RR were decreased as the temperature increased. The current-voltage characteristics of the $Cu_2ZnSnSe_4$ /n-Si heterojunction based on the thermionic emission theory are given by [19, 20]:

$$I = I_0\left(\exp\left(\frac{qV}{nKT}\right)-1\right) \quad (1)$$

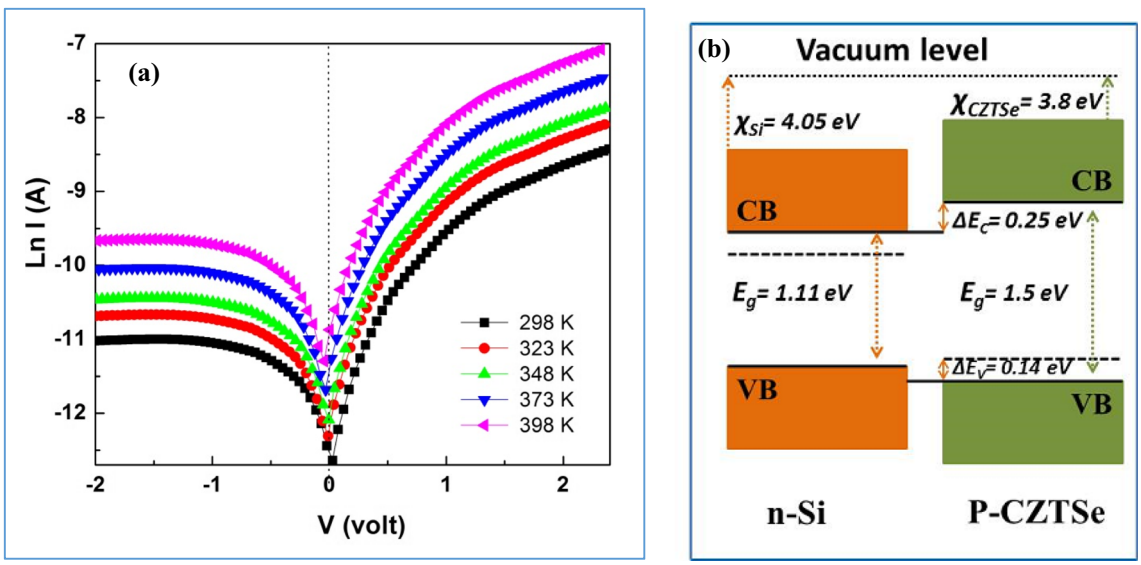

Fig. 3 **a** & **b**: **a** The dark I–V characteristics of Au/$Cu_2ZnSnSe_4$/n-Si/Al heterojunction device at different temperature, **b** The energy band diagram for the Au/$Cu_2ZnSnSe_4$/n-Si/Al heterojunction

Table 1 Junction parameters determined from the dark I-V characteristics of $Cu_2ZnSnSe_4$/n-Si heterojunction

T (K)	RR(at ± 1)	n	R_S ($k.\ \Omega$)	R_{sh} ($k.\ \Omega$)	ϕ_b (eV)
298 K	91.21	2.97	3.62	72.94	0.43
323 K	83.19	2.75	3.24	64.19	0.51
348 K	78.47	2.54	2.87	59.72	0.57
373 K	64.78	2.32	2.49	51.41	0.65
398 K	58.31	2.16	2.37	43.85	0.71

Where

n is the ideality factor,
q is the electronic charge,
T is the absolute temperature,
V is the voltage applied and
I_o is the saturation current.

The saturation current according to the thermionic emission mechanism is given by the following relation [21]:

$$I_o = AA^*T^2\exp\left[\frac{-q\phi_b}{KT}\right] \tag{2}$$

$$A^* = \frac{4\pi qm^*K^2}{h^3} \tag{3}$$

Where:

A is the area of the device,
A^* is the Richardson constant for n- Si assumed to be 112 $Acm^{-2}\ K^{-2}$ [22],
K is the Boltzmann constant,
m^* is the effective mass of the carriers (≈ 0.3 m_o where
m_o is the rest mass of the electron) and ϕ_b: is the barrier height.

The values of barrier height ϕ_b of the $Cu_2ZnSnSe_4$ /n-Si heterojunction have been obtained by the following equation [23]:

$$\phi_b = \frac{K_BT}{q}\ Ln\left(\frac{AA^*T^2}{I_0}\right) \tag{4}$$

The values of barrier height ϕ_b were recorded in Table 1.

The ideality factor n is the factor that shows how the diode follows the ideal diode equation [24]. The value of n was estimated from the slope of the linear region of the forward bias ln I-V characteristics Fig. 3. The dependence of both barrier height ϕ_b and ideality factor n on the temperature is shown in Fig. 4. The values of the barrier height ϕ_b of the $Cu_2ZnSnSe_4$ /n-Si heterojunction were increased as the temperature increased while the values of the idelity factor n were decreased as the temperature increased. This behavior explained as the current transport through the heterojunction is thermally activated process. As the temperature increases, more electrons get sufficient energy to surmount the higher barrier. This lead to increase the conduction and decrease the value of the ideality factor [25].

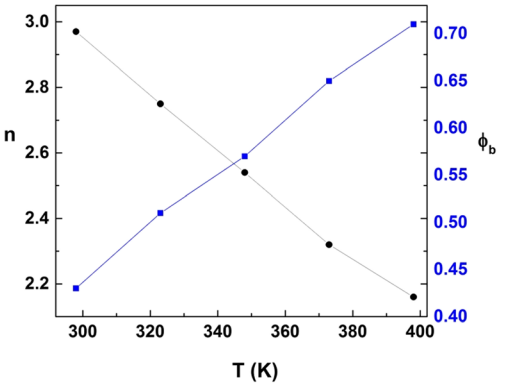

Fig. 4 The ideality factor and barrier height versus temperature for Au/$Cu_2ZnSnSe_4$/n-Si/Al heterojunction

The shunt resistance R_{Sh} and series resistance R_S are important parameters related to improving the performance of the heterojunction device. The series resistance R_S has been calculated from the slope of the linear part of the forward current-voltage curve by using the following relation [26]:

$$R_S = \frac{\Delta V_{Forward\ Bias}}{\Delta I_{Forward\ Bias}} \tag{5}$$

While the shunt resistance R_{Sh} has been calculated from the slope of the linear part of the reverse I-V curve by using the following relation [27]:

$$R_{Sh} = \frac{\Delta V_{Reverse\ Bias}}{\Delta I_{Reverse\ Bias}} \tag{6}$$

The temperature dependence characteristics of the $Cu_2ZnSnSe_4$ /n-Si heterojunction for the series resistance R_S and shunt resistance R_{Sh} were represented in Fig. 5. It is observed that the values of the R_S and R_{Sh} were decreased with increasing the temperature. This decreasing related to the improvement of diode conductivity by increasing the temperature [28]. The values of R_S and R_{Sh} were recorded in Table 1.

3.3 Photovoltaic Properties of the CZTSe /n-Si Heterojunction

Figure 6a shows the I–V characteristics of the Au/$Cu_2ZnSnSe_4$/n-Si/Al heterojunction at room temperature under light illumination. It can be seen from Figs. 3 and 6 that the values of current at a given voltage for $Cu_2ZnSnSe_4$/n-Si

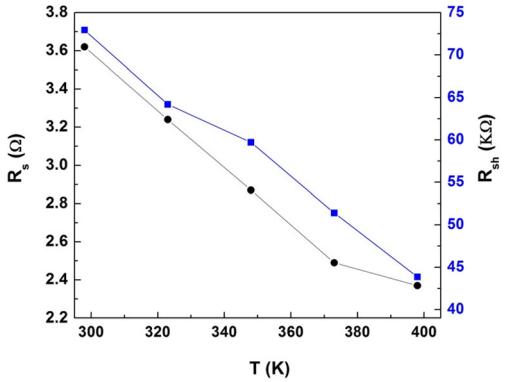

Fig. 5 Series and shunt resistance versus temperature for Au/$Cu_2ZnSnSe_4$/n-Si/Al heterojunction device

heterojunction under illumination are higher than that in the dark. This indicates that the light produce carrier contributing photocurrent due to the electron-hole pair production resulting from the light absorption [29]. The illumination was by halogen lamp of the power of 100 mW/cm^2.

The efficiency (η) of a solar cell is a parameter used to compare the performance of one solar cell to another. The efficiency (η) of a solar cell is given by [30].

$$\eta = \frac{P_{max}}{P_{in}} = \frac{FF \times V_{OC} \times I_{SC}}{P_{in}} \times 100\% \quad (7)$$

Where

η is the efficiency of a solar cell,
P_{max} is the output energy from the solar cell,
P_{in} is the input energy from the sun,
V_{oc} is the open-circuit voltage
I_{sc} is the short-circuit current,
FF is the fill factor.

Figure 6b shows the J–V graph of the Au/$Cu_2ZnSnSe_4$/n-Si/Al heterojunction at room temperature under light illumination of 100 mWcm^{-2}. The photovoltaic parameters of the $Cu_2ZnSnSe_4$/n-Si heterojunction were determined as 3.23 mA/ cm^2, 0.68 V, 2.14 mA/ cm^2, 0.4 V and 0.39 for J_{sc}, V_{oc}, J_M, V_M and FF, respectively. The solar conversion efficiency of the $Cu_2ZnSnSe_4$/n-Si heterojunction is 3.42% at room temperature. The low value of efficiency may be related to different factors such as the film thickness, the type and shape of the back contact for the fabricated device.

3.4 Dielectric Characteristics of the CZTSe /n-Si Heterojunction

The Rs-dc bias along the frequency scale points out that the device series resistance declines to less than half upon the application of dc bias resulting in an easier traffic for the charge carries. This effect is faintly enhanced with temperature. Consequently, applying negative or positive dc bias to this device causes a forward bias-like phenomenon; in addition, the temperature effect enhances the device's charge carriers making it more reliable as a photocell. At higher frequencies, 10^7 and 2e7 Hz, series resistance decreases drastically below 1e^3 Ohm and becomes almost dc bias independent as clarified in Fig. 7b. As seen the 3d figure gives more information than the 2d one, it clearly shows the whole frequency spectrum along with the dc bias as well for the selected parameter. In addition, one can estimate by a simple look the role of temperature on the specified parameter between both negative and positive dc bias. This is difficult, or even impossible, in 2d graphs for most cases. It is also noticed that a decline of the R_s peak's strength with frequency (20). This device can't be stated as an N or P-type as its conductivity is increased, more or less, linearly with both positive and negative bias and its response to negative bias is slightly better giving higher conductivity and vice versa with respect to R_s.

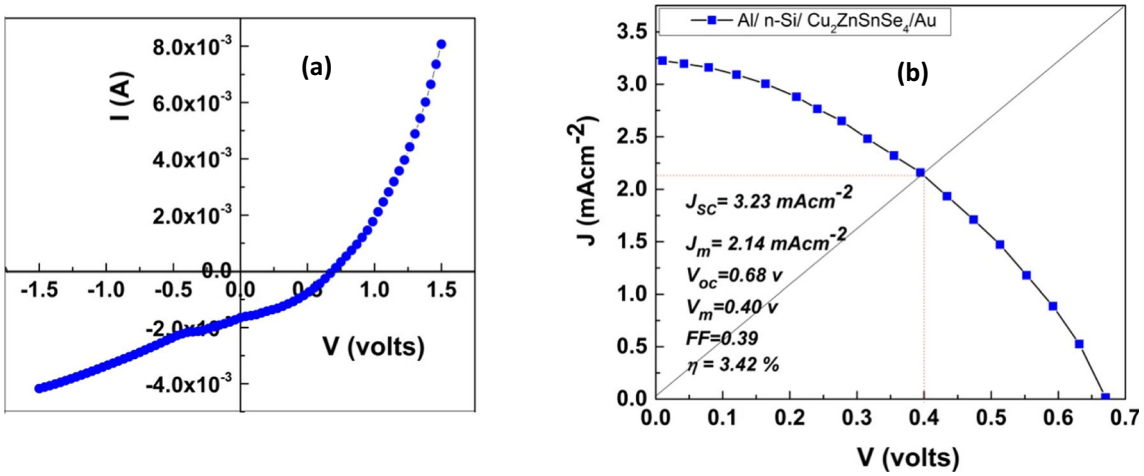

Fig. 6 **a** & **b**: **a** The I–V characteristics of Au/$Cu_2ZnSnSe_4$/n-Si/Al heterojunction device under illumination at room temperature, **b** The J–V characteristics for $Cu_2ZnSnSe_4$/n-Si heterojunction under illumination of 100 mWcm^{-2}

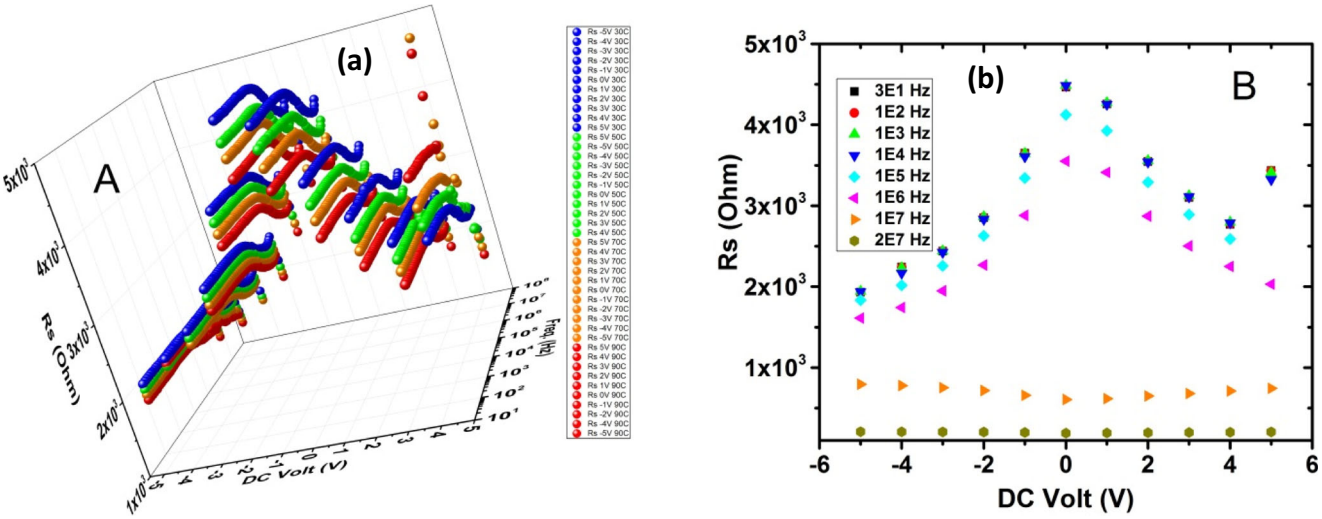

Fig. 7 **a** & **b**: **a** The series resistance behavior with dc bias along the whole frequency scale in 3d for all temperatures for the $Cu_2ZnSnSe_4$/n-Si heterojunction, **b** The series resistance behavior with dc bias at different frequencies in 2d for the $Cu_2ZnSnSe_4$/n-Si heterojunction

Conductivity demonstrates that the device gives a semiconductor behavior all over the dc bias range except at 5 V has a metallic behavior, Fig. 8. The current device has a good feature that its conductivity increases with both types of dc bias being more n-type than p-type. This feature means it can function well during the application of both dc bias types. Up to 1 MHz, we notice that the conductivity increases with frequency and with the decrease of the absolute of dc bias voltage as a result of the decrease of the series resistance [31–34]. At higher frequencies, 10^7 and $2*10^7$Hz, the reversal of the curve's behavior is not an issue as the conductivity has increased by an order, i.e. from 1e-4 to 1e-3 S/cm.

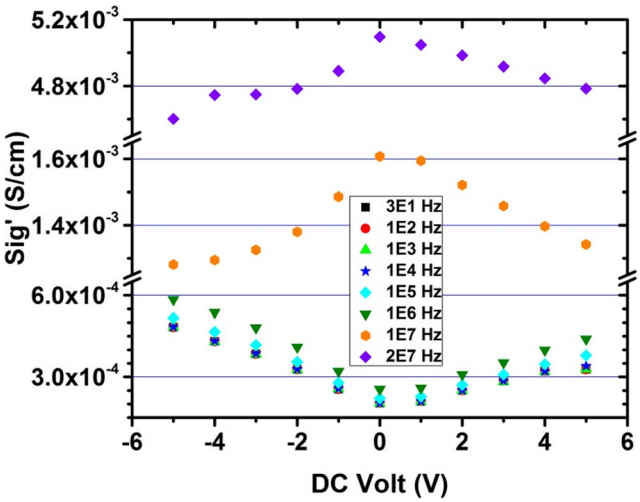

Fig. 8 The conductivity as a function of dc bias at 30 °C for the $Cu_2ZnSnSe_4$/n-Si heterojunction

Series capacitance is dependent on dc bias and frequency as excepted while it is slightly temperature dependent [35, 36]. In Fig. 9 capacitance-voltage behavior shows an inverted peak, compared to [37], at each frequency up to 1 MHz. the reason for this behavior is unknown to us, however, it wouldn't draw much attention since our device's efficiency as a solar cell is almost double that of reference [37]. The capacitance-voltage characteristic curve of the device has similar behavior as two forward biased Schottky diodes one for each dc bias polarity. Using the majority and minority charge carriers as a base to describe the situation for this unique device we can say that it contains both electrons and holes as charge carriers, with a slightly higher ratio of electron donors [38]. The capacitance of the device is a frequency and dc bias dependent. The interesting point here is the behavior of the device's capacitance reversing the capacitance-voltage response of ref. [37] which had a peak slightly below or above 0 dc bias depending on the components' ratio. Both devices have the same capacitance order, however, our device's capacitance increases with the absolute of the dc bias voltage. Rising the frequency leads to change in the C-V behavior through an intermediate step at 10^7 Hz then it follows the same pattern as that of the device made in ref. [37] but at 2×10^7 Hz. There a question upsurges out here, wondering whether this capacitance behavior is related to the efficiency of the device, as this device has double the efficiency of the one in the mentioned reference. Well, which we think is due to the success of the traditional liquid phase epitaxial method to creating a single crystal or at least high homogeneity in the resulting device, thus reducing the number of interface states among the different components of the device leaving only the series resistance of the device resulting crystal.

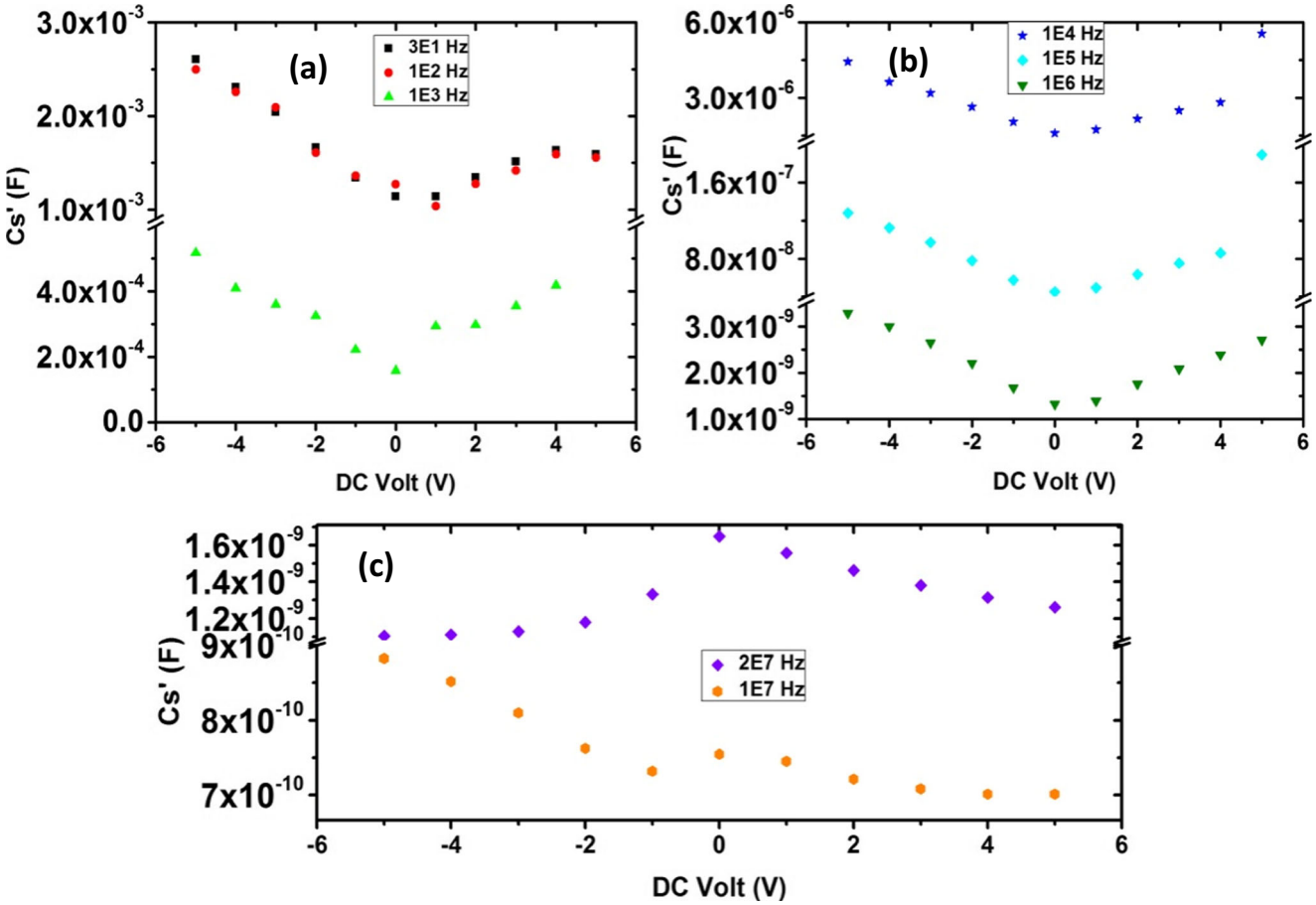

Fig. 9 **a–c**: The C-V curves of the $Cu_2ZnSnSe_4$/n-Si heterojunction at different frequencies

4 Conclusion

The Cu2ZnSnSe4 /n-Si heterojunction has been fabricated by liquid phase epitaxy technique. The current-voltage (I-V) characteristic of the Cu2ZnSnSe4 /n-Si heterojunction follows the thermionic emission mechanism in the temperature range (298–398 K). The effect of the temperature on the heterojunction parameters as series resistance (Rs) shunt resistance (Rsh), diode ideality factor (n) and the effective barrier height (ϕ_b) were determined from the dark I-V measurements. The solar parameters as short circuit current, open circuit voltages, fill factor and power conversion efficiency have been calculated from the current-voltage (I-V) characteristic curve under illumination. The efficiency of the Cu2ZnSnSe4/n-Si heterojunction is 3.42% at room temperature. The unique homogenous structure of the device reaching to a smart device that switches the charge carrier type automatically from electrons to holes depending on, and proportional to, the type of applied dc bias voltage as indicated from the dielectric analysis. In addition, it has a minimum of capacitance and conductivity and a maximum series resistance in the absence of dc bias voltage. Thus this structure allows the use of the device as a capacitance, conductivity and /or resistance switch for both ± dc voltage. Besides to it was used as a solar cell.

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