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ORIGINAL PAPER

Enhancement of a Nanoscale Novel Esaki Tunneling Diode Source TFET (ETDS-TFET) for Low-Voltage Operations

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Abstract

This paper presents a novel nanoscale tunnel FET consisting of an Esaki tunneling diode in the source region. A unique part of the source region is replaced by a heavily doped N-type silicon material establishing a tunneling diode inside the source region. Also, the gate metal is deliberately extended into the source region in order to more couple the created tunneling diode inside the source region. In the result of this new configuration, the band energy bending occurs inside the source region and also the potential barrier will be modified in the channel region thus increasing the ratio of I_{ON} to I_{OFF} (I_{ON}/I_{OFF}) and reducing the leakage current and ambipolar current for the proposed structure. The proposed structure has been compared with the conventional TFET and PNPN-TFET structure in terms of the I_{ON}/I_{OFF}, Leakage current, ambipolar current, drain-source conductance, short channel effects, source-drain capacitance and minimum noise figure showing a performance superiority with respect to other structures under the study.

Keywords Tunnel FET · Esaki tunneling diode · Band energy · Potential barrier

1 Introduction

The SOI technology based structures have been taken into account for attention in the VLSI circuits as a proper substitution for the MOSFETs. Since, scaling the MOSFETs is reaching the end of the semiconductor devices roadmap, a special effort has been done in order to characterize the SOI technology [1]. The substantial features in terms of reduced short channel effects, immunity to latch-up current, high voltage gain, and mitigated junction capacitances have made the SOI-MOSFET more proper than the MOSFET for the low-voltage applications [2, 3].

Improving the electrical performance of devices which are based on the SOI configurations, the novel and efficient structures utilizing the SOI concept have been proposed in the various literatures [4–8]. These structures are indeed an optimized version of a conventional SOI-MOSFET. Although, the SOI technology has been introduced as a solution to overcome the problems of MOSFETs, but it still suffers from the serious weaknesses which will gain a very serious situation when the its scale goes to the nanoscale limit. Therefore, the need for exploring the novel devices with different concept in the carrier transport is very vital.

The tunnel Field Effect Transistor (TFET) has been proposed as a modern structure for CMOS low voltage applications to supersede the MOSFETs and SOI-MOSFETs based structures [9–11]. Since the carrier transport in the TFETs is governed by the tunneling process in the source region, some main figures of merit such as low leakage current, steep subthreshold swing, good immunity to short channel effect and compatibility with the common CMOS process are explored [12–16].

Many structures which are based on the TFET technology have been designed to enhance the electric performance. A double-gate tunnel FET including High-K gate dielectric is introduced as a suitable device to increase the ON current [17]. It is worth noting that one of the biggest problems for the TFETs is related to the its ON current. Because, the carrier transport is controlled by the tunneling process.

In the other study, a lightly doped drain has been utilized in order to decrease the leakage current. The reason for the

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reduction of OFF current is predominantly related to thermal injection which is seen in the proposed device [18].

It should be pointed out that the most of the devices implemented based on the TFET are designed at double gate configuration to overcome the short channel effects with fabrication complexity cost. But, this paper has given an attractive solution to enhance the electric performance for a TFET based on the SOI technology which is very compatible with common CMOS process unlike the double gate TFETs.

This work has compared the proposed structure with the conventional TFET and the other novel PNPN-TFET in terms of the electric performance. The PNPN-TFET is generated by inserting a heavily doped N-type material inside the channel region beneath the main gate [19]. The reduction of the tunneling width happens to the PNPN-TFET device thus increasing ON current when compared with the conventional structure. Although, the TFET based on the SOI technology has been introduced as a good structure, but high subthreshold swing, high leakage current, high ambipolar current and especially the reduced ratio of ON current to OFF current (I_{ON}/I_{OFF}) are identified as the important problems of this device limiting its use for the nanoscale low voltage applications.

To overcome the substantial weaknesses of the PNPN-TFET structure, we have offered a new idea in order to reduce the leakage current by the formation of further potential barrier inside the channel region. Instead of inserting the N-type silicon material inside the channel region for increasing the tunneling current [19], the tunneling process have been transferred into the source region by embedding a N-type doped material inside the source region. Also for more coupling of gate electrode on the tunneling mechanism, the gate meal has been extended into device left side. Indeed, the proposed structure enhances ON current without reduction of the effective channel length in contrast to the PNPN-TFET structure. Only, a part of the source region has been attributed to the inserted N-type material for the proposed structure. The most important reason for the performance superiority in the proposed structure is the moving the peak junction electric field which is inside the channel region for the PNPN TFET toward the source region for the proposed device under the study. As a result, the band energy diagram is modified along the channel region and the leakage current and ambipolar current will be reduced caused by the raised potential barrier.

The current work has been arranged in six parts. The first part is about the introduction of the paper. The next one is about the explanation of the proposed structure skeleton. The third part is given to explain the governing physical equations for the proposed structure and also numerical scheme utilized in the simulation domain. Afterward, the improved parameters for the suggested device are given in part 4. Then, a technical consideration is proposed to reach the best electrical performance for the device under the study. Finally, whole the work is concluded, successfully.

2 Proposed Device Archituture

Figure 1 demonstrates a cross-sectional view of the proposed structure implemented in this work. The device includes an extra region inside the source region filled by a heavily doped N-type silicon material having the most important role in the electron transport. The additional embedded region is characterized by the width of Esaki tunneling diode (W) and the

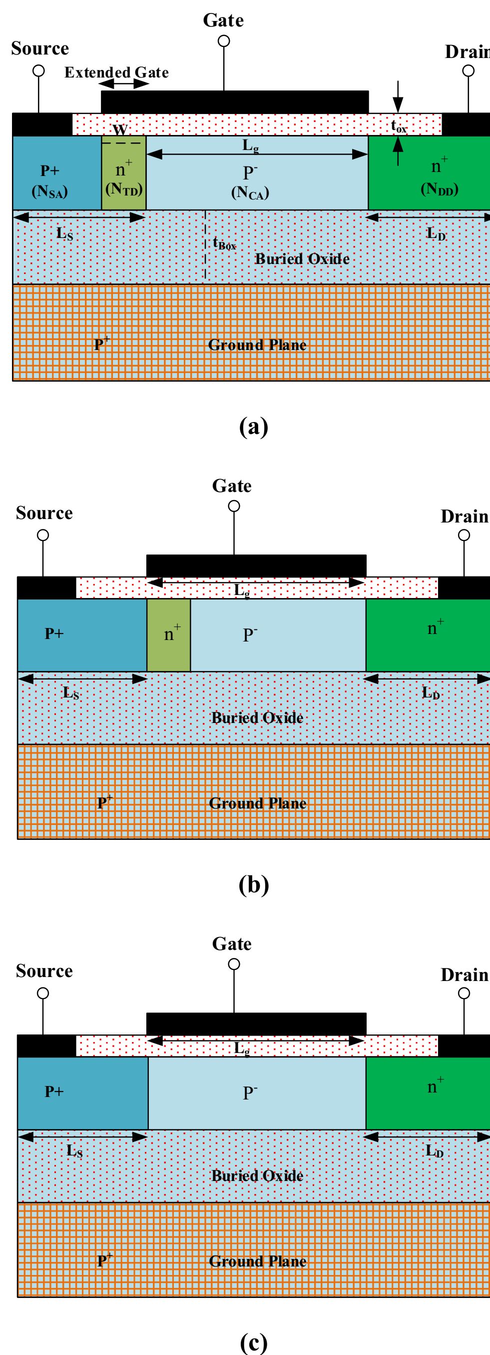

Fig. 1 The cross-sectional view of (**a**) the ETDS-TFET (**b**) the PNPN-TFET and (**c**) the conventional TFET structures implemented in the paper for the performance comparison

doping value (N_{TD}) as shown in the figure. It is worth noting that the depth of this region is equal to the channel region thickness. The figure has demonstrated three different types of the structures in terms of the conventional TFET, PNPN-TFET [19] and the proposed structure for the electrical performance comparison. Since, the proposed device handles the tunneling process inside the source region with the creation of an Esaki tunneling diode, it has been called as ETDS-TFET structure. As shown in the figure, the gate electrode is deliberately extended into the device left side in order to enhance the electrostatic coupling of the tunneling region. Instead of creating the peak junction electric field inside the channel region [19], we have created it inside the source region and modified it by the extension of the gate metal electrode toward the source region. Unlike the PNPN-TFET structure in which the channel region is utilized to change the shape of the band energy, the ETDS-TFET structure keeps whole the channel region along with the modification of the band energy throughout the channel region. Indeed, the PNPN-TFET shows a TFET with the gate length smaller than its typical length whereas it is not seen in the proposed structure.

To analyze the proposed device, Table 1 has listed the important parameters which are required for the simulation. It should be noted that all the parameters for the conventional TFET and PNPN-TFET structures are equivalent to those for the ETDS-TFET structure unless otherwise stated.

3 Fundemental Physical Equations and Numerical Scheme

In order to analyze the proposed device under the study, it is imperative to consider the proper mathematical models in the structures. Two important concepts in the cases of the electrostatic coupling and carrier transport must be taken into account for the simulation of the suggested device.

Table 1 List of essential parameters for the simulation of structures under the study

Parameters	ETDS-TFET
Gate length, L_g	22 nm
Source/drain region length, (L_S, L_D)	50 nm
Gate oxide thickness, t_{Ox}	1 nm
Silicon channel thickness, t_{Si}	10 nm
Buried oxide thickness, t_{Box}	25 nm
Doping concentration of channel region, N_{CA}	1×10^{17} cm^{-3}
Doping concentration of source region, N_{SA}	1×10^{20} cm^{-3}
Doping concentration of drain region, N_{DA}	5×10^{18} cm^{-3}
Doping concentration of Esaki tunneling diode, N_{TD}	1×10^{20} cm^{-3}
Width of Esaki tunneling diode, W	5 nm

The key equation stating a fundamental relation between the electric potential and space charge density is Poisson equation given as equation bellow:

$$div\left(\varepsilon_{(x,y)} \nabla \Psi\right) = q\left(n_{(x,y)} - p_{(x,y)} - N_{d(x,y)} + N_{a(x,y)}\right) \tag{1}$$

where $\Psi$is the electric potential referenced by the intrinsic potential, $\varepsilon_{(x,\,y)}$ is the dielectric permittivity of the proposed structure materials in the simulation domain, $n_{(x,y)}$, $p_{(x,y)}$, $N_{d(x,y)}$, and $N_{a(x,y)}$ are the electron density, hole density, donor doping concentration and acceptor doping concentration throughout the proposed structure grid points. It is worth noting that x and y are the grid points in the simulation domain and the unknown parameters are evaluated in this points.

The connection between the carrier transport and electric potential is performed by the carrier continuity equations as follow:

$$\frac{\partial n_{(x,y)}}{\partial t} = \frac{1}{q} div \overrightarrow{J_n}_{(x,y)} + G_{n(x,y)} - R_{n(x,y)} \tag{2}$$

$$\frac{\partial p_{(x,y)}}{\partial t} = -\frac{1}{q} div \overrightarrow{J_p}_{(x,y)} + G_{p(x,y)} - R_{p(x,y)} \tag{3}$$

$$\overrightarrow{J_n}_{(x,y)} = q\mu_{n(x,y)} \overrightarrow{F_n}_{(x,y)} + D_{n(x,y)} \nabla\left(n_{(x,y)}\right) \tag{4}$$

$$\overrightarrow{J_p}_{(x,y)} = -q\mu_{p(x,y)} \overrightarrow{F_p}_{(x,y)} + D_{p(x,y)} \nabla\left(p_{(x,y)}\right) \tag{5}$$

$$\overrightarrow{F_n}_{(x,y)} = -\nabla V_{(x,y)} - \frac{\nabla \chi_{e(x,y)}}{q} \tag{6}$$

$$\overrightarrow{F_p}_{(x,y)} = -\nabla V_{(x,y)} - \frac{\nabla\left(\chi_{e(x,y)} + E_{g(x,y)}\right)}{q} \tag{7}$$

It is worth noting that the variables $\mu_{n(x,\,y)}$, $D_{n(x,\,y)} = (KT_L/q)\mu_{n(x,\,y)}$ are the effective mobility and diffusion constant for the electrons. Note that the subscripts (p) at the equations are relevant to the holes. q is elementary charge, K is Boltzmann constant, and T_L is the local lattice temperature. The parameters $G_{(x,y)}$ and $R_{(x,y)}$ are the generation/recombination rates for the electron and hole. The parameters $\overrightarrow{J_n}_{(x,y)}$ and $\overrightarrow{J_p}_{(x,y)}$ are current density for the electron and hole, respectively. $\chi_{e(x,\,y)}$ and $E_{g(x,\,y)}$ are electron affinity and bandgap energy.

Regarding to the carrier transport for the structures based on the TFET, it is very important to consider the tunneling well-defined models for reaching realistic results. Two important tunneling models in terms of the local and nonlocal tunneling models have been utilized in the proposed structure in order to give an accurate current density for the devices under the study. Regarding to the local tunneling model, the Klaassen model is set to the simulation domain due to indirect transition of the silicon material as following:

$$G_{Klassen} = \alpha E^{\beta} \exp\left(-\frac{\lambda}{E}\right) \tag{8}$$

where $G_{Klassen}$ is the generation rate and also α, β and λ are the constant parameters given in the reference of [20]. Regarding to the equation, it is added to Eqs. (2) and (3) as electron and hole generation rate.

To accurately model the tunneling process, it is imperative to include the spatial variation of bands energy. Since the Esaki tunneling diode inserted inside the source region has been heavily doped, then we have applied the nonlocal band-to-band tunneling model in the simulation domain. Regarding to the tunneling process as the transfer of electron across the junction inside the source region, the current density for an electron with longitudinal energy E and transverse energy E_T is calculated as follow:

$$J(E) = \frac{q}{\pi\hbar}\iint T(E)\left[f_l(E+E_T) - f_r(E+E_T)\frac{\sqrt{m_e m_h}}{2\pi\hbar^2}\right]dEdE_T \tag{9}$$

where T(E) is the tunneling probability for an electron with longitudinal energy E.

$$f_l = (1+\exp(E+E_T-E_{Fl})/KT)^{-1} \tag{10}$$

$$f_r = (1+\exp(E+E_T-E_{Fr})/KT)^{-1} \tag{11}$$

where f_l and f_r are Fermi-Dirac function utilizing quasi-fermi level on the left hand side of junction (E_{Fl}) and on the right hand side of junction (E_{Fr}), respectively. Integrating Eq. (9) with respect to the transverse energy, the contribution to current from the longitudinal energy is obtained according to the equation bellow:

$$J(E)\Delta E = \frac{qKT\sqrt{m_e m_h}}{2\pi^2\hbar^3} \tag{12}$$

$$T(E)Log\left(\frac{(1+\exp(E_{Fr}-E)/KT)(1+\exp(E_{Fr}-E-E_{\max})/KT)}{(1+\exp(E_{Fl}-E)/KT)(1+\exp(E_{Fl}-E-E_{\max})/KT)}\right)\Delta E$$

where E_{max} is smaller value of $E-E_{lower}$ and $E_{upper}-E$. It is worth noting that the highest energy at which an electron can tunnel is E_{upper} and the lowest is E_{lower}. Hence, Eq. (12) gives the tunneling current density at a given perpendicular energy and the resulting current is added to the simulation domain at the x_{start} and x_{end} grid points. This is done and repeated for all the energy ranges between E_{lower} and E_{upper} in the tunneling region. We mention that the tunneling probability T(E) is given in [21].

In order to solve Eqs. (1–12), the finite difference discretization process is performed to numerically calculate the required variables in the grid points (x,y). The calibrated famous simulator of ATLAS which is from the SILVACO family is implemented in this work in order to numerically solve Eqs. (1) to (12) for the proposed structure at both DC and AC operations [21]. The most important models in terms of the transverse electric field dependent mobility, bandgap narrowing and Shockley-Read-Hall (SRH) recombination have been activated in the ATLAS for accurate calculations. To reach realistic results, the ATLAS simulator has been calibrated with an experimental data [22]. The various parameters in terms of the low-electric field mobility, energy relaxation time and electron saturation velocity have been modified for the best fitting.

4 Improvements for The ETDS-TFET Structure

The most important parameter in the case of the transverse characteristic have been evaluated for the conventional TFET, PNPN-TFET and ETDS-TFET structures as shown in Fig. 2. The drain current is measured at the bias $V_D = 0.7$ V for the different gate voltages. Regarding the figure, it is easily seen that the drain current of the conventional TFET is far less than that of the PNPN-TFET structure and the proposed structure. Since, there is an Esaki tunneling diode inside the source region in the ETDS-TFET then the tunneling width increases thereby enhancing the ON current. What makes the present work more attractive is related to the electric performance comparison between the PNPN-TFET and the ETDS-TFET devices. According to the figure, the ON currents are nearly the same at the operating bias $V_G = 0.7$ V for the PNPN-TFET and the ETDS- TFET structures. To better understand, three important parameters in terms of OFF current (I_{OFF}), I_{ON}/I_{OFF} and ambipolar current (I_{amb}) have been inspected and brought at the Table 2. I_{ON} is evaluated at the conditions of $V_G = V_D = 0.7$ V, I_{OFF} is evaluated at the biases of $V_D = 0.7$ V and $V_G = 0$ V and also $I_{ambipolar}$ is measured at the biases of $V_D = 0.7$ V and $V_G = -0.5$ V. Regarding the value of the OFF current, the proposed structure has given the least value among the conventional TFET and PNPN-TFET structures which is very desirable. Although, the PNPN-TFET device has presented

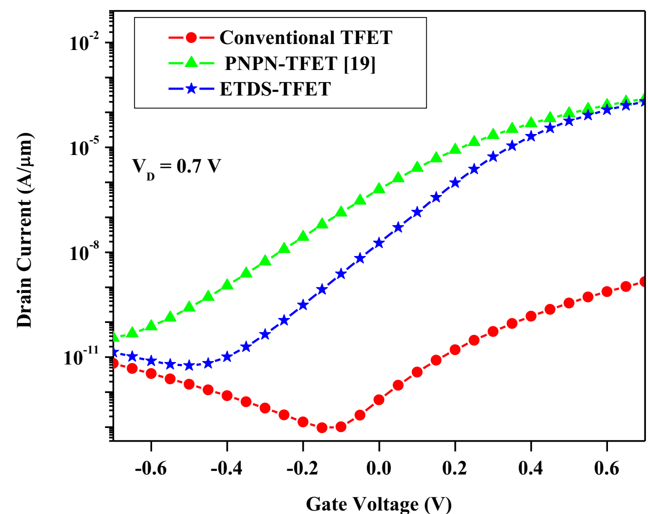

Fig. 2 Transfer characteristic for the ETDS-TFET, the PNPN-TFET and the conventional TFET structures

Table 2 The extraction of I_{OFF}, I_{ON}/I_{OFF} and $I_{ambipolar}$ for the ETDS-TFET and the PNPN-TFET structures

Parameter Structure	OFF current (I_{OFF})	Ratio of ON current to OFF current (I_{ON}/I_{OFF})	Ambipolar current, ($I_{ambipolar}$)
ETDS-TFET	1.8×10^{-8} A/μm	1.15×10^{4}	5.7×10^{-12} A/μm
PNPN-TFET [19]	6.3×10^{-7} A/μm	393.5	2.8×10^{-10} A/μm
Conventional TFET	6×10^{-13} A/μm	2.4×10^{3}	1.7×10^{-12} A/μm

higher I_{ON} than the conventional TFET but it suffers from a very low I_{ON}/I_{OFF} as compared to the common TFET. The situation is very good for the proposed structure since it has given a I_{ON}/I_{OFF} about 1×10^4 which is four orders of magnitude greater than that of the PNPN-TFET structure. Also, its value is more than that of the conventional TFET. Indeed, the insertion of Esaki tunneling diode inside the source region modifies the band energy profile along the channel region and the potential barrier increases resulting in decrease in the leakage current, considerably. This current is controlled by the thermionic mechanism and will be reduced owing to increased potential barrier for the proposed structure as compared to the PNPN-TFET structure. The other main parameter is related to ambipolar current. As shown in the table, the ETDS-TFET exhibits a reduced ambipolar current which is two orders of magnitude smaller than that of the PNPN-TFET structure. Hence, it can be stated that the proposed structure performance is much better than that of the conventional TFET and the PNPN-TFET structures for low-power applications.

To better become aware of governing physical mechanism in the proposed structure, the band energy profile along the middle of the channel region is plotted for the PNPN-TFET and the ETDS-TFET structures at the conditions of $V_D = 0.7$ V and $V_G = 0$ V as shown in Fig. 3. As an interesting exploration, it is evident from the figure that the potential barrier for the proposed structure is more than that for the PNPN-TFET structure. Embedding the Esaki tunneling diode inside the source region, the band energy profile gets an enhanced modification along the channel region thus resulting in increase in the conduction band energy inside the channel region when compared with the PNPN-TFET structure. One meaningful result is that the fewer electrons can overcome the potential barrier after tunneling from the Esaki tunneling diode inside the source region owing to increase in the potential barrier. Hence, the leakage current is considerably reduced. It is worth noting that the role of the potential barrier will be weak at the ON conditions since the gate coupling on the channel region increases and therefore available energy levels for tunneling the electrons enhances. The final result is that the ON current for the PNPN-TFET and ETDS-TFET structures is the same, nearly.

To better understand the performance of the proposed structure, current density have been graphically brought for the ETDS-TFET and the PNPN-TFET structures at the operating conditions of $V_G = 0$ V and $V_D = 0.7$ V as shown in Fig. 4. It is clearly observed from the figure that the opened path for the flow of electrons inside the channel region of the proposed structure has a more resistance as compared to that

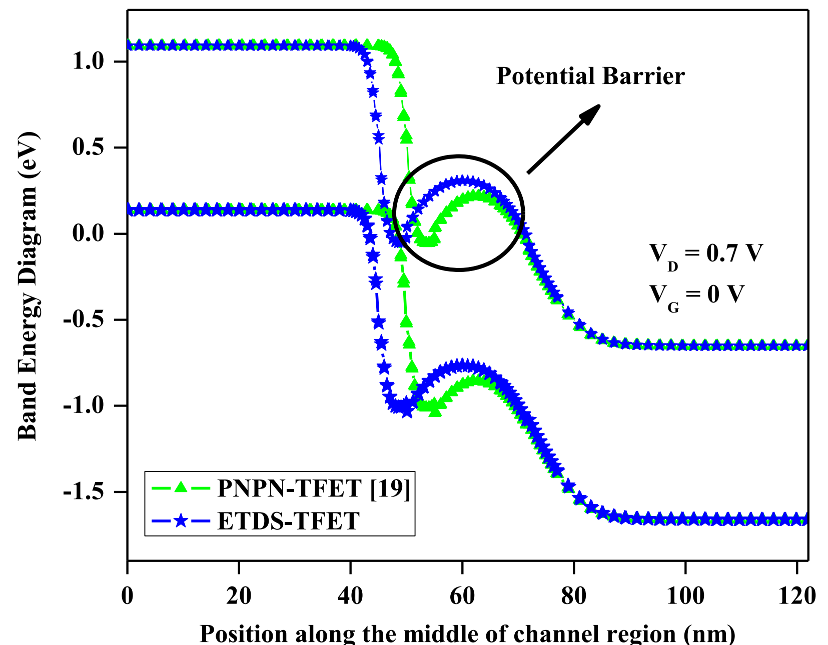

Fig. 3 Band energy profile along the middle of the channel region for the ETDS-TFET and the PNPN-TFET structures

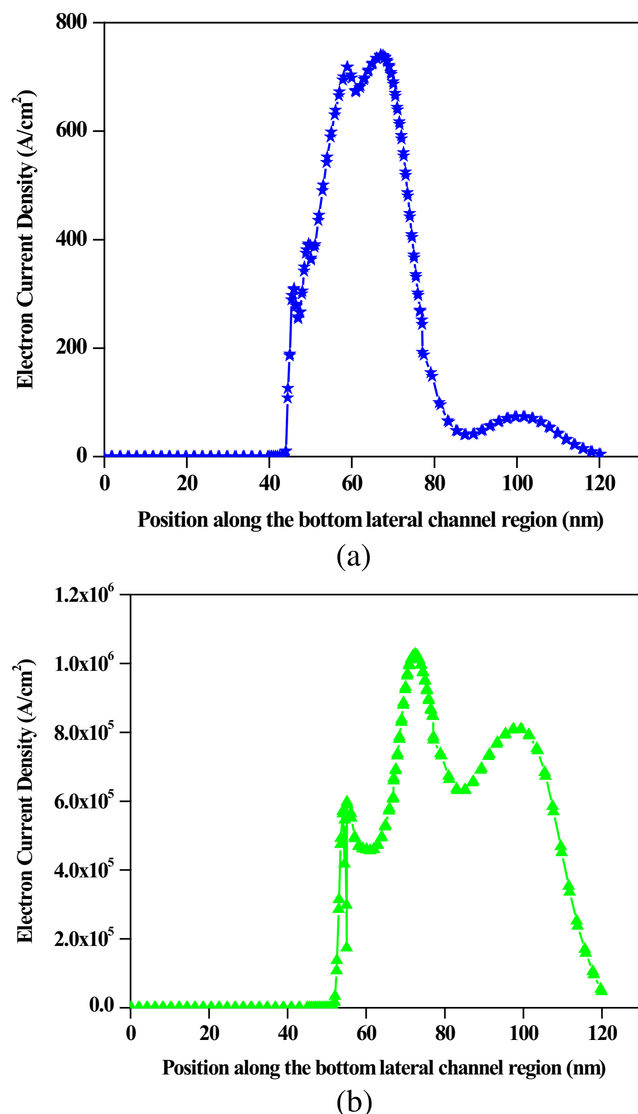

Fig. 4 Electron current density along the bottom lateral channel region for (**a**) the ETDS-TFET and (**b**) the PNPN-TFET structures

for the PNPN-TFET structure. This high resistance in the proposed structure causes the fewer electrons to obtain sufficient ability to reach the drain region thus reducing the current density, considerably.

The output characteristic for both the structures at the bias of $V_G = 0.7$ V has been shown in Fig. 5. Since, the Esaki tunneling diode has been created inside the source region, the effective resistance of this region increases thus reducing drain current, eventually. But, the reduction rate for the proposed structure is not considerable with respect to raised I_{ON}/I_{OFF} investigated at the pervious paragraphs. Moreover, one of the other improvements can be stated is about the output conductance. In the inset of Fig. 5, the drain conductance as a function of the drain voltage which is derivative of drain current over the drain voltage has been illustrated at the bias of $V_G = 0.7$ for the PNPN-TFET and the ETDS-TFET structures. It is evident from the figure that the drain conductance of the

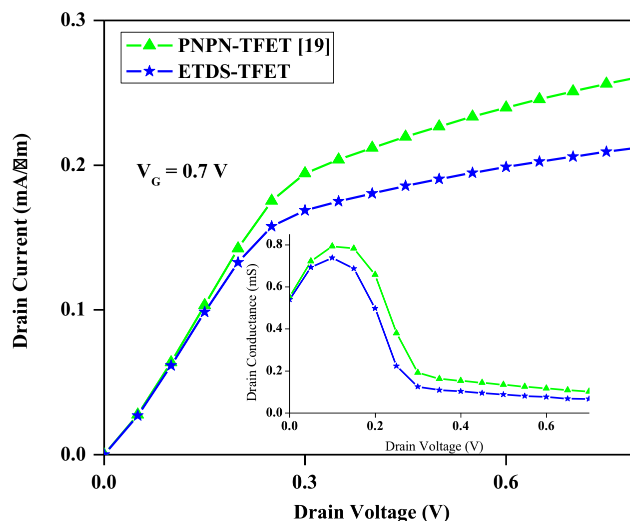

Fig. 5 The drain current as a function of the drain voltage for the ETDS-TFET and the PNPN-TFET structures. In the inset of the figure the drain-source conductance has been plotted

suggested device is less than that of the PNPN-TFET device promising a powerful isolation between the input and output ports. It can be sated that the peak junction electric field is transferred to the source region thus reducing the channel length modulation for the proposed structure. As a result, the drain conductance is successfully reduced.

Since the scaling of the devices are going to nanoscale regime by an aggressive growth, it is important to investigate the variation rate of threshold voltage for the structures. In this respect, the threshold voltage as a function of the channel length is brought at the bias of $V_D = 0.05$ V as shown in Fig. 6. The threshold voltage in this work is evaluated by calculating the maximum slope of V_G/I_D curve finding the intercept with the X axis (i.e. gate voltage) and then subtracting the half of the applied drain bias. The figure shows

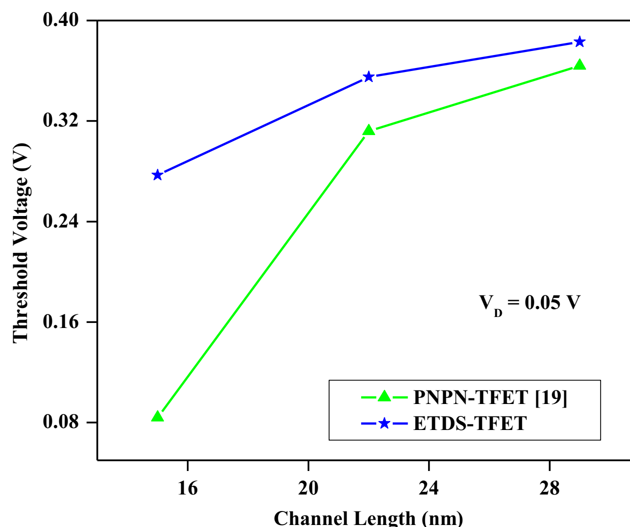

Fig. 6 Threshold voltage upon the channel length for the ETDS-TFET and the PNPN-TFET structures

that the variation rate of the threshold voltage for the ETDS-TFET structure is less than that for the PNPN-TFET structure. The depletion layer extension from the active regions into the channel region is more for the PNPN-TFET device when compared with the ETDS-TFET device. Therefore, it can be concluded that the proposed structure reliability is more than that of the PNPN-TFET structure at the low-voltage operations.

The subthreshold swing as an important factor defining the role of the short channel effect on the reliability of the nano-structure devices is investigated for the ETDS-TFET and the PNPN-TFET structures at the bias of $V_D = 0.7$ V as shown in Fig. 7. The subthreshold swing is defined as the inverse of derivative of drain current logarithm over the gate voltage at a specific drain voltage. Regarding the figure, the subthreshold slope has been reduced for the proposed structure as compared to the PNPN-TFET structure for the various gate lengths. Inspecting in the figure, there is a considerable difference between the subthreshold swing of the proposed structure and the PNPN-TFET structure at the channel length of 15 nm. Since, the tunneling process occurs inside the channel region for the PNPN-TFET it is expected that the effective channel length starts to dramatically decrease thus increasing the sub-threshold swing in contrast to the ETDS-TFET structure including the tunneling process inside the source region. Hence, the switching speed of the proposed structure is more than that of the PNPN-TFET structure for the low-power applications.

The improvements explored until now by the advent of the ETDS-TFET structure was related to the static electric performance. For more comprehensive comparison, the small signal performance of the structures under the study has been investigated in terms of the extraction of drain-source conductance, source-drain capacitance and the minimum noise figure. At first, the drain-source conductance as a function of the gate voltage is plotted at the conditions of $V_G = V_D = 0.7$ V for both the devices under the study at the operating frequency of f = 100 MHz as illustrated in Fig. 8. The ETDS-TFET structure revealed a less drain-source conductance than the PNPN-TFET structure showing an efficient device for the analog and digital circuits.

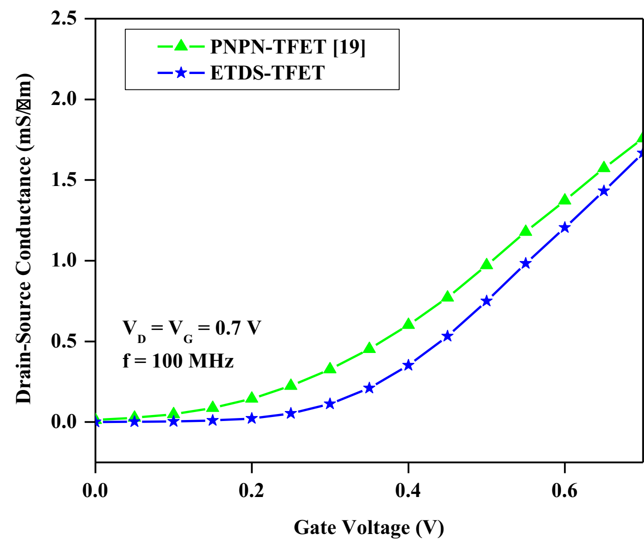

Fig. 8 AC drain-source conductance as a function of the gate voltage for the ETDS-TFET and the PNPN-TFET structures

Figure 9 demonstrates the source-drain capacitance as a function of the gate voltage at the conditions of $V_G = V_D = 0.7$ V for the proposed structure and PNPN-TFET structure at the frequency of 100 MHz. It is clearly seen form the figure that the source-drain capacitance is reduced owing to higher gate coupling of the ETDS-TFET on the channel region. Hence, the reduction of the parasitic capacitance in the ETDS-TFET device can boost the electrical performance for the small signal aims.

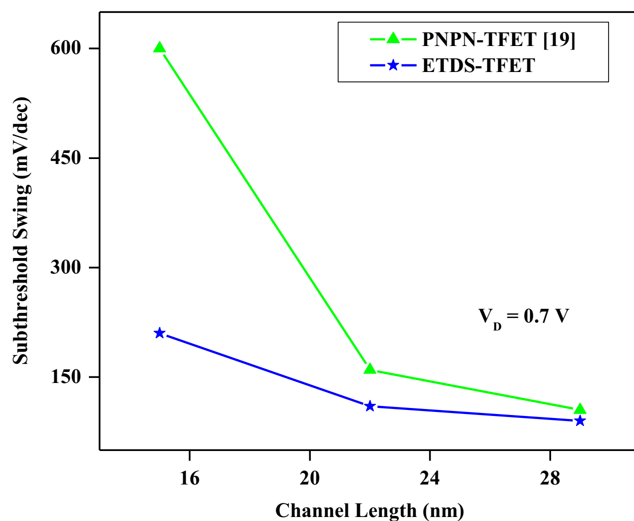

Fig. 7 Subthreshold swing upon the channel length for the ETDS-TFET and the PNPN-TFET structures

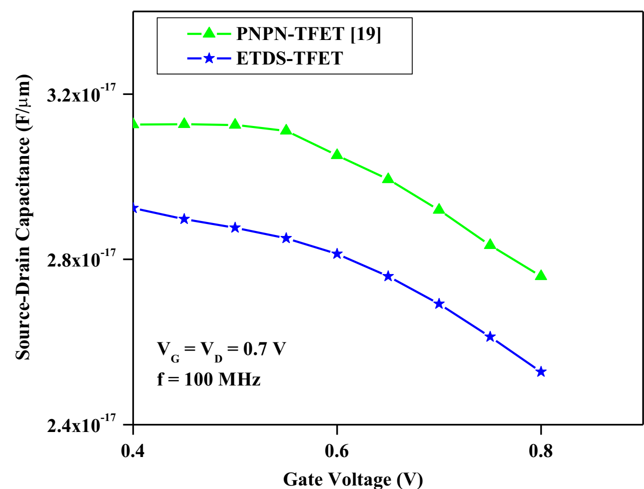

Fig. 9 Source-drain capacitance as a function of the gate voltage for the ETDS-TFET and the PNPN-TFET structures

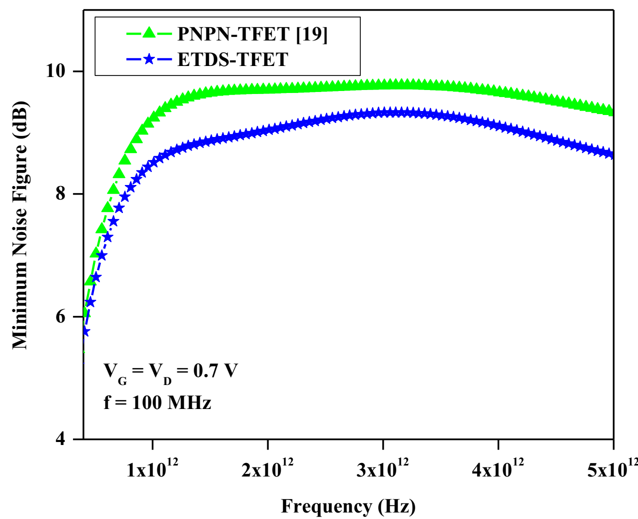

Fig. 10 Minimum noise figure versus the frequency for the ETDS-TFET and the PNPN-TFET structures

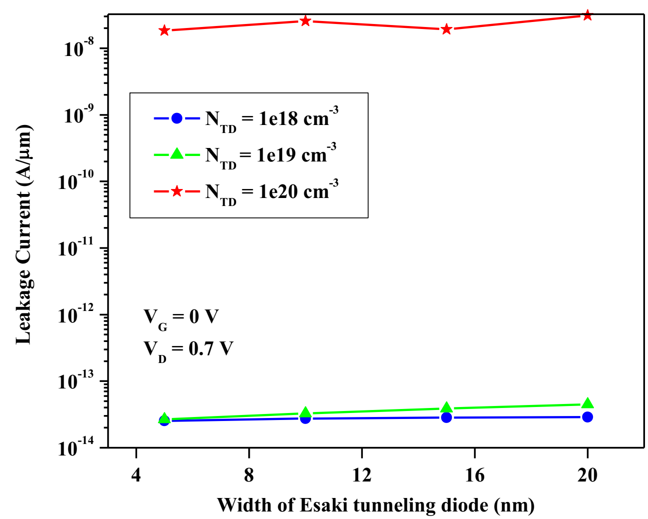

Fig. 12 Leakage current versus the Esaki tunneling diode width (W) and doping level (N_{TD}) for the ETDS-TFET structure

The inherent noise existence in the devices has been proved that can degrade the electrical performance. The minimum noise figure in the unite of dB versus the frequency as an important variable which can characterize the role of noise on the devices has been shown in Fig. 10 for the ETDS-TFET and the PNPN-TFET devices at the conditions of $V_G = V_D = 0.7$ V. The figure illustrates a decrease in the minimum noise figure for the proposed structure in contrast to the PNPN-TFET structure. One the meaningful result is that the proposed structure can operate with high reliability in the noisy environments when compared with the PNPN-TFET device.

5 Designing Considerations

The important structural parameters of the embedded Esaki tunneling diode inside the source region in the cases of the width (W) and the doping concentration (N_{TD}) have a significant influence on the electrical performance of the ETDS-TFET structure. Hence, a useful designing guideline has been proposed to reach the best proficiency when the device works at the low voltage operations. Figure 11 has shown the ON current as a function of the Esaki tunneling diode width (W) for the different doping levels of $N_{TD} = 1 \times 10^{18}$ cm^{-3}, $N_{TD} = 1 \times 10^{19}$ cm^{-3} and $N_{TD} = 1 \times 10^{20}$ cm^{-3}. As shown in the figure, the ON current is the highest for the situation of $N_{TD} = 1 \times 10^{20}$ cm^{-3}. The most important reason for this event is related to the formation of an Esaki tunneling diode with narrower tunneling width simplifying the transfer of the

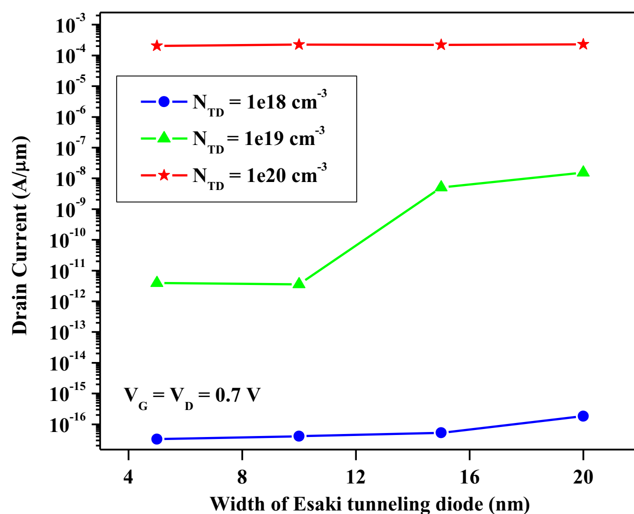

Fig. 11 ON current versus the Esaki tunneling diode width (W) and doping level (N_{TD}) for the ETDS-TFET structure

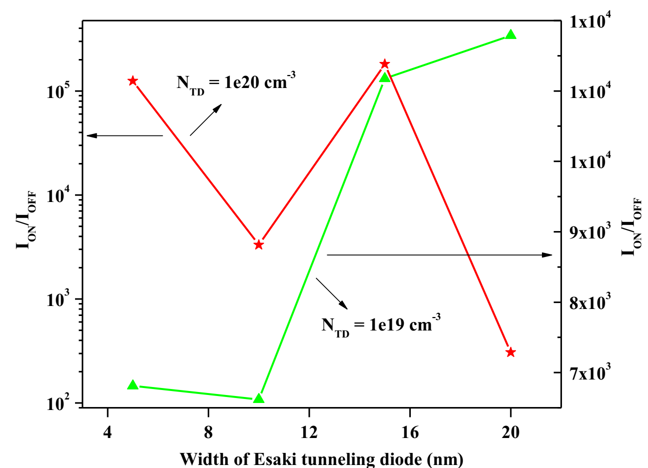

Fig. 13 Ratio of I_{ON} to I_{OFF} versus the Esaki tunneling diode width (W) and doping level (N_{TD}) for the ETDS-TFET structure

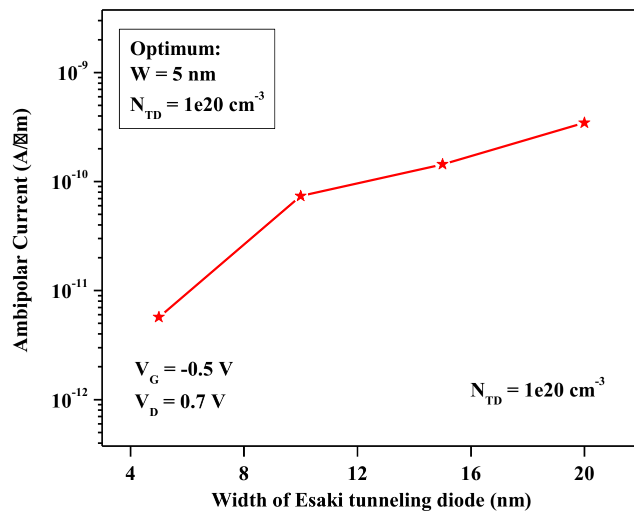

Fig. 14 Ambipolar current versus the Esaki tunneling diode width (W) for the ETDS-TFET structure

electron from the source region toward the drain region. In the next figure, the leakage current as a function of W has been illustrated for the aforementioned doping levels. As shown in Fig. 12, it is evident from the figure that the leakage current is more for the doping level of $N_{TD} = 1 \times 10^{20}$ cm^{-3}. The question may be asked is that what the doping level is proper for the proposed structure. In order to select the proper doping level, the key parameter in the case of I_{ON}/I_{OFF} versus the variable W is evaluated and plotted in Fig. 13. The figure shows higher I_{ON}/I_{OFF} for the W smaller than 16 nm at the doping level of $N_{TD} = 1 \times 10^{20}$ cm^{-3} when compared with that for $N_{TD} = 1 \times 10^{19}$ cm^{-3}. Since, this variable aggressively decreases at the doping level of $N_{TD} = 1 \times 10^{20}$ cm^{-3} for W greater than 16 nm, it is concluded that the high values of W are not proper. It should be noted that the ON current is very low for $N_{TD} = 1 \times 10^{19}$ cm^{-3} thus removing all the improvements of the ETDS-TFET device as compared to the conventional TFET and the PNPN-TFET devices. Regarding aforementioned texts, it is stated that the doping level of $N_{TD} = 1 \times 10^{20}$ cm^{-3} is proper as the final optimum doping level of the Esaki tunnel diode.

Regarding the selected doping level, Fig. 14 depicts the ambiolar current as a function of W. It is clearly observed form the figure that the ambipolar current is reduced when the variable W decreases. Indeed, increase in the variable W makes a more conductive source region thereby enhancing the ambipolar current. As a result, the optimum value of W = 5 nm has been selected for reaching the best electrical performance in the proposed structure.

6 Conclusion

The formation of an Esaki tunneling diode inside the source region of a conventional TFET has been proposed as a useful method in order to reduce the leakage current for the proposed structure. The new configuration increases the potential barrier inside the channel region thus decreasing the thermionic current and increasing I_{ON}/I_{OFF}. The performance comparison between the ETDS-TFET, the PNPN-TFET and the conventional TFET structures in terms of the leakage current, ratio of I_{ON} to I_{OFF}, threshold voltage variations, subthreshold swing, ambipolar current, drain-source conductance, source-drain parasitic capacitance and the minimum noise figure have displayed that the proposed structure can reach the best electrical performance for both the static and dynamic operations. Also, a designing guideline has been done in order to select the optimum characteristics of embedded Esaki tunneling diode. Hence, it is expected that the ETDS-TFET structure can attract the special attention of the researchers and experimentalists to implement it since it is a very proper candidate for the low power operations to supersede the conventional TFET and the PNPN-TFET structures.

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References

1. Colinge JP (2004) Silicon-on-insulator technology: materials to VLSI3rd edn. Kluwer Academic Publishers, London
2. Arnold E (1994) Silicon-on-insulator devices for high voltage and power IC applications. J Electro Chem Soc 141(7):1983–1988. https://doi.org/10.1149/1.2055040
3. Cristoloveanu S (2011) Trends in SOI technology: hot and green. J Korean Phys Soc 58(5):1461–1467. https://doi.org/10.3938/jkps.58.1461
4. Saremi M, Ebrahimi B, Afzali-Kusha A, Mohammadi S (2011) A partial-SOI LDMOSFET with triangular buried-oxide for breakdown voltage improvement. Microelectron Eng 51(12):2069–2076. https://doi.org/10.1016/j.microrel.2011.07.084
5. Jamali Mahabadia SE, Rajabi S, Loiacono J (2015) A novel partial SOI LDMOSFET with periodic buried oxide for breakdown voltage and self-heating effect enhancement. Superlattice Microst 85:872–879. https://doi.org/10.1016/j.spmi.2015.07.011
6. Moghadam HA, Orouji AA, Dideban A (2011) A novel 4H–SiC SOI-MESFET with a modified breakdown voltage mechanism for improving the electrical performance. Semicond Sci Technol 27(1):015001. https://doi.org/10.1088/0268-1242/27/1/015001
7. Anvarifard MK (2016) Successfully controlled potential distribution in a novel high-voltage and high-frequency SOI MESFET. IEEE Trans Device Mater Reliab 16(4):631–637. https://doi.org/10.1109/TDMR.2016.2618850
8. Zareiee M, Orouji AA (2017) Superior electrical characteristics of novel nanoscale MOSFET with embedded tunnel diode. Superlattice Microst 101:57–67. https://doi.org/10.1016/j.spmi.2016.11.022
9. Seabaugh AC, Zhang Q (2010) Low-voltage tunnel transistors for beyond CMOS logic. Proc IEEE 98(12):2095–2110. https://doi.org/10.1109/JPROC.2010.2070470
10. Barah D, Singh AK, Bhowmick B (2018) TFET on selective buried oxide (SELBOX) substrate with improved I_{ON}/I_{OFF} ratio and

reduced Ambipolar current. Silicon:1–9. https://doi.org/10.1007/s1263
11. Koswatta SO, Lundstrom MS, Nikonov DE (2009) Performance comparison between p-i-n tunneling transistors and conventional MOSFETs. IEEE Trans Electron Devices 56(3):456–465. https://doi.org/10.1109/TED.2008.2011934
12. Kumar MJ, Janardhanan S (2013) Doping-less tunnel field effect transistor: design and investigation. IEEE Trans Electron Devices 60(10):3285–3290. https://doi.org/10.1109/TED.2013.2276888
13. Saurabh S, Kumar MJ (2011) Novel attributes of a dual material gate nanoscale tunnel field-effect transistor. IEEE Trans Electron Devices 58(2):404–410. https://doi.org/10.1109/TED.2010.2093142
14. Molaei R, Saremi M (2018) A Resonant Tunneling Nanowire Field Effect Transistor with Physical Contractions: A Negative Differential Resistance Device for Low Power Very Large Scale Integration Applications. J Electron Mater 47(2):1091–1098. https://doi.org/10.1007/s11664-017-5823-z
15. Vishnoi R, Kumar MJ (2014) A pseudo-2-D-analytical model of dual material gate all-around nanowire tunneling FET. IEEE Trans Electron Devices 61(7):2264–2270. https://doi.org/10.1109/TED.2014.2321977
16. Molaei R, Saremi M, Vandenberghe WG (2017) A novel PNPN-like Z-shaped tunnel field-effect transistor with improved ambipolar behavior and RF performance. IEEE Trans Electron Devices 64(11):4752–4758. https://doi.org/10.1109/TED.2017.2755507
17. Boucart K, Ionescu AM (2007) Double-gate tunnel FET with high-κ gate dielectric. IEEE Trans Electron Devices 54(7):1725–1733. https://doi.org/10.1109/TED.2007.899389
18. Basak S, Asthana PK, Goswami Y, Ghosh B (2015) Leakage current reduction in junctionless tunnel FET using a lightly doped source. Appl Phys A Mater Sci Process 118:527–1533. https://doi.org/10.1007/s00339-014-8935-9
19. Jhaveri R, Nagavarapu V, Woo JCS (2011) Effect of pocket doping and annealing schemes on the source-pocket tunnel field-effect transistor. IEEE Trans Electron Devices 58(1):80–86. https://doi.org/10.1109/TED.2010.2089525
20. Hurkx GAM, Klaassen DBM, Knuvers MPG (1992) A new recombination model for device simulation including tunneling. IEEE Trans Electron Devices 39:331–338. https://doi.org/10.1109/16.121690
21. (2015) ATLAS device simulation software. Silvaco, Santa Clara, https://www.silvaco.com.
22. Kedzierski J, Boyd D, Zhang Y, Steen M, Jamin FF, Benedict J, Ieong M, Haensch W (2003) Issues in NiSi-gated FDSOI device integration. In: IEDM Tech. Dig., pp 18.4.1–18.4.4. https://doi.org/10.1109/IEDM.2003.1269317