Silicon (2018) 10:1021–1033
DOI 10.1007/s12633-017-9565-6

ORIGINAL PAPER

# Simulation Studies of Annealing Effect on a mc-Si Ingot for Photovoltaic Application

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Received: 10 September 2016 / Accepted: 17 April 2017 / Published online: 24 July 2017


**Abstract** A multi-crystalline silicon (mc-Si) ingot was grown by the directional solidification (DS) process for photovoltaic (PV) application. We have numerically investigated shear stress and thermal stress for different annealing time and temperature of the directionally solidified mc-Si ingot after the solidification and also we discuss the melt-crystal (m-c) interface during the solidification. Initially the planar m-c interface is observed during the solidification process, after that a slightly convex m-c interface is obtained for the rest of the solidification process. Maximum shear stress has least value at the center region of the mc-Si ingot for 900 K annealing temperature. Maximum shear stress has least value at the peripheral region of the mc-Si ingot for 700 K annealing temperature. The whole mc-Si ingot has lower thermal stress at 700 K annealing temperature. 5 h annealing time is enough to decrease the internal stress of the mc-Si ingot. Increase of the annealing time beyond 5 h does not further decrease the stress significantly.

**Keywords** Simulation · Multi-crystalline Silicon · Directional solidification process · Annealing effect · Stress

## 1 Introduction

Silicon solar cells play a crucial role in PV application. PV solar cells have advantages such as: 1. They can help to reduce the impact of $CO_2$ in the atmosphere and 2. The lifetime of PV solar panels is warranted up to 25 years. Silicon is the predominant material in PV markets and it is the second most abundant material on earth. 60% of the PV markets utilize the mc-Si solar cells. Most of the mc-Si wafers are produced by the DS process, because of its relatively simple operating process, low purity feed stock material, mass production, lower wastage during the cell processing and low cost [1, 2]. The DS process has heat conduction, convection and radiation. Anadha Babu et al. have [3] improved the mc-Si ingot quality using single layer silicon beads (SLSB) with silicon nitride coating. SLSB grown mc-Si have small grains, high percentage random grain boundary and low density of dislocation cluster. Yeh et al. have improved the mc-Si ingot by using the spot cooling method [4]. During the DS process what happens inside the furnace is very complicated, numerical simulation is the best tool to answer the "what happens inside the furnace?" [5]. From the simulation we can save money and time, we get information about the heat transfer characteristics inside the DS furnace during the solidification and cooling time. Carbon, nitrogen, oxygen and SiC impurity levels and their distribution on the mc-Si ingot are also estimated. In this DS process to control the thermal field and to control the m-c interface shape are very important, because they are directly related to the efficiency of the mc-Si ingot. Through the simulation suitable conditions can be obtained. Yang et al. have simulated the DS system to grow a mc-Si ingot. They mainly investigated the heat transfer characteristics for different pulling down rates of the crucible [6]. Gao et al. have simulated the DS process for the reduction of multi-nucleation near the crucible wall [7] and Black et al. have [8] numerically simulated the seeded DS furnace. Yang et al. have investigated numerical simulation and an experimentally modified DS furnace, from this investigation a conical insulation unit at the bottom of the hot zone is reported to

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have improved the mc-Si ingot quality [9]. From the addition of a side insulation partition block Ma et al. have [10] increased the conversion efficiency by 1.2% compared to the conventionally grown mc-Si solar cell. In this investigation simulation results validated the experimental results. Nagarajan et al. have [11] simulated a DS furnace for different crucible rotation and studied the carbon, nitrogen and oxygen impurity distribution on the mc-Si ingot. Srinivasan et al. have [12] numerically simulated a bottom grooved DS furnace to grow a mc-Si ingot for PV application. Wu et al. have studied impurities removal from metallurgical grade silicon by using gas blowing refining techniques and molecular dynamic simulation [13, 14]. DS grown mc-Si wafer efficiency was mainly affected by the dislocation density and impurities. They can be controlled by the m-c interface which influences thermal stress during the DS process. During the solidification the crystal cannot expand freely near the crucible, it will produce stress in the crystal. Uneven temperature distribution is the main reason for stress generation in the crystal. A slightly convex or planar m-c interface is favorable for a mc-Si ingot for PV application, because it reduces the multi-nucleation near the crucible wall and avoids the impurities formation inside the mc-Si ingot during the solidification. Many researchers working on the DS process look forward to modifying the DS process, to improve the quality and reduce the cost, adding external blocks and introducing new tricks on the cooling rate and gas flow velocity. Nguyen et al. have added the insulation blocks to control the m-c interface and reduce power consumption [15]. During the growth of a mc-Si ingot by the DS process annealing is most important, because it can reduce the internal stress and improve the structure of the mc-Si ingot. Hao et al. have increased the lifetime of a mono-silicon wafer by annealing at 723 K [16]. Gou et al. increased the lifetime of the mc-Si wafer with a three step annealing process [17]. Our main aim is to numerically simulate the suitable annealing time and temperature of a mc-Si ingot and analyze the melt-crystal interface during the solidification, shear stress and thermal stress at the final stage of the DS process.

## 2 Directional Solidification Process

The DS process is a simple operating process compared to the Czochralski (Cz) growth process. In this DS process there are five steps: First one is heating the furnace; before heating the furnace the feed stock materials are loaded in the quartz crucible. During the DS process lower purity feed stock material (Compared to Cz) can be used. Second one is melting; furnace is heated above 1600 K. After melting the silicon feed stock materials furnace is maintained for a few hours for homogenization of molten silicon. At the same time argon gas flows from the top position of the crucible. Third one is crystallization; after the melting furnace temperature is reduced for crystallization of molten silicon. The temperature at the crystallization interface was set at 1685 K. During the crystallization heater temperature is reduced and at the same time the side insulation basket is lifted in the upward direction. Heat flux is flowing through the bottom opening place, the nucleation starts at the bottom of the crucible, then the columnar mc-Si ingot is grown from the bottom to top direction. Dislocations are generated during the crystallization process. The efficiency of the mc-Si ingot depends on grain orientation and grain boundaries. Control of grain orientation and grain boundaries during the DS process is very difficult, however a lot of research is being done on this. Grain size was increased by the dendritic growth process and spot cooling method [4]. The seed assisted DS process is also tried to improve the mc-Si ingot but in this process the thermal stress is produced from the bottom seeds [18]. Moreover, during the crystallization process maintaining the planar or slightly convex m-c interface shape is important. Fourth one is the annealing process; the mc-Si ingot is annealed at various temperatures for a particular time (5 h) and then finally (Fifth one) the furnace is cooled.

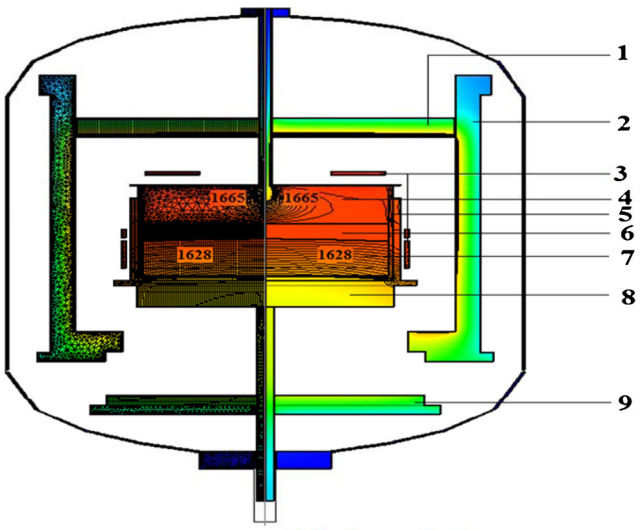



**Fig. 1** Schematic diagram of DS furnace

## 3 Mathematical Model

The temperature distribution of the DS system during the solidification process is calculated based on Fourier's fundamental laws of heat transfer. The governing equation of heat transfer is

$$-\nabla.(\lambda_{ik}\,\nabla T) + \rho\Delta H\frac{\partial f_s}{\partial t} = \rho C_p\frac{\partial T}{\partial t} \quad (1)$$

where T, $\rho$, $\lambda$, $C_p$, t and H are the temperature, density, thermal conductivity, heat capacity under constant pressure, time and latent heat respectively. Here, $f_s$ is the solid fraction of the mc-silicon during the directional solidification [12].

The thermal stress analysis is analysed using a displacement-based thermo-elastic stress model. The governing partial

**Table 1** Material properties

| Material | Properties | Values | Units |
|---|---|---|---|
| Argon | Heat conductivity | 0.01 | $W\,m^{-1}\,K^{-1}$ |
| | Heat capacity | 521 | $J\,kg^{-1}\,K^{-1}$ |
| | Dynamic viscosity | $P(T) = 8.466 \times 10^{-6} + 5.365 \times 10^{-8}T - 8.682 \times 10^{-12}T^2$ | Pa S |
| Graphite | Heat conductivity | $P(T) = 146.8885 - 0.17687T + 0.000127T^2 - 4.6899 \times 10^{-008}T^3 + 6.665 \times 10^{-012}T^4$ | $W\,m^{-1}\,K^{-1}$ |
| | Emissivity | 0.8 | |
| | Density | 1950 | $kg\,m^{-3}$ |
| | Heat capacity | 710 | $J\,kg^{-1}\,K^{-1}$ |
| Insulation | Heat conductivity | 0.5 | $W\,m^{-1}\,K^{-1}$ |
| | Emissivity | 0.8 | |
| | Density | 500 | $kg\,m^{-3}$ |
| | Heat capacity | 100 | $J\,kg^{-1}\,K^{-1}$ |
| Quartz | Heat conductivity | 4 | $W\,m^{-1}\,K^{-1}$ |
| | Emissivity | 0.85 | |
| | Heat capacity | 1232 | $J\,kg^{-1}\,K^{-1}$ |
| | Density | 2650 | $kg\,m^{-3}$ |
| Steel | Heat conductivity | 15 | $W\,m^{-1}\,K^{-1}$ |
| | Emissivity | 0.45 | |
| | Heat capacity | 1000 | $J\,kg^{-1}\,K^{-1}$ |
| | Density | 7800 | $kg\,m^{-3}$ |
| Si Melt | Heat conductivity | 66.5 | $W\,m^{-1}\,K^{-1}$ |
| | Emissivity | 0.3 | |
| | Density | $P(T) = 3194 - 0.3701T$ | $kg\,m^{-3}$ |
| | Melting temperature | 1685 | $kg\,m^{-3}$ |
| | Surface tension | 0.7835 | $N\,m^{-1}$ |
| | Dynamic viscosity | 0.0008 | Pa S |
| | Heat capacity | 915 | $J\,kg^{-1}\,K^{-1}$ |
| | Wetting angle | 11 | Deg |
| | Latent heat | 1800000 | $J\,kg^{-1}$ |
| Si crystal | Heat conductivity | $P(T) = 110.6122042 - 0.1507227384T + 0.0001093579825T^2 - 4.009416795 \times 10^{-008}T^3 + 5.66839358 \times 10^{-012}T^4$ | $W\,m^{-1}\,K^{-1}$ |
| | Emissivity | $P(T) = 0.9016 - 0.00026208T$ | |
| | Density | 2530 | $kg\,m^{-3}$ |
| | Latent heat | 1800000 | $J\,kg^{-1}$ |
| | Heat capacity | 1000 | $J\,kg^{-1}\,K^{-1}$ |

differential equations for momentum balance in an axisymmetric model [19] can be written as,

$$\frac{1}{r}\frac{\partial}{\partial r}(r\sigma_{rr}) + \frac{\partial}{\partial z}(\sigma_{rz}) - \frac{\sigma_{\phi\phi}}{r} = 0 \tag{2}$$

$$\frac{1}{r}\frac{\partial}{\partial r}(r\sigma_{rz}) + \frac{\partial}{\partial z}(\sigma_{zz}) = 0 \tag{3}$$

where $\sigma_{rr}$, $\sigma_{zz}$ and $\sigma_{\phi\phi}$ are normal stresses in the radial, axial and azimuthal directions, respectively, and $\sigma_{rz}$ is the shear stress, r is radius and z is height. Integrating the above equation in the control volume V of a solid material bounded surface S and substituting the stress-strain equation, we get the von Mises stress [5] as

$$\sigma_{von} = \left(\frac{3}{2}S_{ij}S_{ij}\right)^{\frac{1}{2}} \tag{4}$$

where $S_{ij}$ is the stress deviator

$$S_{ij} = \sigma_{ij} - \frac{1}{3}\sigma_{kk}\delta_{ij}$$

$\delta_{ij}$ is Kronecker delta, $\sigma_{ij}$ and $\sigma_{kk}$ are stress components.

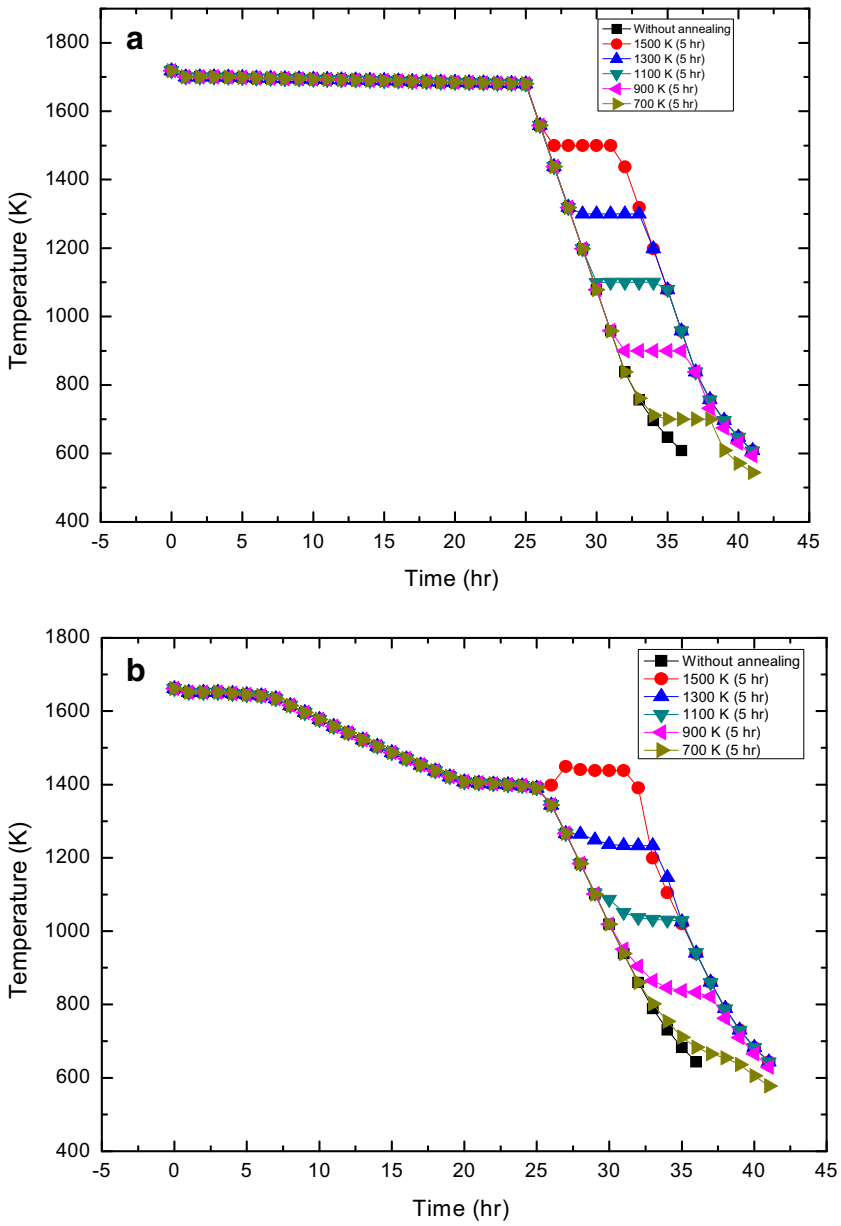



**Fig. 2** Temperature profile of TC1 (**a**) and TC2 (**b**) at 1500 K, 1300 K, 1100 K, 900 K and 700 K annealing temperatures for annealing time of 5 h

In the Alexander-Haasen (AH) model, the creep strain rate and the multiplication rate of the mobile dislocation density can be expressed as follows:

$$\dot{N}_m = K k_0 (\tau_{eff})^{p+\lambda} \exp\left(-\frac{Q}{kT}\right) N_m \tag{5}$$

$$\tau_{eff} = \sqrt{J_2} - D\sqrt{N_m} \tag{6}$$

$$J_2 = \frac{1}{S_{ij} S_{ij}} \tag{7}$$

where $\tau_{eff}$ is effective stress, k is the Boltzmann constant, T is absolute temperature in the silicon crystal, $N_m$ is density of mobile dislocations, $S_{ij}$ is deviatory stress, $J_2$ is second invariant of the deviatoric stress, D is strain hardening factor, $k_0$, K, p and $\lambda$ are material constants [20].

## 4 Numerical Model

Simulation is started from the melting stage, by using the Finite Volume Method (FVM). Structured and unstructured grids are used during the simulation. FVM is suitable to solve the structured and unstructured mesh. The schematic diagram of the DS furnace is shown in Fig. 1. The left side shows quadrangular and triangular grids generated to solve the heat conduction, convection and radiation problems. Furnace parts are shown in the right side. The DS furnace has silicon melt, silicon crystal, argon, insulation, quartz crucible, heaters, heat exchanger block and steel cover. In the numerical model a two-dimensional axisymmetric based on the real DS furnace was assumed, melt was assumed as Newtonian fluid, argon gas was treated as an ideal gas and incompressible, all radiative surfaces are diffuse gray [21–24]. There are totally 22 blocks. They contain 8528 meshes, quadrangular and triangular. Silicon melt, silicon crystal, heater, heat exchanger blocks contain structured cells and argon, insulation, crucible and steel cover have unstructured cells. Mesh size of silicon melt, silicon crystal, heater and heat exchange block are corresponds to 0.92929 $cm^2$, 0.6977 $cm^2$, 0.4760 $cm^2$ and 0.89748 $cm^2$. Material properties are shown in Table 1. The annealing process is numerically simulated. The annealing is done for 5 h at various temperatures, such as 1500 K, 1300 K, 1100 K, 900 K and 700 K. The results of "with annealing process" and "without annealing process" are compared. Numerical simulation is done by the Crystal Growth Simulator (CG Sim) provided by the Semiconductor Technology Research (STR) Group, Russia. Unsteady global simulation was simulated with time varying temperature profile of heater and side insulation movement. 1685 K temperature was set at the m-c interface.

## 5 Results and Discussion

In the DS process the heat transfer plays a crucial role and it is a complicated problem during the DS process. If we can control the temperature distribution we can get good quality mc-Si ingot. Here the heat transfer is controlled by the adjustment of heater temperature and opening the side insulation basket. A thermocouple TC1 was placed on the center of the side top heater, it was adjusted for the cooling rate of 0.9 K/h during the crystallization time. At the end of crystallization the cooling was adjusted for 2 K/min until the annealing temperature is reached. After the 5 h annealing process it was again adjusted for 2 K/min until room temperature was obtained. TC2 was placed on the top center of the heat exchanger block. The side insulation basket had been moved at 0.2 mm/min up to 200 mm height and after that kept constant until the end of the process. During the annealing process the insulation basket was closed. Temperature profiles of TC1 and TC2 at various annealing processes are shown in Fig. 2.

### 5.1 Melt-Crystal Interface

The quality of the mc-Si ingot depends on the m-c interface. The melt-crystal interface is shown Fig. 3. The DS model is an axis symmetry model. Figure 3 shows the melt-crystal

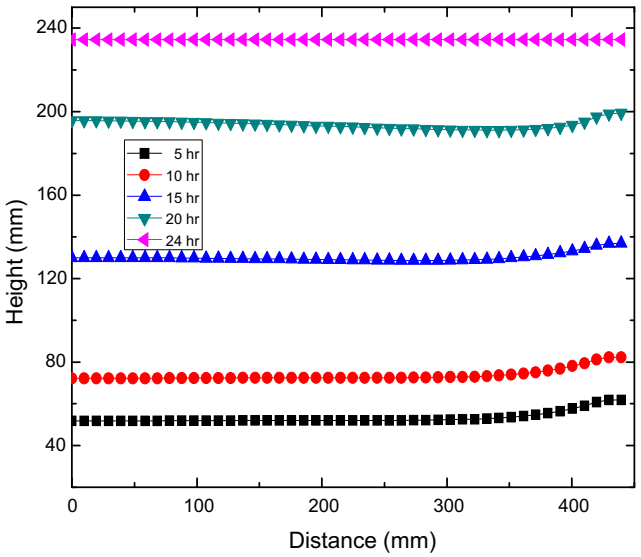



**Fig. 3** Melt-crystal interface at various growth times

interface at various crystallization times. The m-c interface lines are identified by the isothermal line of 1685 K. The crystallization is more in the center region for a convex m-c interface. The crystallization is more in the peripheral region for a concave m-c interface shape. The melt-crystal interface shape has a significant role during the crystal growth. The interface shape represents the isotherm line of melting point of the material. A planar m-c interface is beneficial to remove the impurities, eliminate the defects, reduce the thermal stress and it helps to grow a columnar mc-Si ingot [25]. The distance between the center to peripheral region is 439 mm and ingot height is 235 mm. Initially (5 and 10 h) the m-c interface is near to planar up to 390 mm from the center region of the mc-Si ingot. After that it has a slightly convex interface shape. It is shown in Fig. 3. Differences between the center to peripheral region of 5, 10, 15 and 20 h crystallization times are 11, 10, 8 and 5 mm. At the end of the peripheral region a slightly convex shape occurs due to the crucible heat conduction. The m-c interface is more important in the DS process because it affects the stress and growth rate. A slightly convex or planar interface is favored for crystal growth because it pushes the impurity away during the crystallization time. A planar or slightly convex m-c interface prevents multi-nucleation near the cru-

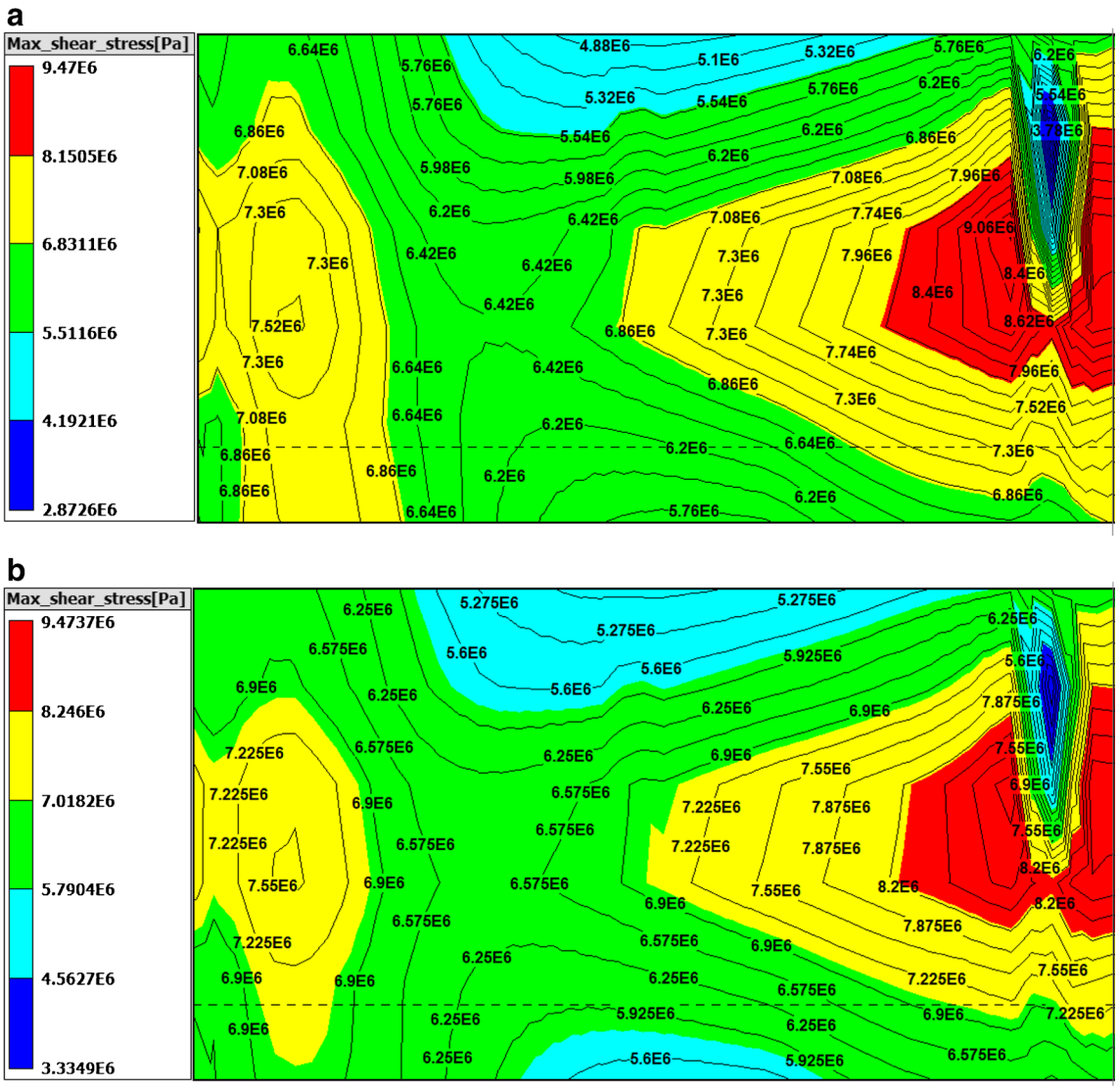



**Fig. 4** Maximum shear stress on mc-Si ingot for various annealing temperature for 5 h **a** (without annealing), **b** (1500 K), **c** (1300 K), **d** (1100), **e** (900 K) and **f** (700 K)

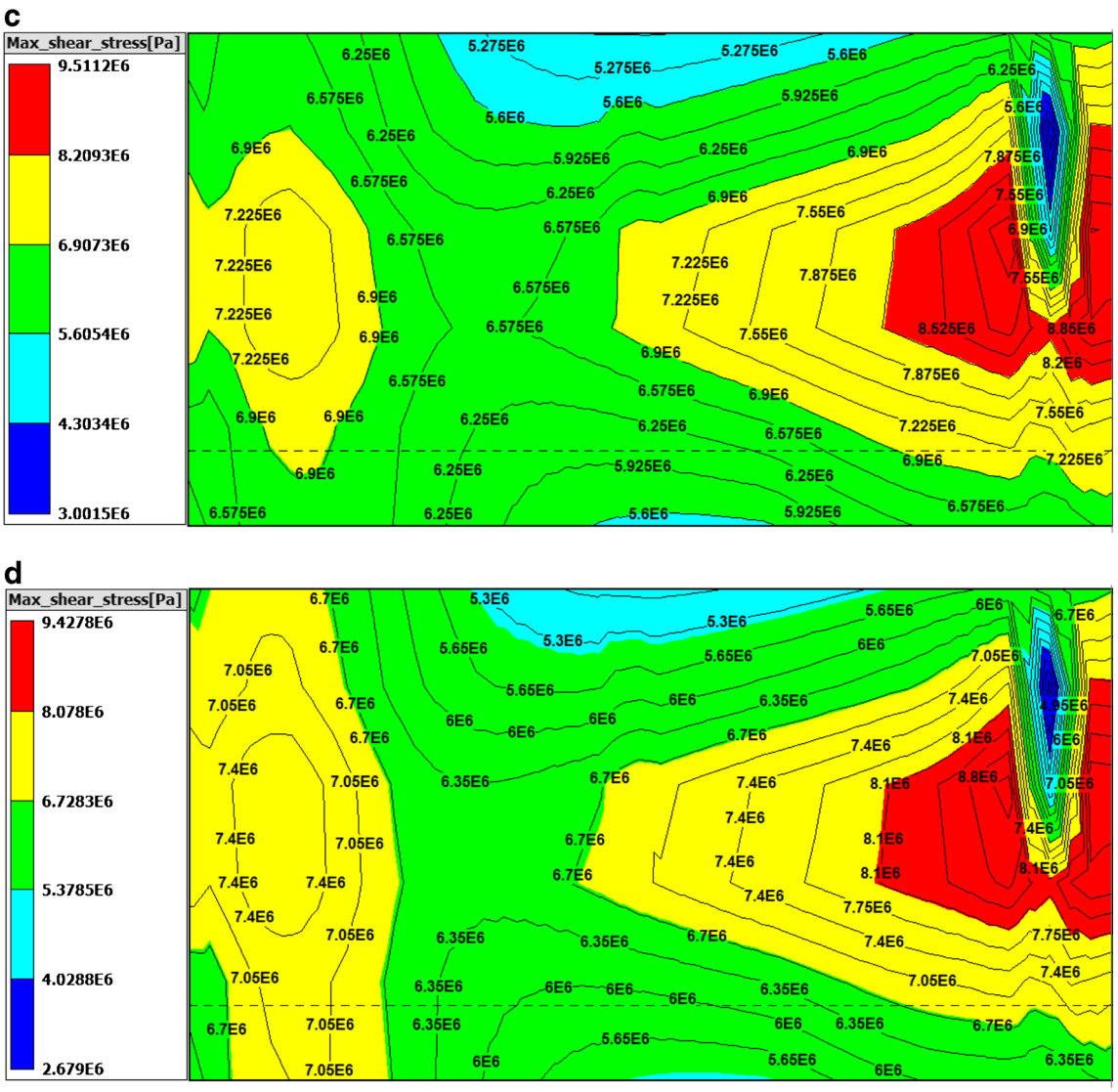



**Fig. 4** (continued)

cible, this can be helpful to reduce the thermal stress on the mc-Si ingot. In the DS process the crystal grows from bottom to top. Outward growth direction of the mc-Si ingot growth during the DS process is beneficial for PV application, because during the outward growth direction the grain size is enlarged, then the columnar ingot is growing and the multi-nucleation is avoided at the place near to the crucible, meaning the defects are reduced. TC1 was adjusted to have a cooling rate of 0.1, 0.3, 0.6, 0.9, 1.2 and 1.5 K/h keeping side insulation movement speed 0.2 mm/min every time. TC1 cooling rate of 0.9 K/h resulted in the most favorable interface. Then the mc-Si ingot quality was improved by the annealing process. The annealing treatment was given at the end of crystallization.

### 5.2 Maximum Shear Stress

During the annealing treatment the structure of the ingot is mainly improved. It means shearing of the mc-Si ingot is decreased. When shearing is reduced the line defects and point defects are reduced. The mc-Si ingot has compressive force from the crucible because during the growth the silicon crystal expands 10% when the melt is crystallized. All the annealing treatments are done for 5 h duration at various

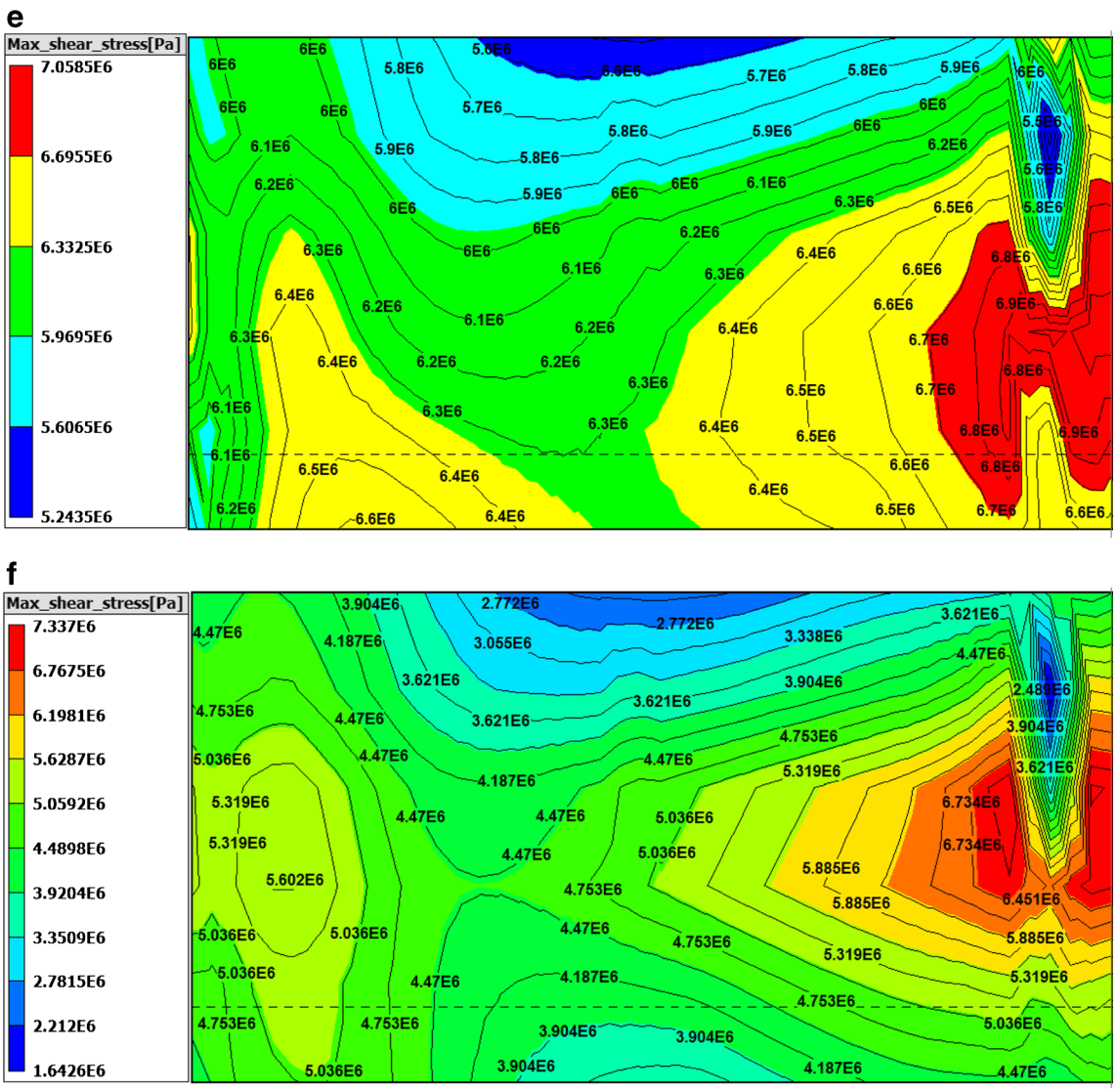



**Fig. 4** (continued)

temperatures. Figure 4 shows maximum shear stress at different annealing temperatures (1500 K, 1300 K, 1100 K, 900 K and 700 K) and the results of "with annealing process" and "without annealing process" are compared. Without annealing treatment the mc-Si ingot has a maximum shear stress of 9.47 MPa. Increase of the annealing temperature increases the axial temperature gradient and thus increases the stress also. The maximum axial temperature gradient is 62 K/m for without annealing treatment and for 1500 K, 1300 K and 1100 K annealing treatment. It decreases to 56 K/m for 900 K annealing treatment and 39 K/m for 700 K annealing treatment. It is shown in Fig. 5. The maximum stress is reduced to 7 MPa at 900 K. Maximum shear stress has least value at the center region of the mc-Si ingot for 900 K annealing temperature. Maximum shear stress has least value at the peripheral region of the mc-Si ingot for 700 K annealing temperature. The whole mc-Si ingot has lower maximum shear stress at 700 K annealing temperature, because in this case there is a lower axial and radial temperature gradient. It is shown in Fig. 5. Takahashi et al. have calculated the shear stress of a mc-Si using finite element analysis of the order of MPa [26]. In Fig. 6 is shown maximum shear stress values at 5 h, 10 h, 15 h and 20 h annealing treatment at different annealing temperatures (1600 K, 1500,

1400 K, 1300 K, 1200 K, 1100 K, 900 K, 800 K and 700 K). The shear stress is minimum at 900 K annealing treatment process at the center region than other heat treatments. Figure 6 shows that increasing the annealing time above 5 h does not decrease stress any further. For increasing the annealing time it requires a large amount of power.

### 5.3 Thermal Stress

The conversion efficiency of the mc-Si ingot mainly depends on the dislocation density, it is born on the mc-Si ingot at the higher stress level. Von Mises stress is thermal stress, it is a combination of shear and normal stress. To enhance the mc-Si ingot quality, thermal stress should be reduced. Due to the annealing thermal stress decreases due to the atoms rearrangement. Figure 7 shows thermal stress for "without annealing treatments" and various "annealing treatments", 1500 K, 1300 K, 1100 K, 900 K and 700 K. All annealing treatments are treated for 5 hr. Without annealing the mc-Si ingot has thermal stress 1.9 E7 Pa. At higher annealing temperature there is no significant change, below 1000 K thermal stress is decreased. 700 K and 900 K annealing results in lower thermal stress (1.4 E7 Pa) at the center region than other heat treatments. Thermal stress has least value (of the order of MPa) at the peripheral region of the mc-Si ingot for 700 K annealing temperature, because of lower axial and radial temperature gradient. The thermal

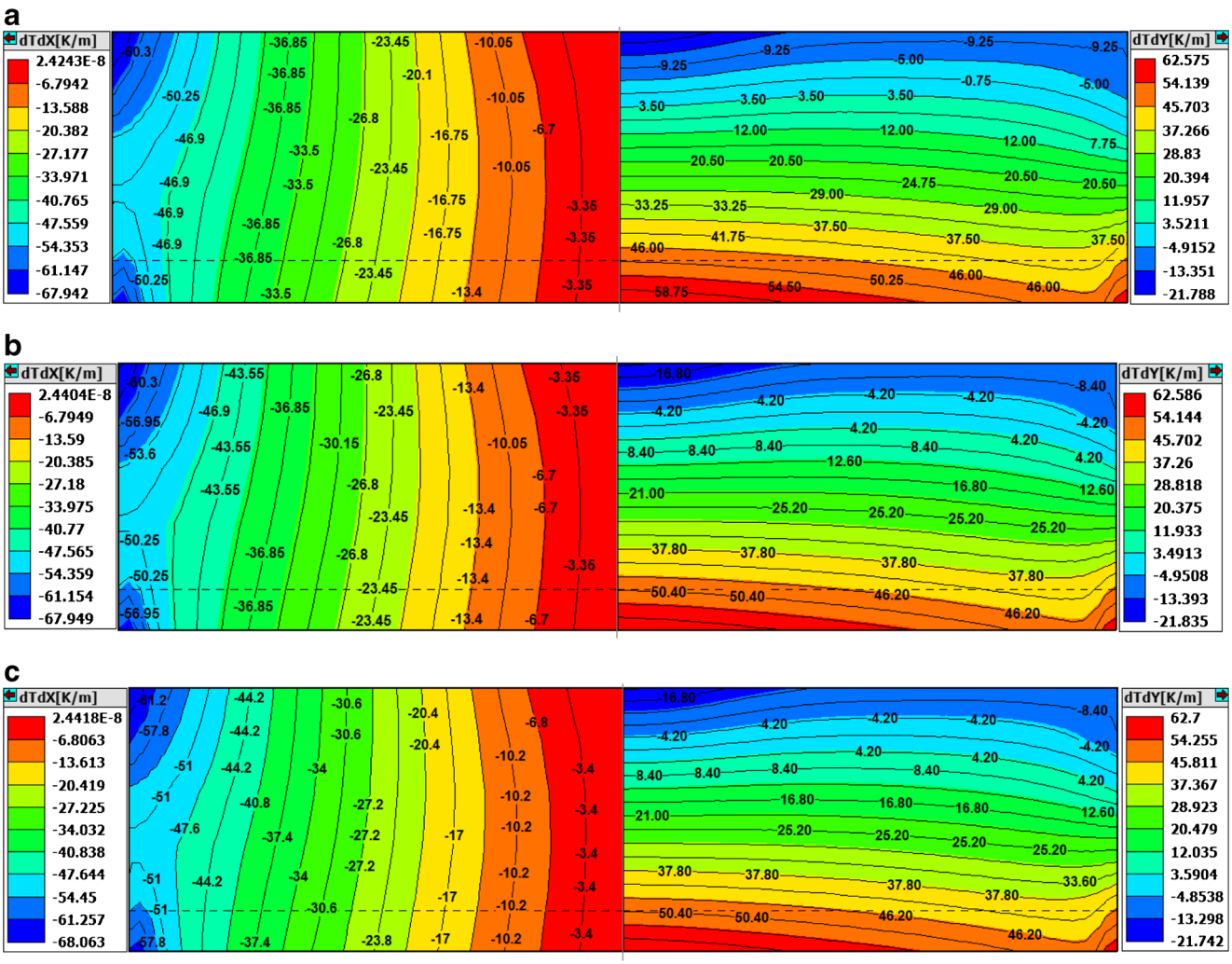



**Fig. 5** Axial (*Left side*) and vertical (*Right Side*) temperature gradient on mc-Si ingot for various annealing temperature for 5 h **a** (without annealing), **b** (1500 K), **c** (1300 K), **d** (1100), **e** (900 K) and **f** (700 K) annealing

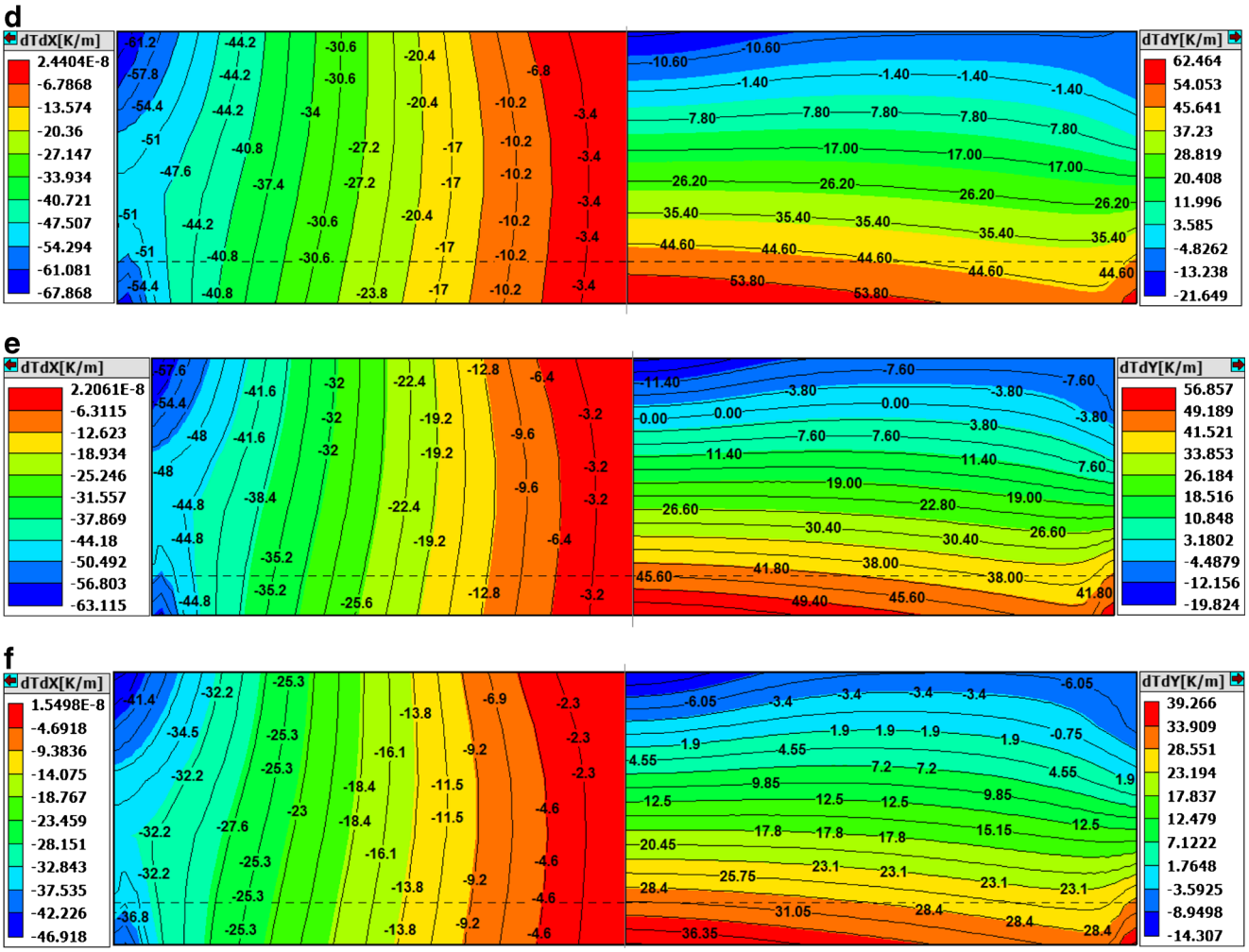



**Fig. 5** (continued)

stress is a combination of all stresses. In the case of shear stress, maximum shear stress has least value at the center region of the mc-Si ingot for 900 K annealing temperature. Maximum shear stress has least value at the peripheral region of the mc-Si ingot for 700 K annealing temperature. The whole mc-Si ingot has lower thermal stress at 700 K annealing temperature compared to other cases. It is shown in Fig. 7.

## 6 Conclusion

Numerical simulation is made for various annealing treatments of the mc-Si ingot for PV applications. The melt-crystal interface in the early stage of growth is nearly planar, after that it is slightly convex. 5 h annealing time

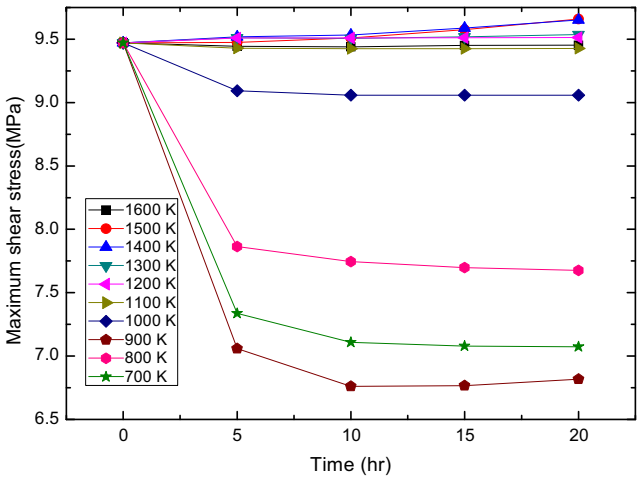



**Fig. 6** Maximum Shear stress at various annealing treatments

is enough to decrease the internal stress of the mc-Si ingot. Increase of the annealing time beyond 5 h does not decrease the stress significantly. Maximum shear stress has least value at the center region of the mc-Si ingot for 900 K annealing temperature. Maximum shear stress has least value at the peripheral region of the mc-Si ingot for 700 K annealing temperature. Thermal stress for the whole ingot is minimum at 700 K annealing temperature

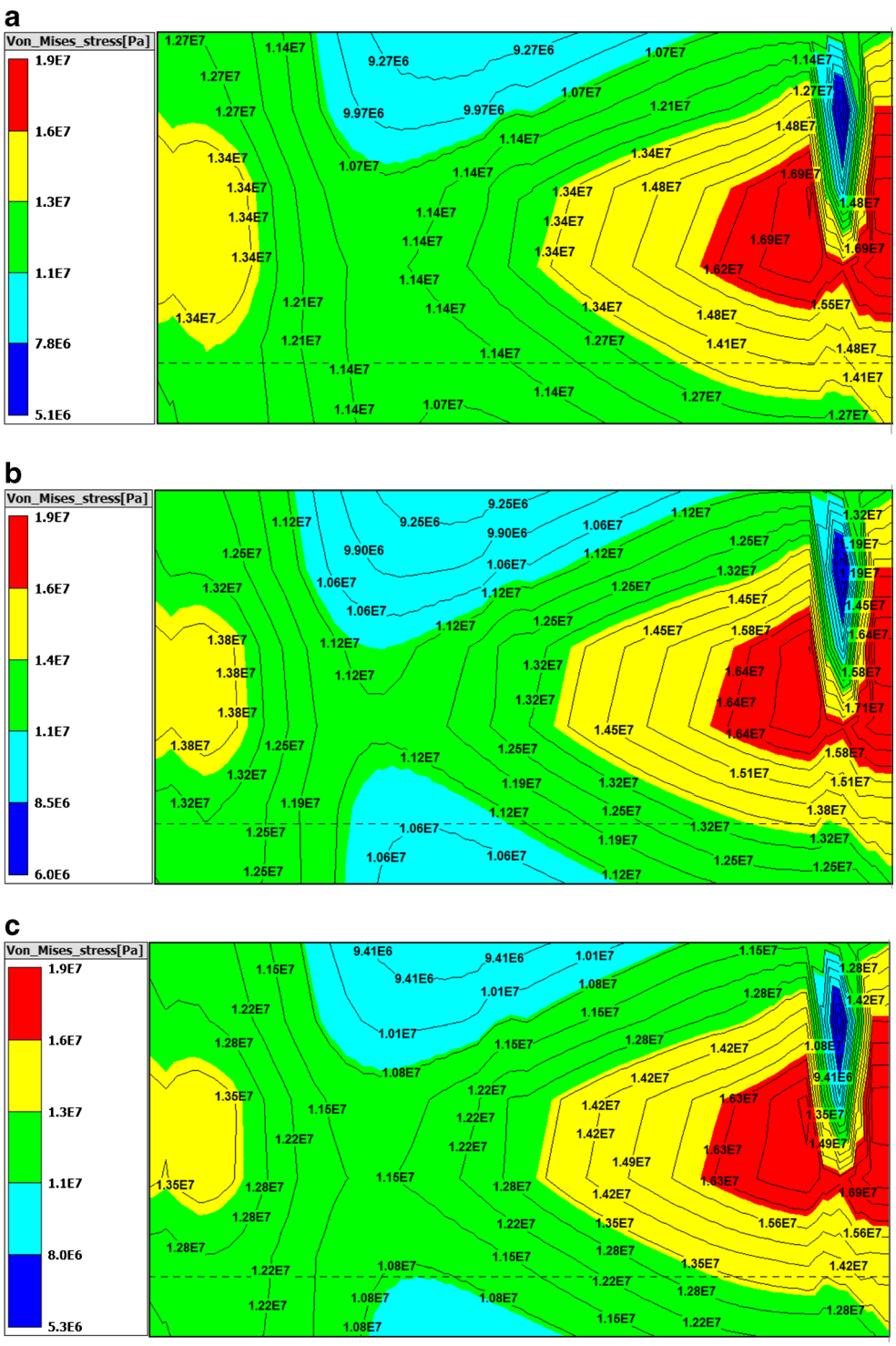
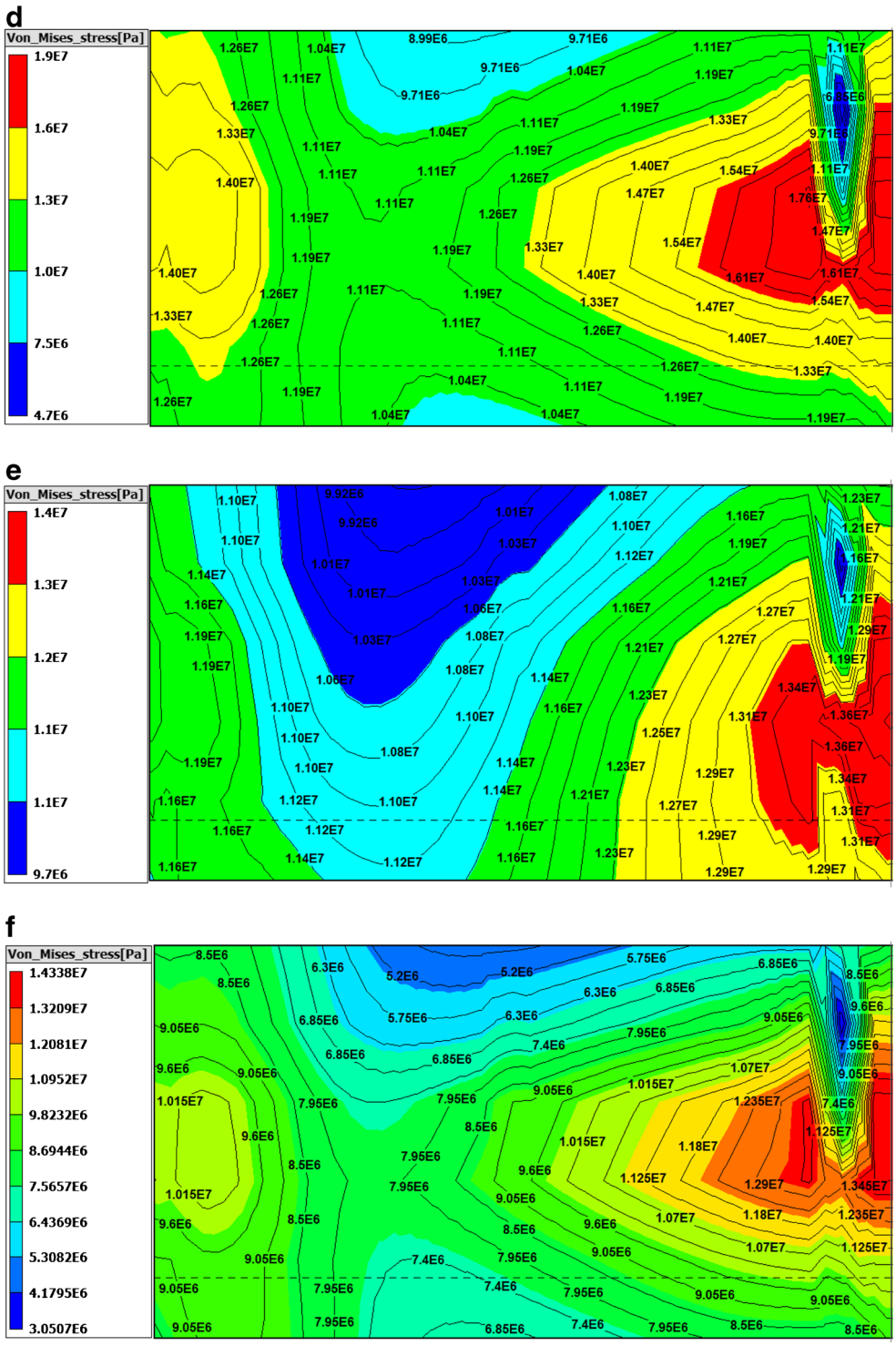



**Fig. 7** Maximum thermal stress on mc-Si ingot for various annealing temperature for 5 h **a** (without annealing), **b** (1500 K), **c** (1300 K), **d** (1100), **e** (900 K) and **f** (700 K)

**Fig. 7** (continued)




compared to other cases, because of lower axial and radial temperature gradients. At the higher annealing temperature (above 1000 K) stress does not reduce significantly. This investigation will be helpful for the industrial DS process to grow better quality mc-Si ingots for PV application.

**Acknowledgements** This work was supported by the Ministry of New and Renewable Energy (MNRE), the Government of India (Order no: 31/58/2013-2014/PVSE & 15-01-2015).

## References


1. Wu Z, Zhong G, Zhang Z, Zhou X, Wang Z, Huang X (2015) Optimization of the high-performance multi-crystalline silicon solidification process by insulation partition design using transient global simulations. J Cryst Growth 426:110–116
2. Lan CW, Yang YM, Yu A, Wu YC, Hsu B, Hsu WC, Yang A (2015) Recent progress of crystal growth technology for multi-crystalline silicon solar ingot. Solid State Phenom 242:21–29
3. Anandha Babu G, Isao T, Satoru M, Noritaka U (2016) Improved multicrystalline silicon ingot quality using single layer silicon beads coated with silicon nitride as seed layer. J Cryst Growth 441:124–130
4. Yeh KM, Hseih CK, Hsu WC, Lan CW (2010) High-quality multi-crystalline silicon growth for solar cells by grain-controlled directional solidification. Prog Photovolt Res Appl 18:265–271
5. Chen XJ, Nakano S, Liu LJ, Kakimoto K (2008) Study on thermal stress in a silicon ingot during a unidirectional solidification process. J Cryst Growth 310:4330–4335
6. Xi Y, Lv G, Ma W, Xue H, Chen D (2016) The effect of radiative heat transfer characteristics on vacuum directional solidification process of multicrystalline silicon in the vertical Bridgman system. Appl Therm Eng 93:731–741
7. Gao B, Nakano S, Harada H, Miyamura Y, Sekiguchi T, Kakimoto K (2012) Reduction of polycrystalline grains region near the crucible wall during seeded growth of monocrystalline silicon in a unidirectional solidification furnace. J Cryst Growth 352:47–52
8. Black A, Medina J, Pineiro A, Dieguez E (2012) Optimizing seeded casting of mono-like silicon crystals through numerical simulation. J Cryst Growth 353:12–16
9. Xi Y, Ma W, Lv G, Wei K, Luo T, Chen D (2014) A modified vacuum directional solidification system of multicrystalline silicon based on optimizing for heat transfer. J Cryst Growth 400:7–14
10. Ma W, Zhong G, Sun L, Yu Q, Huang X, Liu L (2012) Influence of an insulation partition on a seeded directional solidification process for quasi-single crystalline silicon ingot for high-efficiency solar cells. Sol Energy Mater Sol Cells 100:231–238
11. Nagarajan SG, Srinivasan M, Aravinth K, Ramasamy P (2016) Simulation analysis on impurity distribution in mc-Si grown by directional solidification for solar cell applications. Int J Mater Res 107:1–9
12. Srinivasan M, Karuppasamy P, Ramasamy P, Barua AK (2016) Numerical modelling on stress and dislocation generation in multi-crystalline silicon during directional solidification for PV applications. Electron Mater Lett 12:431–438
13. Wu J, Li Y, Ma W, Liu K, Wei K, Xie K, Yang B, Dai Y (2014) Impurities removal from metallurgical grade silicon using gas blowing refining techniques. Silicon 6:79–85
14. Wu J, Liu K, Chen X, Ma W, Yang B, Dai Y (2013) Prediction of covalent interactions between Si and B, Fe, Al or Ca in metallurgical grade silicon using ab initio molecular dynamic simulations. Silicon 7:253–259
15. Nguyen THT, Liao S-H, Chen J-C, Chen C-H, Huang Y-H, Yang C-J, Lin H-W, Bich NH (2016) Effects of the hot zone design during the growth of large size multi-crystalline silicon ingots by the seeded directional solidification process. J Cryst Growth 452:27–34
16. Hao Q, Xie X, Wang B, Liu C (2012) Effect of annealing temperature on the properties of silicon crystal. Adv Mater Res 415–417:1323–1326
17. Gou X, Li X, Ying XU, Liang X, Zhao Y (2009) Effect of thermal annealing on characteristics of polycrystalline silicon used for solar cells. Mater Res Soc Symp Proc 1123:P03–06
18. Lan CW, Yang CF, Lan A, Yang M, Yu A, Hsu HP, Hsu B, Hsu C (2016) Engineering silicon crystals for photovoltaics. CrystEngComm 18:1474–1485
19. Fang HS, Wanga S, Zhou L, Zhou N. G, Lin MH (2012) Influence of furnace design on the thermal stress during directional solidification of multicrystalline silicon. J Cryst Growth 346:5–11
20. Nakano S, Chen XJ, Gao B, Kakimoto K (2011) Numerical analysis of cooling rate dependence on dislocation density in multicrystalline silicon for solar cells. J Cryst Growth 318:280–282
21. Ding C, Huang M, Zhong G, Ming L, Huang X (2014) A design of crucible susceptor for the seeds preservation during a seeded directional solidification process. J Cryst Growth 387:73–80
22. Ding C, Huang M, Zhong G, Liu L, Huang X (2014) Movable partition designed for the seed-assisted silicon ingot casting in directional solidification process. Cryst Res Technol 49:405–413
23. Teng Y-Y, Chen J-C, Huang B-S, Chang C-H (2014) Numerical simulation of impurity transport under the effect of a gas flow guidance device during the growth of multicrystalline silicon ingots by the directional solidification process. J Cryst Growth 385:1–8
24. Liu L, Yu Q, Qi X, Zhao W, Zhong G (2015) Controlling solidification front shape and thermal stress in growing quasi-single- crystal silicon ingots: process design for seeded directional solidification. Appl Therm Eng 91:225–233
25. Lv G, Chen D, Yang X, Ma W, Luo T, Wei K, Zhou Y (2015) Numerical simulation and experimental verification of vacuum directional solidification process for multicrystalline silicon. Vacuum 116:96–103
26. Takahashi I, Usami N, Kutsukake K, Stokkan G, Morishita K, Nakajima K (2010) Generation mechanism of dislocations during directional solidification of multicrystalline silicon using artificially designed seed. J Cryst Growth 312:897–901