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ORIGINAL PAPER

Effect of Secondary Annealing on the Electrical Properties of Polysilicon Thin Films

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Abstract In this work, we study the electrical characteristics of polysilicon (resistivity, free carrier concentration and Hall mobility of carriers), depending on the annealing temperature of implantation for films of polycrystalline silicon having undergone a long heat treatment after implantation, and also the secondary annealing temperature (900-1100 °C) of longer periods. The results have shown that the longer periods of secondary annealing have permitted the improvement of electrical characteristics of our films (decrease of the resistivity, increase of the free carriers concentration and the carriers Hall mobility).

Keywords Polycrystalline silicon · Thin films · Annealing · Electrical properties

1 Introduction

The direct conversion of solar energy into electrical energy through solar cells remains an ongoing concern of researchers [1, 2], in order to reduce their cost. The use of polycrystalline silicon can achieve this goal. However, the photovoltaic efficiency of solar cells made of this type of material is limited by the presence of grain boundaries (GBs) [3–5], which include dangling bonds, which represent states traps for minority carriers. The latter defects, running as important recombination centers, are a serious limitation in photovoltaic cell performances. Several techniques were used to eliminate undesired impurities and realize the GBs passivation in order to improve the electrical properties [6]. This can be done by heat treatments [7], ion implantation [7–9] and hydrogenation [10–12].

In this paper, we present an experimental approach to limit the extended GB by heat treatment in order to reduce the defects and to allow the ions to be positioned in electrically active centers [13].

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2 Experimental

Polycrystalline silicon thin films were deposited by standard low pressure chemical vapor deposition LPCVD at 620 °C by SiH_4 decomposition [14]. In our experiments we used 0, 7 μ m thickness samples, deposited on a mono-crystalline silicon substrate of orientation <111>and resistivity 6 to 12 Ω .cm, with a thin layer (0.116 μ m) of silicon dioxide which was used to isolate the films from the substrate. The films were doped by boron ion implantation (various doses were undertaken, 10^{15} cm^{-2}, 2.10^{15} cm^{-2}; implantation was effected by gaseous BF_3). These films undergo firstly for 120 min a high temperature treatment 1150 °C before implantation and for 30 min a thermal annealing (1050 ° C - 1200 °C) after implantation and for secondary annealing temperature (900 °C - 1100 °C) for 27, 9, 3 and 0.5 hours, respectively. Measurements of the Hall effect and the resistivity were carried out on these films.

3 Results and Discussion

Figures 1, 2 and 3 shows that the electrical characteristics remain unchanged for annealed films after implantation in the range of temperatures (1050 °C - 1200 °C), and they vary only for temperatures above, this indicates that the

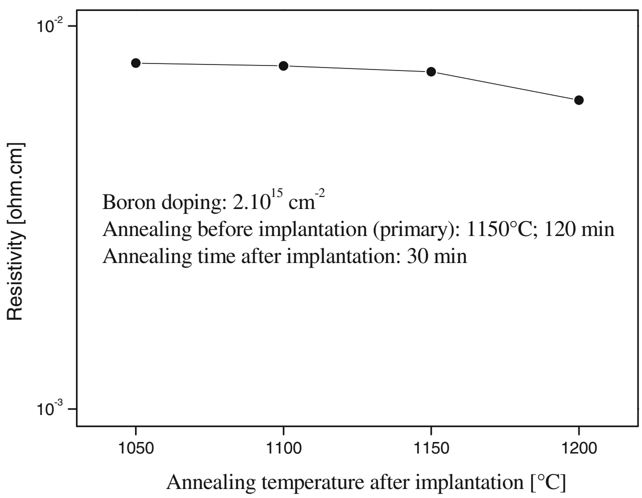

Fig. 1 Resistivity as a function of annealing temperature after implantation

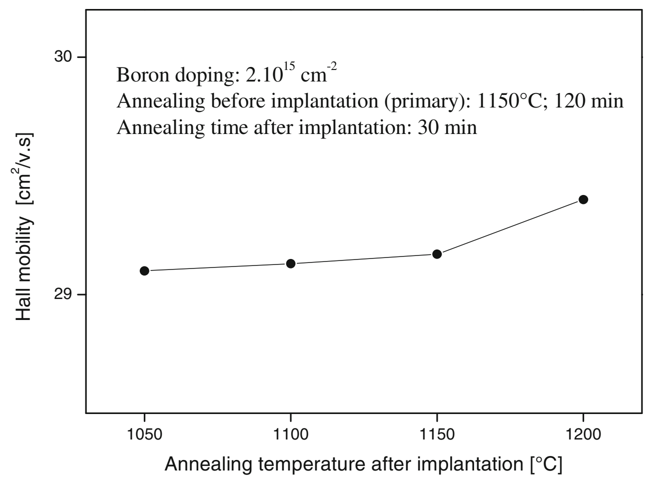

Fig. 3 Hall mobility as a function of annealing temperature after implantation

average grain size remains constant for annealing temperatures lower than that of heat treatment after implantation, and increases for higher temperatures. These variations are explained by the fact that the rise in temperature increases the resistivity of the neutral regions [15] and excites free carriers that pass more easily over the potential barrier, which reduces the resistivity of regions of barriers. This is due to the reduction of trap density of states and sites of segregation by the rearrangement of the network of joints and grain growth, resulting in an increase in the concentration of free carriers and the decrease in the height of barriers potential.

In this study, we chose boron as a doping element because of its low tendency to segregation at the grain boundaries, and we took care to slowly heat samples (in the annealed condition after implantation), to allow the atoms doped that spread within the grain, to take their place back at the grain boundaries.

The fast increase in the carriers mobility for the low doping levels is explained by the strong reduction of potential barriers height of deserted zones. Indeed, in this range of doping, in spite of the increase of the concentration of the ionized atoms, the reduction of the potential barriers height of deserted zones favors the increase of the carriers mobility. When doping is increased, the potential barriers height of deserted zones decreases less quickly, whereas the concentration of the ionized atoms becomes more and

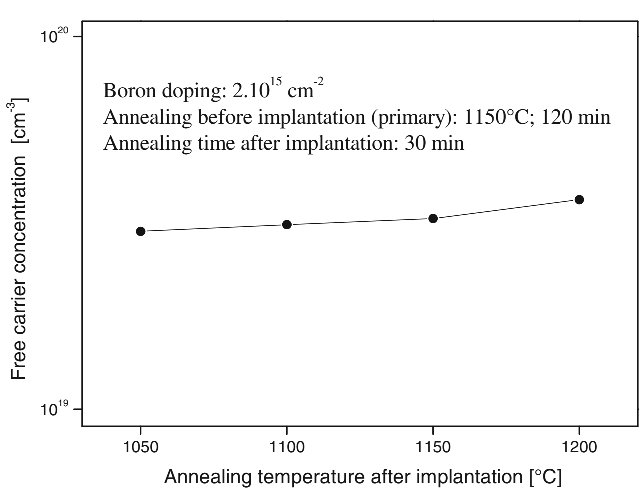

Fig. 2 Free carrier concentration as a function of annealing temperature after implantation

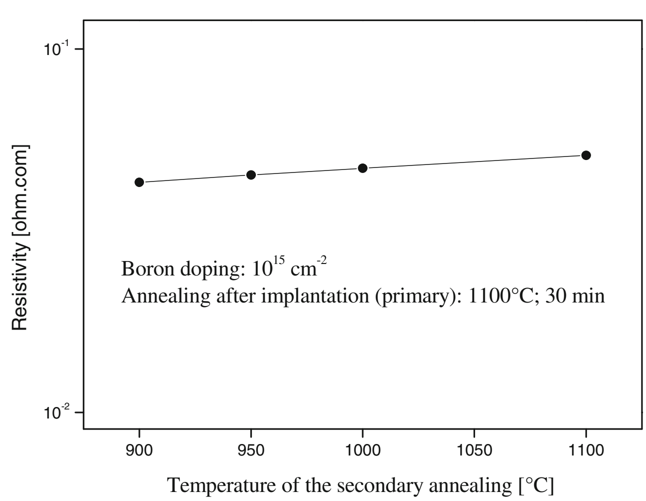

Fig. 4 Resistivity as a function of secondary annealing temperature

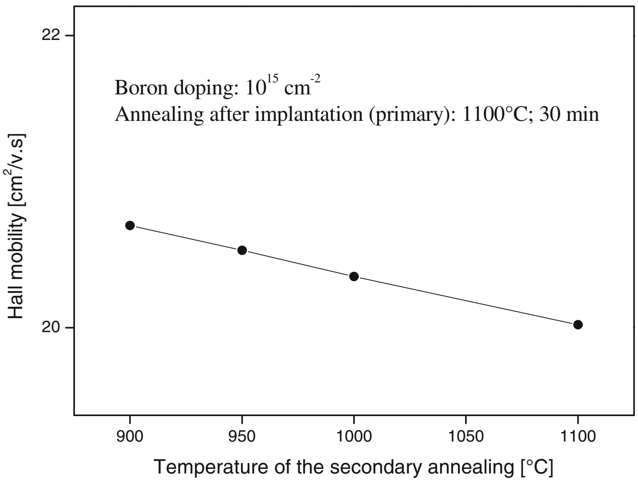

Fig. 5 Hall mobility as a function of secondary annealing temperature

more important. Thus, the mobility tends towards a maximal value then decreases as a result of the free carrier's dispersion by the ionized atoms.

The doping atoms concentration in the boundaries reduces when the temperature of the heat treatments after implantation increases. The heat treatments reduce the number of segregation sites at the grains boundaries, and consequently, they limit the quantity of the doping atoms that may accumulate in these boundaries.

Figures 4, 5 and 6 show a slight variation of the electrical characteristics (decrease of the resistivity, increase of the free carriers concentration and the carriers Hall mobility) when the temperature of secondary annealing decreases for increasingly longer times. These variations indicate that there is a slight grain growth when the temperature of secondary annealing decreases. We did not observe any tendency of the boron segregation; this is due to slight grain growth that would have masked the low segregation of boron atoms at the grain boundaries.

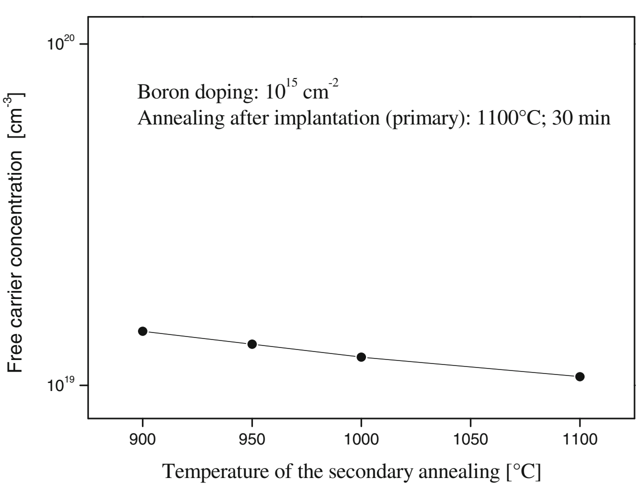

Fig. 6 Free carrier concentration as a function of secondary annealing temperature

This growth of the grains is explained by the increase of the coefficient of silicon self-diffusion in the grains boundaries. For the samples having undergone a long thermal treatment before implantation (1150 °C; 120 min.), the average grains size remained constant for lower annealing temperatures after implantation, but it increases for higher temperatures or for longer times.

4 Conclusion

We have investigated the influence of heat treatments on the electrical properties of polycrystalline silicon films prepared by LPCVD. The heat treatments before and/or after implantation reduce the number of trapped carriers and the amount of doping atoms at the grain boundaries. In addition, they decrease the resistivity. The secondary annealing temperatures improve the electrical properties (resistivity, free carriers concentration and the Hall mobility) of these samples.

References

1. Petinot F, Plais F, Mencaraglia D, Legagneux P, Reita C, Huet O, Pribat D (1998) J of Non-Cryst Solids 227–230:1207–1212
2. Mandal G, Ganguly T (2011) Indian J Phys 85:1229–1245
3. Trabelsi A, Zouari A (2014) Sol Energy 107:220–226
4. Seto JYW (1975) J Appl Phys 46:5247–5254
5. Baccarani G, Ricco B, Spandini GJ (1978) J Appl Phys 49: 5565–5570
6. Zaidi B, Hadjoudja B, Felfli H, Chibani A (2011) Turk J Phys 35:185–188
7. Zaidi B, Hadjoudja B, Felfli H, Chouial B, Chibani A (2011) Rev Métal 108:443–446
8. Ai B, Shen H, Liang Z, Chen Z, Kong G, Liao X (2006) Thin Solid Films 497:157–162
9. Funde AM, Bakr NA, Kamble DK, Hawaldar RR, Amalnerkar DP, Jadkar SR (2008) Sol Energy Mater Sol Cells 92:1217–1223
10. Amor SB, Bousbih R, Ouertani R, Dimassi W, Ezzaouia H (2014) Sol Energy 103:12–18
11. Slaoui A, Pihan E, Ka I, Mbow NA, Roques S, Koebel JM (2006) Sol Energy Mater Sol Cells 90:2087–2098
12. Zaidi B, Hadjoudja B, Chouial B, Gagui S, Felfli H, Chibani A (2014) Silicon. doi:10.1007/s12633-014-9186-2
13. Hadjoudja B, Chibani A, Zeggari R, Chouial B (2003) Phys Chem News 13:85–90
14. Qin Y., Feng T, Li Z, Sun Z (2011) Appl Surf Sci 257:7993–7996
15. Li SS, Thurber WR (1978) Solid-State Elec 21:1109–1117