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RESEARCH ARTICLE

Newly designed modified trinary-valued logic gates using SLM-based Savart plate

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Abstract Multivalued optical logic shows immense promise in modern computing systems with several advantages like ultrahigh computational speed, large amount of data handling capability and high data density. The logic gates are building blocks of computational systems, and all the logic circuits can be realized by cascading different logic gates. This paper proposes a new set of designs for existing logic gates in the Modified Trinary Number system with more efficiency and less complexity. The newly designed gates enable direct cascading of multiple gates and require lesser number of SLMs and Savart plates for realization, hence greatly reducing the circuit complexity of larger circuits. The Optical Tree Architecture of these new logic gates is realized using Spatial Light Modulators (SLM) and Savart plates. Moreover, a comparative study between the newly designed gates and existing gates is also incorporated to demonstrate the reduction in SLMs and Savart plates in the newly developed designs.

Keywords Di-bit · MVL · MTN · OTA · SLM

Introduction

Unlike traditional binary logic system [1], Multivalued Logic (MVL) consists of more than two logical states [2]. The presence of these extra states results in a plethora of advantages over binary logic [3]. These MVL systems can be implemented optically by manipulating polarization of light beam [4]. This optical implementation enables much faster computing speeds, greater energy efficiency and greater information storage. The most notable of these

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optically implemented MVL systems is Trinary- [5–11] and Quadruple-valued logic systems [12–17]. The presence of signed bit in Trinary logic system enables the carry-and-borrow free calculus called Modified Trinary Number (MTN) system [18]. There are different ways to optically implement these logical systems such as using Mach–Zehnder interferometers (MZI) [19], SLM and Savart plates [5, 12].

True, False and Contradiction are three states of the Trinary logic system. These states are represented in di-bit format. The di-bit of 00 or no-light state is considered as redundant, as shown in Table 1. The pre-existing SLM-based Trinary logic gates functioned perfectly but had some drawbacks, such as the state of 0 or 'contradiction' is achieved when both the electrical inputs are provided as 0 to the SLMs of basic building block. The output beam in contradiction state contains both the vertical and horizontal polarization states of light. This is a huge matter of concern for cascading of multiple logic gates as the contradiction state, when converted to electrical signals using optoelectronic converters, generates two electrical bits of 1 and 1. If these bits are provided as input of next block, it will not be able to generate the required state of contradiction. So, an interfacing circuit is required for cascading of multiple logic gates. This drastically increases the circuit complexity. In this paper, a new set of gate designs is introduced without changing the original Trinary logic system. These new designs for the logic gates solve the aforementioned problem as the 0 state is achieved with the electrical inputs of 1 and 1 to the SLMs of a basic building block.

Also, some new propositions are implemented while designing the gates to reduce the required number of Savart plates and SLMs. All these logic gates perfectly realize the same operations, as shown in Table 2.

The Trinary-valued logic system

Trinary-valued logic system is made of three states called True, False and Contradiction. The presence of only vertical polarization of light corresponds to true state and only horizontal polarization at the output corresponds to false state. Finally, the presence of both vertical and horizontal polarization of light at the output beam corresponds to contradiction state. No light at the output is considered redundant. These outputs are also represented as 1, $\bar{1}$, 0 and Di-bit of 01, 10 and 11, as shown in Table 1.

Different unary and binary logical operations are possible in Trinary logic systems, as shown in Table 2.

Table 1 Trinary logic system

Logical state	Representation	Di-bit	Polarization
True	1	01	Vertical
False	$\bar{1}$	10	Horizontal
Contradiction	0	11	Both
Don't care state		00	–

Table 2 Truth table of basic Trinary logic gates

A B	: 1 1 1 0 0 0 $\bar{1}$ $\bar{1}$ $\bar{1}$: 1 0 $\bar{1}$ 1 0 $\bar{1}$ 1 0 $\bar{1}$	Operation
$A \vee B$	: 1 1 0 1 0 $\bar{1}$ 0 $\bar{1}$ $\bar{1}$	A OR B
$A \wedge B$	: 1 0 0 0 0 0 0 0 $\bar{1}$	A AND B
$A \oplus B$	: 0 1 0 1 0 $\bar{1}$ 0 $\bar{1}$ 0	A XOR B
$\overline{A \vee B}$	: $\bar{1}$ $\bar{1}$ 0 $\bar{1}$ 0 1 0 1 1	A NOR B
$\overline{A \wedge B}$	: $\bar{1}$ 0 0 0 0 0 0 0 1	A NAND B
$\overline{A \oplus B}$	: 0 $\bar{1}$ 0 $\bar{1}$ 0 1 0 1 0	A XNOR B
$\bar{A}$	: $\bar{1}$ $\bar{1}$ $\bar{1}$ 0 0 0 1 1 1	Complement
$A\uparrow$	: 1 1 1 1 1 1 0 0 0	True Selector
$A\downarrow$	: 0 0 0 $\bar{1}$ $\bar{1}$ $\bar{1}$ $\bar{1}$ $\bar{1}$ $\bar{1}$	False Selector
$A\spadesuit$	: 1 1 1 0 0 0 0 0 0	Exclusive True Selector
$A\clubsuit$	: 0 0 0 0 0 0 $\bar{1}$ $\bar{1}$ $\bar{1}$	Exclusive False Selector

New designs for Trinary logic gates

The new set of designs for Trinary logic gates provides many advantages such as seamless cascading of multiple gates hence enabling the practical implementation of different combinational and sequential circuits. The number of SLMs and Savart plates needed is also reduced in some gates. Positive SLMs are used for the new designs instead of negative SLMs. To implement the basic building block of the newly designed logic gates in Ternary Logic System, positive Spatial Light Modulators (SLMs) have been used. The implementation is shown in Fig. 1. In the first stage, light from the laser source L gets incident on the polarizer P. After polarization at an angle of 45°, it is split into two orthogonal components by the Savart plate S_1. The two components—vertical and horizontal, emerge from the Savart plate S_1 having a spatial shift between them. The positive SLMs P_1 and P_2 are then used against the two supplied inputs. The operation of a positive SLM is just opposite to a negative SLM, i.e., it allows the light to pass when a true electrical signal is provided on it. The input here is appraised in the form of di-bit electrical equivalents.

The two polarized beams are then reunited by the second Savart plate S_2 for fur. Various combinations of the basic building block form the Optical Tree Architecture (OTA) of different logic gates.

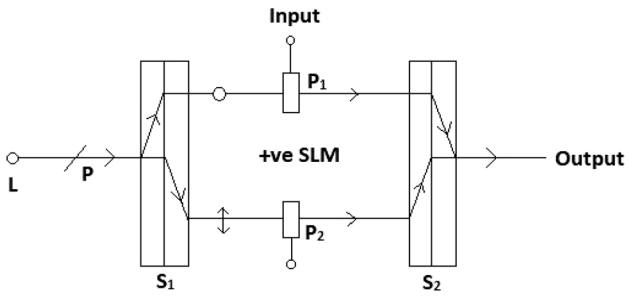


Fig. 1 Basic building block

AND gate

Figure 2 shows the delineation of the AND gate which is formed by connecting two basic building blocks in parallel. After being polarized by the polarizer P, the beam emerging from the laser source L is split into two parts by the beam splitter BS_1. The first part is passed through a basic building block where input A is provided as electrical di-bit equivalents to the positive SLMs P_1 and P_2. The other part is reflected by mirror M_1 and drifted through the other basic building block where input B, as electrical di-bit equivalents, is provided to the positive SLMs P_3 and P_4. The beam combiner BS_2 combines the two output lines to generate the ultimate output.

For instance, if the given inputs are A = 1 (A_1 = 0 and A_2 = 1) and B = 1 (B_1 = 0 and B_2 = 1), the horizontal component split by the Savart plate S_1 will be obstructed by the SLM P_1, but the vertical component will pass through P_2. So, only vertical polarization state will be obtained at the output. In the case of the second basic building block, a similar case occurs as the SLM P_4 blocks the horizontal component trying to pass through it. Ultimately, at the final output, the only vertical polarization state is obtained which, according to Table 1, is equivalent to 1.

The circuit shown in Fig. 2 is similarly valid for the other input combinations as per the Truth table shown in Table 2.

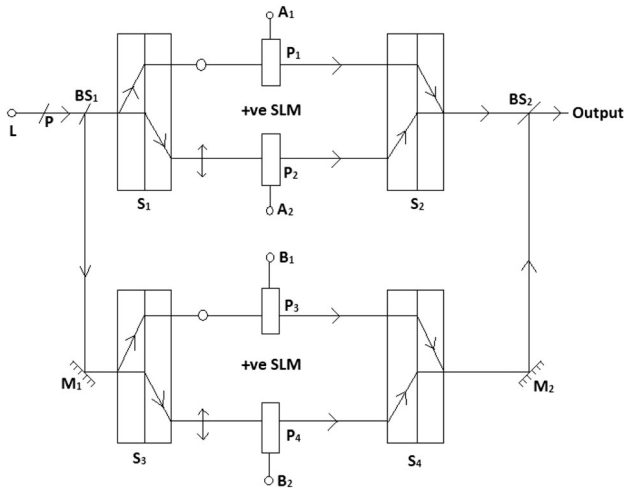


Fig. 2 AND gate

NOT gate

Figure 3 shows the illustration of the NOT gate. Here, negative SLMs have been used in the basic building block. The output of this gate is just the implementation of the input provided. As shown, after getting incident on the beam splitter BS_1, the light coming from the laser source L splits into two parts. One part is progressed through a basic building block where input A is provided as electrical di-bit equivalents to the negative SLMs P_1 and P_2. The other part gets reflected by the mirrors M_1 and M_2 and is passed through another negative SLM P_3.

Now, the output of the basic building block is again split by beam splitter BS_2. One part is passed through an Optical-to-Electrical converter which produces the electrical equivalent signal of the optical signal. The obtained signal is then applied to the negative SLM P_3 which becomes opaque or transparent according to the value of the applied signal. The Optical-to-Electrical converter along with the negative SLM P_3 is used as a compensation circuit. Finally, the beam combiner BS_3 combines the output lines to generate the full and final output.

For example, if an input of A = 1(A_1 = 0 and A_2 = 1) is provided to the SLMs P_1 and P_2, P_1 will allow the horizontal component to pass, while P_2 will block the vertical one. As a result, only the horizontal component is obtained at the output of the basic building block which is equivalent to $\bar{1}$.

OR gate

The design for the OR gate is shown in Fig. 4. Two basic building blocks are connected in series to form the OR gate. As shown, light from the laser source L is first passed through a polarizer P and then gets incident on a beam

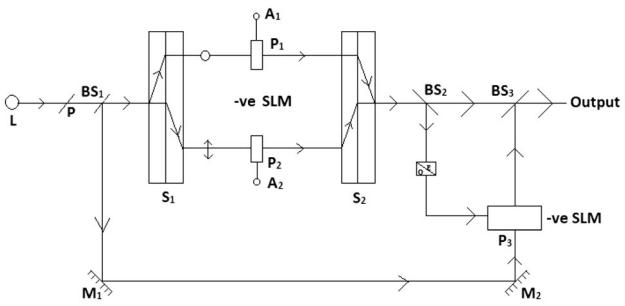
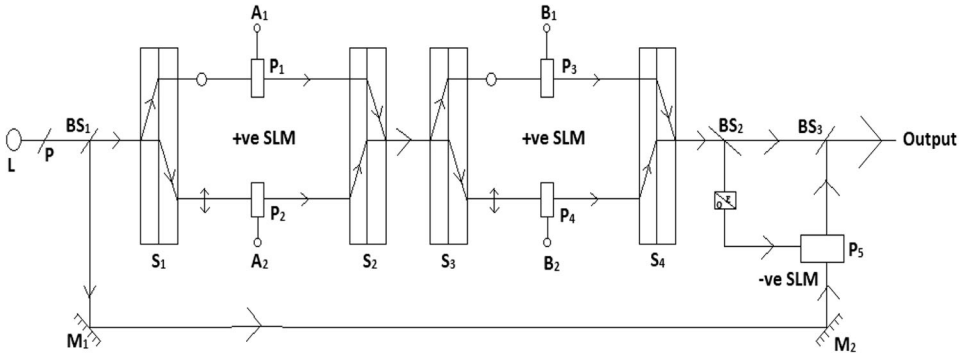


Fig. 3 NOT gate

Fig. 4 OR gate



splitter BS_1. BS_1 bifurcates the beam. One part gets incident on a basic building block where the positive SLMs P_1 and P_2 are provided with an input A in the form of electrical di-bit equivalents. After getting combined by the Savart plate S_2, the output of this basic building block gets incident on another basic building block where an input B, in the form of electrical di-bit equivalents, is supplied to the positive SLMs P_3 and P_4. Mirrors M_1 and M_2 help to reflect the other part of the original beam.

After getting split by the beam splitter BS_2, one of the output lines of the second basic building block is passed through a compensation circuit containing an Optical-to-Electrical converter and a negative SLM as mentioned before. The beam combiner BS_3 helps to produce the final output.

For instance, $A = 0(A_1 = 1$ and $A_2 = 1)$ and $B = 1(B_1 = 0$ and $B_2 = 1)$ are given as inputs to the positive SLMs P_1, P_2, P_3 and P_4, respectively. Now, SLMs P_1 and P_2 will allow their corresponding beams to go through them and both the horizontal and vertical components will be obtained at the output of the first basic building block. In the case of the second block, the vertical component corresponding to SLM P_4 will pass, while the horizontal component will be blocked by P_3. So, at the final output, the only vertical polarization state is achieved which is equivalent to 1.

The delineation also works for other input combinations as per the Truth table shown in Table 2.

NAND gate

Figure 5 shows the design for NAND gate. The operation is easily implemented by providing the output of AND gate (shown Fig. 2) as the inputs of a NOT gate (shown in Fig. 3) using optoelectronic converters.

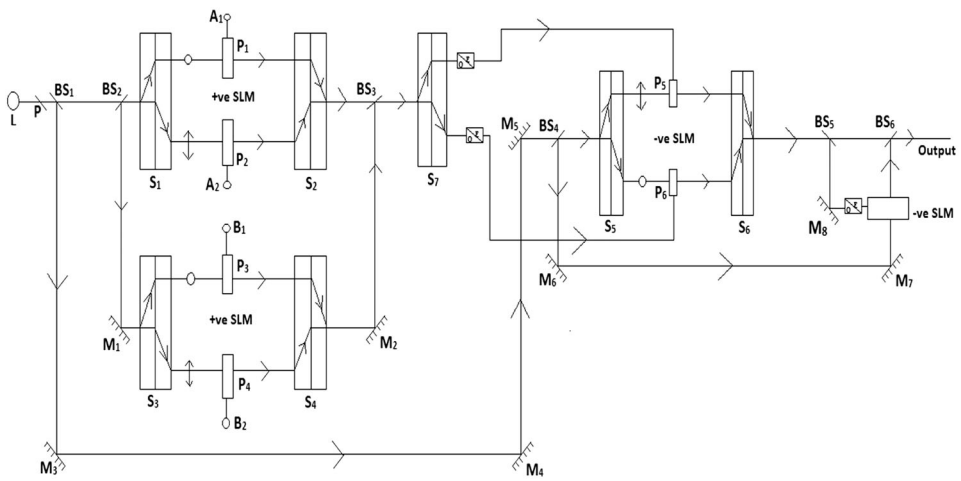
True Selector gate

As shown in Fig. 6, the True Selector operation is achieved by making the second input B of an OR gate (shown in Fig. 4) a default state of 1 or electrical di-bit 01.

False Selector gate

Similar to True Selector, the False Selector operation is implemented by making the B input of an OR gate to a default state of $\bar{1}$. The design for False Selector gate is shown in Fig. 7.

Fig. 5 NAND gate



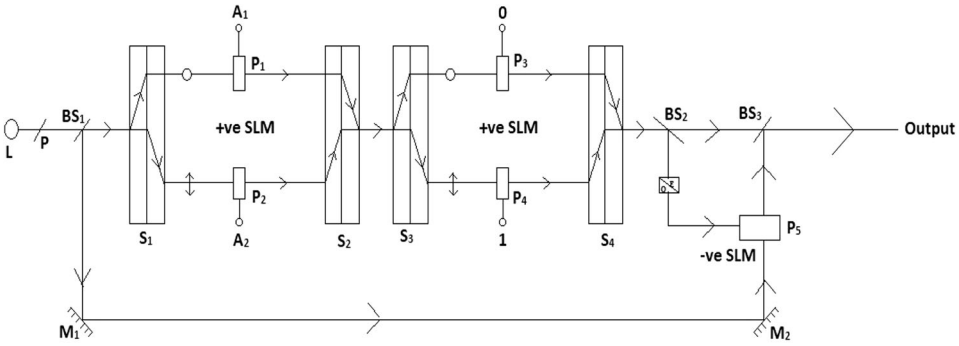


Fig. 6 True selector gate

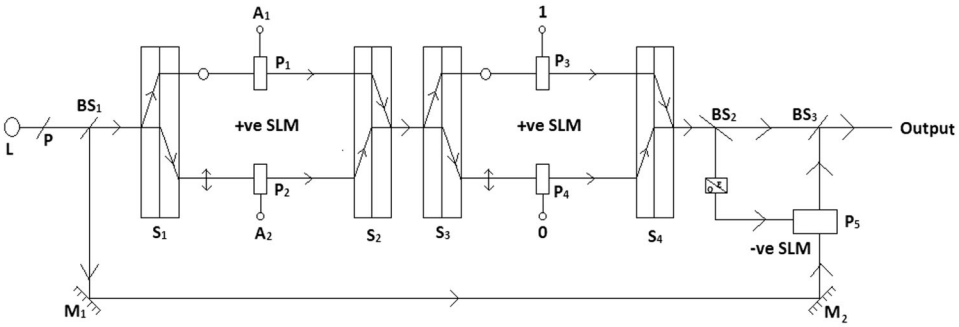


Fig. 7 False selector gate

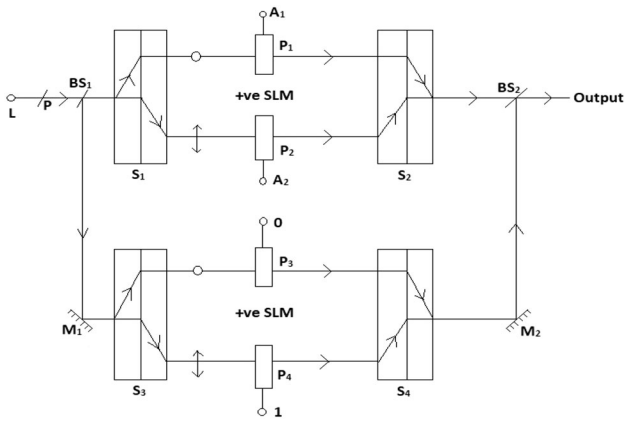


Fig. 8 Exclusive true selector gate

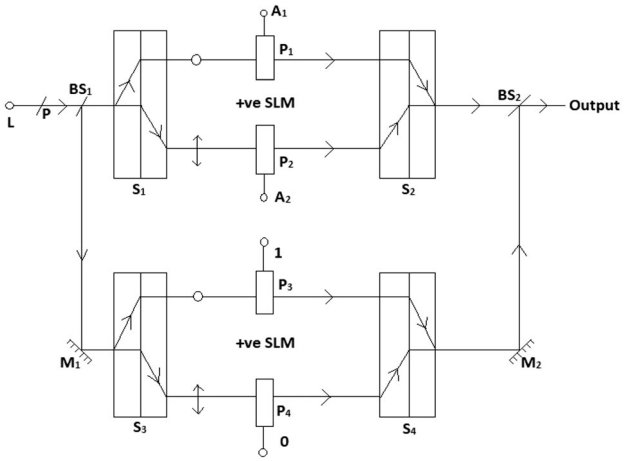


Fig. 9 Exclusive false selector gate

Exclusive True selector gate

As shown in Fig. 8, the Exclusive True selector gate is made of an AND gate (of Fig. 2) with the second input being a constant state of 1 or electrical di-bit 01.

Exclusive False Selector gate

Figure 9 shows the design for Exclusive False selector gate. The operation is realized by making the second input of an AND gate (of Fig. 2) to a default state of $\bar{1}$ or electrical di-bit of 01.

NOR gate

As shown in Fig. 10, the NOR operation is easily achieved by providing the output of an OR gate (of Fig. 4) as inputs of a NOT gate (of Fig. 3) using optoelectronic converters.

Fig. 10 NOR gate

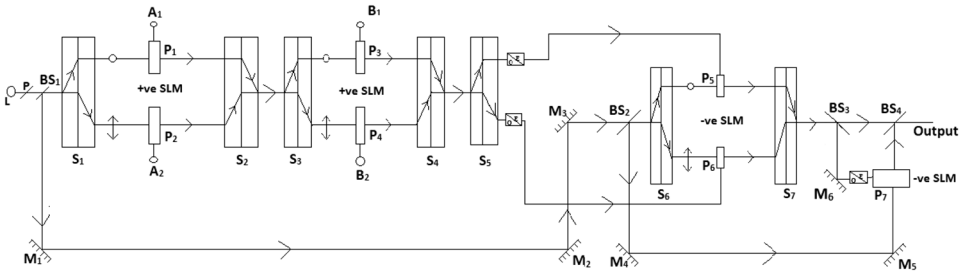


Fig. 11 XOR gate

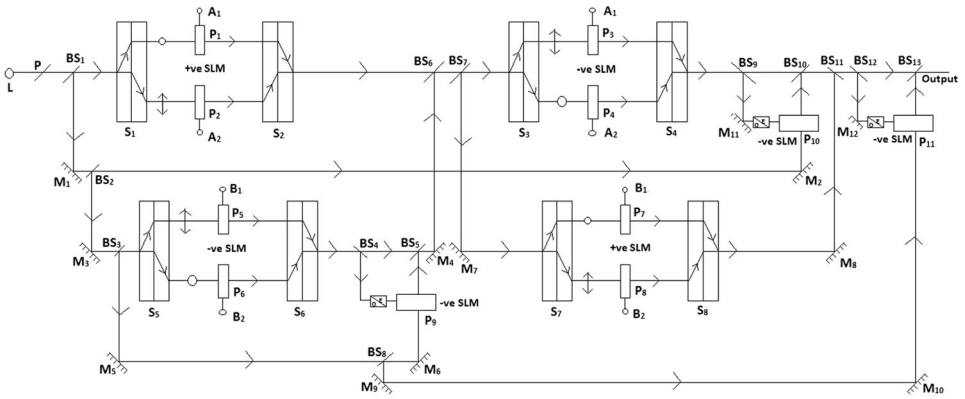
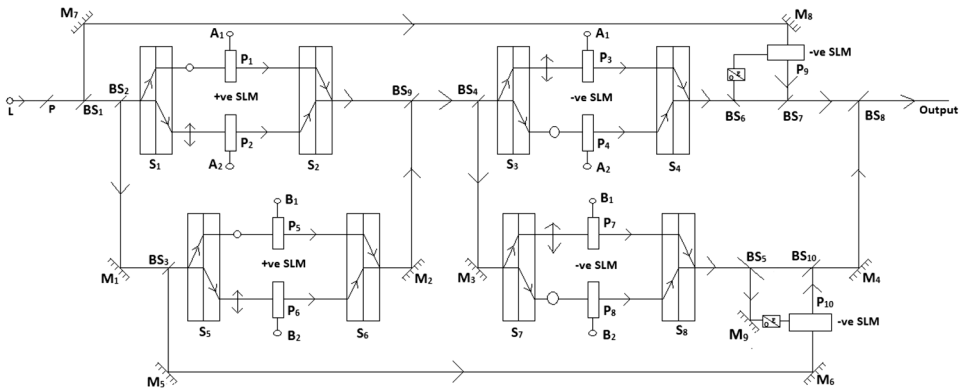


Fig. 12 XNOR gate



XOR gate

Figure 11 shows the diagram of XOR gate. One basic building block and a NOT gate (of Fig. 3) are connected in parallel. The input A is provided at the basic building block and B at NOT gate. The outputs of these blocks are combined using beam combiner BS_6 and split again using BS_7. The two beams after the split are then passed through a NOT gate and a basic building block. The input A is now provided to the NOT gate, and B is provided to the basic building block. Then these two outputs are combined BS_{11} to generate an output. The original beam is reintroduced at the output using a negative SLM to generate the final output; hence, compensation for no-light condition is achieved.

XNOR gate

The OTA (Optical Tree Architecture) of XNOR gate is shown in Fig. 12 The circuit is made by combining an AND gate (shown in Fig. 2) with inputs A and B and two NOT gates (of Fig. 3). The output of the AND gate is then split into two beam by beam splitter BS_{-4}. These two beams are then passed through two NOT gates, and the outputs of the NOT gates are then combined using beam combiner BS_{-8} to generate the final output.

Table 3 Comparative study between existing logic gates and newly designed logic gates

Name of the gate	Existing logic gates		Newly designed logic gates	
	No. of Savart plates required	No. of SLMs required	No. of Savart plates required	No. of SLMs required
OR	4	5	4	5
AND	4	4	4	4
NOR	7	7	7	7
NAND	7	7	7	7
NOT	5	4	2	3
XOR	11	11	8	11
XNOR	14	13	8	10
True selector	4	5	4	5
False selector	4	5	4	5
Exclusive True selector	8	7	4	4
Exclusive False selector	8	7	4	4

Advantages of the newer logic gates

Along with solving the problem in cascading multiple gates, some new techniques are also introduced to reduce the number of SLMs and Savart plates needed to realize the logic gates. This section compares the number of SLMs and Savart plates required to realize each of the gates in existing logic and new logic, as given in Table 3. It can be seen that the newly designed NOT, XOR, XNOR, Exclusive True Selector, Exclusive False Selector gates require lower number of total SLMs and Savart plates for implementation. These new gates can be cascaded directly using simple optoelectronic converters with no interfacing circuit. The ease in cascading and the lower number of SLMs and Savart plate required to realize the logic gates make the new designs worthwhile. All these make the newly designed gates a better solution overall without changing the fundamentals of the Trinary logic or the operations of the logic gate themselves.

Conclusion

In this paper, all the Trinary logic gates are redesigned to enable direct cascading of multiple gates and also to reduce complexity. For faster operation, the newly designed gates are also implemented optically using SLM and Savart plate. The number of SLMs and Savart plate in some gates are also reduced in the newly designed logic gates. By using these newly designed gates, any combinational and sequential circuit of the Trinary logic system can be designed. These gates have huge application in the field of computation and communication in MVL system. Direct cascading of these gates helps to reduce circuit complexity and cost of implementation of massive circuits with high processing speed.

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