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Minimization of Warpage for Wafer Level Package using Response Surface Method

Hye-Jin Lee[1], Sun-Myoung Park[2], and Sung-Jun Park[2,#]

1 Research Institute of Industrial Technology Convergence, Korea Institute of Industrial Technology, 143, Hanggaul-ro, Sangnok-gu, Ansan-si, Gyeonggi-do, 15588, South Korea
2 Department of Mechanical Engineering, Korea National University of Transportation, 50, Daehak-ro, Daesowon-myeon, Chungju-si, Chungcheongbuk-do, 27469, South Korea
Corresponding Author / E-mail: park@ut.ac.kr, TEL: +82-43-841-5130, FAX: +82-43-841-5120

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Warpage issues occurring during semiconductor package process present high probability of loose contacts during assembly processes of chips and package, which has become a critical cause that reduces process yield rates. Therefore, it is necessary to find the right package materials and package structure to minimize such warpage issues. This study performed and investigated the results of a finite-element analysis to find the method to reduce warpage and looked at the effect based on the selection of substrate materials and package structure. Moreover, the study tried to identify factors of, and conditions to minimize, significant effect on warpage by statistically analyzing experimental results based on RSM. According as the substrate and EMC thickness are larger, the warpage is tended to decrease. In addition, the smaller the die-pitch, tends to decrease the warpage. Warpage analysis is performed with respect to the optimal conditions, and it extracts an error of about 0.13 mm as compared with the experimental result. Thus, this analysis result is confirmed that similar to the experimental result.

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1. Introduction

Technological demand for making semiconductor components used in mobile phones, computers, and electronics lighter and smaller while equipping with more features in more complex structures is increasing due to rapid developments in advanced industries such as IT and semiconductors in recent years. Technical developments in the semiconductor industry of high-performance electronics products in line with such trends have been active in all areas of manufacturing processes. It is no exaggeration to say that semiconductor technology developments are focused on securing price competitiveness by reducing production cost whereas achieving high-density and high-speed execution. Especially, marketing products with a competitive edge at the right time helps lead a domination and economic profit creation, which is why competition among major global semiconductor manufacturers has become increasingly fierce.[1-3]

The trend has been making semiconductor package smaller, thinner, and lighter, so that high-density packaging was indispensable to achieve it. These semiconductor packaging trends have moved from surface-mounting technologies such as PGA (Pin Grid Array) and QFP (Quad Flat Package) to area-array technologies such as BGA (Ball Grid Array), CSP and from single-chip packaging in the past to module or system package concept mounting multiple chips on a single package.[4]

Among such package technologies, the WLP (Wafer Level Package) technology is a next-generation technology which has been already used by many manufacturers and researchers. It is a method of dicing after package completion based on integrated processing of connection of chip pad with external connectors using semiconductor rewiring technology and flip chip technology on the wafer level. This technology has the advantage of reducing manufacturing cost by significantly improving assembly processes, and it allows packaging on each wafer before die dicing.[5]

However, packaging large-area wafers at a time may generate problems such as warpage and die shift and dealing with these problems during processes are more difficult than conventional packaging technologies. Furthermore, semiconductor components require continued reduction in both size and thickness due to the development of portable electronic devices that are growing more advanced but smaller. Accordingly, the thickness of semiconductor package components such as silicon-die, EMC, boards, etc. must be reduced to cope with such requirements. That can generate various issues on reliability.[6,7]

Among them, the package warpage problems occur due to differences

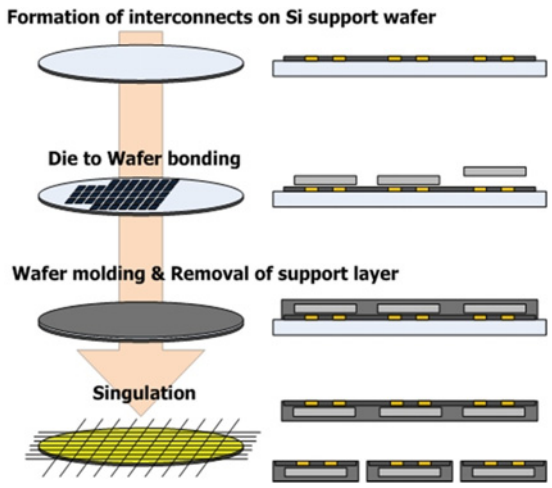

Fig. 1 Wafer level package process[4]

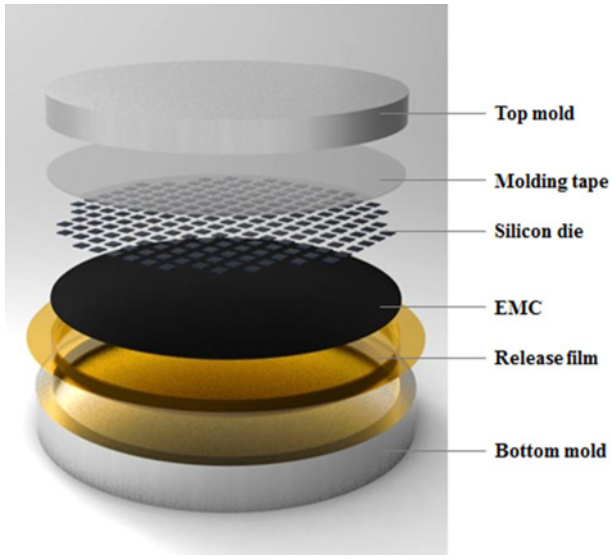

Fig. 2 Schematic configuration of wafer level package

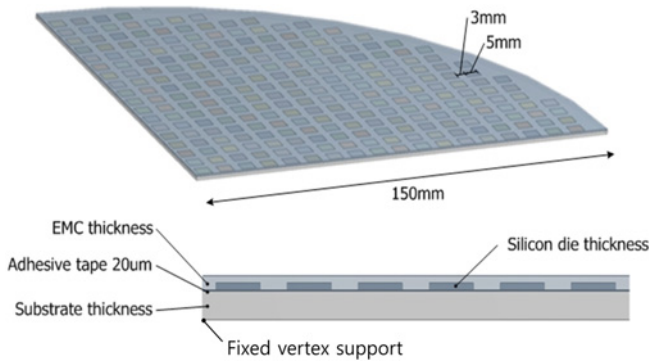

Fig. 3 Schematic configuration of analysis model

in the CTE (Coefficient of Thermal Expansion) of component materials, and generally they occur during curing and cooling processes in molding processes. There is a high probability of loose contacts during assembly processes of chips and package, which has become a critical cause that reduces process yield rates. Therefore, it is necessary to find the right package materials and package structure to minimize such warpage problems. Especially, it is essential to secure reliable design technologies enabling the prediction of bending, stress distribution, etc. as well as reliability problems occurring in package before developing new package.[8-11]

This study aimed to find a method to reduce warpage occurring during WLP processes. A finite-element analysis by selecting EMC thickness, silicon-die thickness, and the materials and thickness of substrates, etc. as the key variable is performed. The effects based on the selection of substrate materials, and package structure are investigated from the results. Moreover, the study tried to identify the significant effect of factors and conditions on minimizing warpage by statistically analyzing experimental results based on variance analysis and RSM.

2. WLP (Wafer Level Package) Process

Fig. 1 shows WLP processes. The first process is the formation of interconnects on the Si support wafer. This is the process of expanding the micro-units of electric interconnects of semiconductor chip element to macro-units to mount on boards during product finalization. Subsequently, Pick and Place and Bonding processes are carried out in which diced semiconductor chips are positioned in a regular sequence on the interconnected support carrier wafer. And then, the whole areas of the wafer are molded using EMC at a time. Each of the elements with dicing after molding process is made into a finalized semiconductor product. The remaining processes are electrical and environmental tests to confirm product reliability.

The molding process, one of the key technologies required in the WLP process, is a process to mold semiconductor chips. This is a highly critical process that acts as a protection to the chips and adds product reliability, as well as the one with the highest defect ratio and difficult to predict among entire semiconductor processes.

For this study, a finite element analysis was carried out to identify the characteristics of warpage. And the most outstanding problem generated during cooling process on the assumption that the entire wafer area is filled with EMC in such a molding process. Fig. 2 shows WLP composition in the molding process.

3. Finite Element Analysis Condition

Fig. 3 shows substrate, silicon-die, EMC, and molding tape for the analysis model of finite element analysis carried out in this study. A quarter(1/4) symmetric model of the package has been used in the FEM analysis to reduce the calculation time without sacrificing simulation accuracy. The elastic-plastic analysis was performed according to thermal load. The thermal condition was set with the initial temperature of 180 C and then cooled to a room temperature of 25°C. Fixed support condition was shown in Fig. 3.

With fixing the silicon-die size of 5×5 mm and adhesive tape thickness of 20 μm, EMC thickness, substrate materials, substrate

Table 1 Geometry parameters of analysis model

Parameter	Variable		
EMC thickness	600 μm	800 μm	1000 μm
Silicon-die thickness	300 μm	400 μm	500 μm
Substrate thickness	0.7 mm	1.2 mm	1.5 mm
Substrate material	Ceramic	Titanium	Sodalime glass

Table 2 Material properties of analysis model

Parameter	Young's modulus (GPa)	Poison's ratio	CTE (ppm/°C)
EMC	19.8	0.3	8 / 30
Silicon-die	112.4	0.28	2.62
Adhesive tape	0.0028	0.4	205
Ceramic substrate	390	0.23	8
Titanium substrate	102.7	0.41	8.64
Sodalime glass substrate	73	0.21	8.5

*Material properties were provided by NEPES Corp. and GCOM Ltd.

thickness, and silicon-die thickness have been treated as optimized variables in the FEM analyses. Table 1 shows the variables used for this analysis. Nine cases of analysis were carried out with EMC thickness and substrate thickness as variables for each substrate material. Therefore, a total of 27 analyses were performed for three substrate materials. Also, additional analyses were carried out with silicon-die thickness as a variable while EMC thickness and substrate thickness are fixed to 600 μm and 1.5 mm respectively. Thus, a total of 30 warpage analyses were made to identify the effect of the variables.

Table 2 shows the parameters of package components applied in this analysis. As mentioned above, warpage is known to be generated due to CTE differences of package component materials. Accordingly, this study selected materials for substrate with similar CTE values to EMC such as ceramic, titanium, sodalime glass, etc. in order to reduce warpage generated due to CTE differences. Furthermore, this study aimed to identify the materials that minimize warpage occurrence among the substrate materials selected through analysis and analyzed its cause.

4. Analysis Result and Discussion

Fig. 4 shows a graph displaying warpage analysis results for substrate materials (ceramic, titanium, and sodalime glass).

Analysis results show the differences in the amount of warpage occurred according to different substrate materials though the occurrences display similar tendencies. First, the results show that warpage occurrences are reduced as substrate thickness is increased. On the contrary, warpage occurrences are increased as EMC thickness is increased. That suggests that the CTE values for selected substrates and EMC are similar but Young's modulus values of EMC are higher than those of EMC. Generally, Young's modulus is a parameter unique to materials displaying the degree of stretch. Materials with higher Young's modulus are less prone to deformation as a result of external forces. Therefore, it is thought that substrates with little deformation as a result of thermal contraction control the deformation of EMC. And the effect is increased or reduced according to the thickness of substrate or EMC.

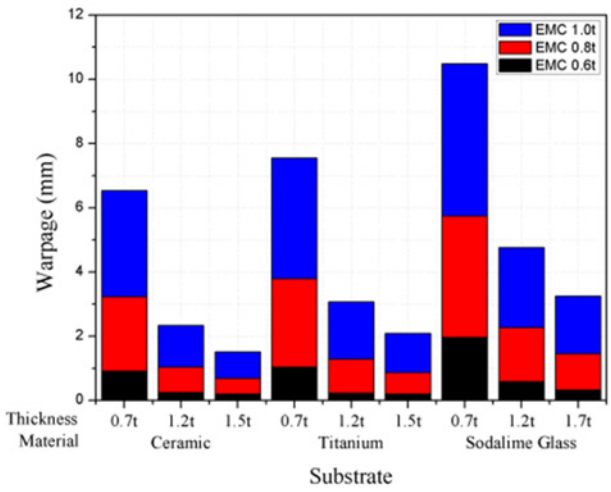

Fig. 4 Warpage result according to substrate material

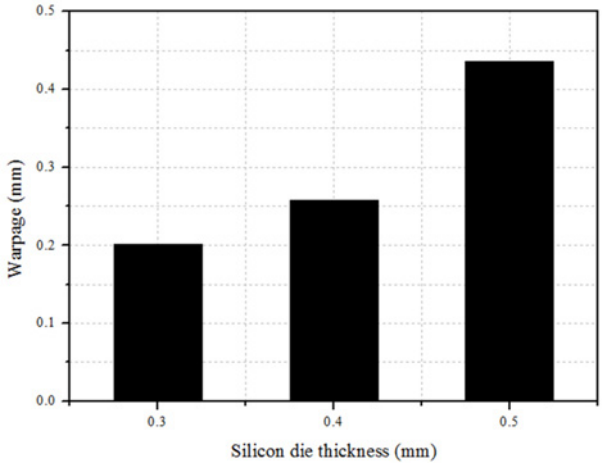

Fig. 5 Warpage results according to silicon-die thickness

It was found that warpage occurrences were lowest for ceramic and highest for sodalime glass. As to the preceding results, the results are thought to occur due to the differences of Young's modulus values for the three substrate material types. It was found that warpage amount was reduced when Young's modulus value is increased.

To conclude, warpage can be minimized when EMC thickness is reduced and substrate thickness is increased in the case EMC and substrate of similar CTE values are selected for package materials in molding processes. Also, the results suggest that selection of substrate materials with higher Young's modulus value can effectively reduce warpage. Therefore, ceramic substrate seems to be the most appropriate material for reducing warpage based upon the analysis results.

Fig. 5 shows warpage according to different silicon-die thickness. The warpage occurrence was minimized at the conditions of 1.5 mm ceramic substrate thickness and 0.6 mm EMC thickness in preceding analysis results. As shown in the figure, warpage increases when silicon-die thickness is increased. The results suggest that warpage is increased when silicon-die thickness with different CTE values is increased while substrates and EMC CTE values are similar.

It is possible to find the methods to reduce warpage using analysis results as shown, but this study aimed to identify the impact of each factor on warpage more accurately using the statistical analysis methods.

5. Analysis of Variance (ANOVA)

Analysis of Variance is a method to identify which factor causes significant changes by analyzing parameter variances of different factors. This study aims to identify the impact on warpage of different factors.

Four different residual plots shown in Fig. 6. It helps to confirm the residual normality and demonstrate the validity of the test design model through existence and distribution pattern within the control limit. First, Normal Probability Plot shows that most data are found on a single line to conform to a normal distribution pattern. Residual Versus Fits Plot illustrates that distribution has constant values as there is no identifiable pattern. Residual Histogram shows a bell-shaped graph conforming to normal distribution pattern and Residual Versus Order Plot shows that the residuals are independent. Furthermore, random tests were carried out, and the graph shows that the data around 0 are randomly distributed without any identifiable pattern.

Fig. 7 shows main effect plot allowing relative identification of warpage impact by tested factors through graph slope. The factor with the largest warpage impact was found from the test result to be substrate thickness. EMC thickness was the next and substrate material was found to be the factor with the least impact on warpage.

Fig. 8 shows the interaction effect plot of warpage, in which the impact of interactions by each factor is illustrated. It is found that the impact of interactions on warpage is not large based on the fact that lines on the interaction effect plot are not intersected but parallel moving into the large.

6. Additional Analysis and Response Surface Method

Preceding analysis results proved that ceramic substrate is the best material to reduce wafer warpage. However, handling damage problems occurred in the ceramic substrate during real-world tests. Accordingly, Titanium substrate with small warpage differences compared to a ceramic substrate in analysis results seems to be superior in terms of productivity and efficiency for application in actual molding equipment. Therefore, additional analyses were carried out to identify the conditions to minimize warpage by analyzing the results of additional analysis based on Titanium substrate with Response Surface Method (RSM).

As Titanium was selected as the substrate material for the analysis, substrate material was removed among the variables shown in Table 1 above and silicon-die pitches of 1 mm, 3 mm, and 5 mm were added instead. Therefore, the analysis was conducted with three variables and three levels of substrate thickness, EMC thickness, and silicon-die pitch for Titanium substrate.

Fig. 10 shows the tendency of warpage occurrence in the additionally performed analysis results. As shown in the figure, the warpage displayed either convex type or concave type according to variables.

Fig. 9 shows the comprehensive analysis results displaying values

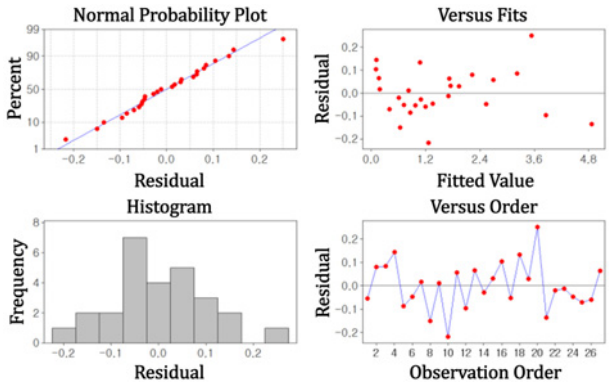

Fig. 6 Residual plot of warpage

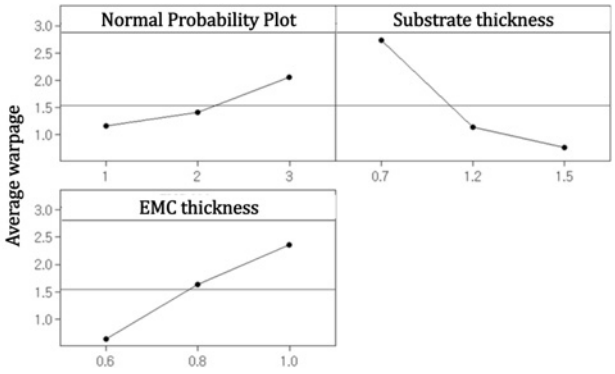

Fig. 7 Main effect plot of warpage

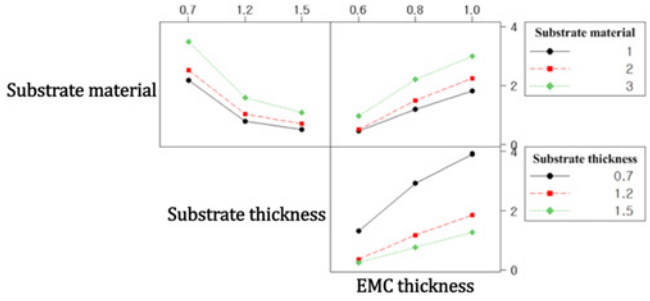

Fig. 8 Interaction effect plot of warpage

below 0 for comparison of Convex type warpage with Concave type. The analysis results show that the effect of EMC thickness varies according to warpage directions though it was the same with the preceding analysis results in which warpage is reduced when the substrate thickness is increased. Thus, the parts which are difficult to be identified with only data were analyzed using RSM statistically.

RSM is an analysis method used to identify the relationship between response variables and experiment variables with the aim of finding the variable condition to optimize response variables. Accordingly, this study derived estimated regression equation for warpage using data of uuencoded units as follows by carrying out response surface analysis to find the optimal variables for target warpage. Here, X, Y, and D denote

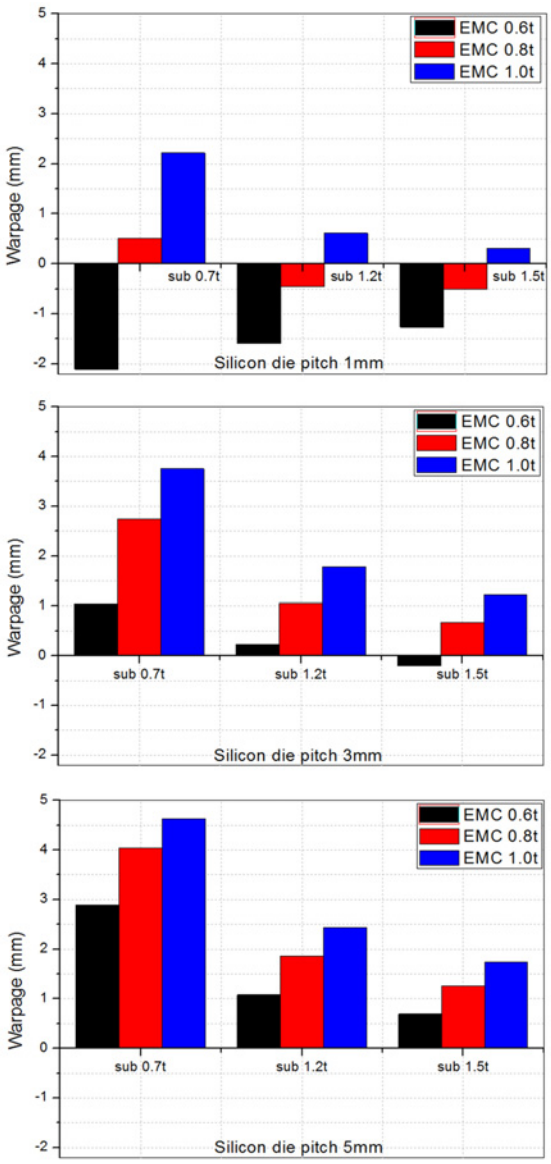

Fig. 9 Warpage results according to silicon-die pitch

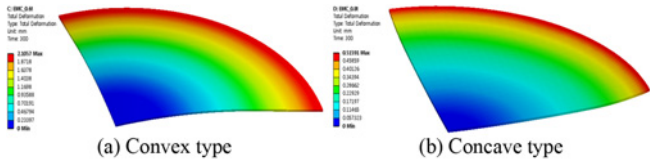

Fig. 10 Warpage type according to direction

substrate thickness, EMC thickness, and silicon-die pitch respectively.

$$\text{Warpage} = 1.1295 - 0.8942*(X) + 0.4458*(Y) + 0.6502*(D) + 0.3287*(X^2) + 0.1964*(Y^2) + 0.2663*(D^2) - 0.2938*(XY) - 0.4382*(XD) + 0.4959*(YD) \quad (1)$$

Table 3 shows the analyzed regression coefficients for warpage based on coded units of different factors. The table shows that most P values

Table 3 Estimated regression coefficients for warpage

Term	Coefficient	SE coefficient	T	P
Constant	1.1295	0.2623	4.305	0.00
Sub thick	-0.8942	0.1171	-7.635	0.00
EMC thick	0.4458	0.1177	3.788	0.001
Die pitch	0.6502	0.1177	5.524	0.00
Sub thick * Sub thick	0.3287	0.2186	1.504	0.151
EMC thick * EMC thick	0.1964	0.2028	0.968	0.346
Die pitch * Die pitch	0.2663	0.2028	1.313	0.207
Sub thick * EMC thick	-0.2938	0.1420	-2.070	0.054
Sub thick * Die pitch	-0.4382	0.1420	-3.087	0.007
EMC thick * Die pitch	0.4959	0.1434	3.458	0.003
S = 0.4969 R-Sq = 88.7% R-Sq(adj) = 82.8%				

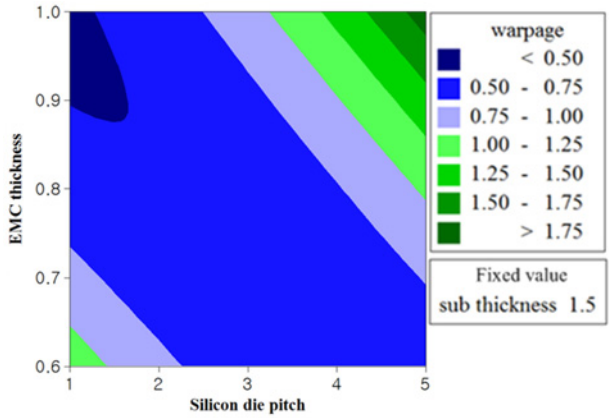

Fig. 11 Response contour plot of warpage

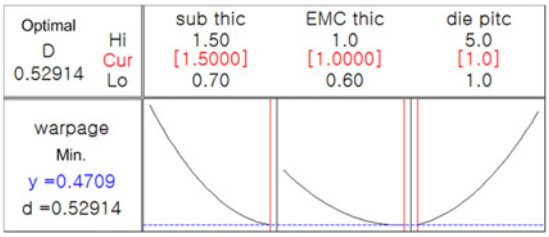

Fig. 12 Response optimization plot

are smaller than the significant level of 0.05, which confirms that the main effects, square, and secondary interactions of main variables on warpage are significant. Also, the reliability level of over 80% indicates is sufficiently persuasive (R-Sq = 88.7%, R-Sq (adj) = 82.8%).

Fig. 11 is the contour plot of warpage showing EMC thickness and silicon-die pitch with fixed 1.5 mm substrate thickness. The substrate thickness was fixed to 1.5 mm, which is the largest number among the selected conditions because warpage generation is reduced when substrate thickness is increased in the performed analysis results whereas the thickness does not affect semiconductor specifications and productivity.

The plot shows a wide distribution of warpage occurrences between 0.5 mm and 0.75 mm while the distribution is significantly reduced for

(a) Appearance of the equipment

(b) Top and bottom mold

Fig. 13 12-inch wafer level compression molding test equipment

0.5 mm or smaller. The plot helps to predict warpage occurrence in advance.

Fig. 12 shows the level of the optimum factor obtained by a regression model when the warpage set the minimum value. These results are deduced using the response optimizing method on the three factors (substrate, EMC thickness, die-pitch). According as the substrate and EMC thickness are larger, the warpage is tended to decrease. In addition, the smaller the die-pitch, tends to decrease the warpage. The warpage occurred in optimal factors(substrate thickness 1.5 mm, EMC thickness 1 mm, die-pitch 1mm) is 0.47 mm. By such methods, the condition to minimize warpage using RSM was found and analysis result based on the condition shows the warpage of 0.22 mm with approximately 0.25 mm error margins.

7. Experimental Verification

For verification of performed analyses, the following verification tests and analyses were carried out. The tests were conducted by molding pure EMC only on top of substrates without silicon-die due to the limitation in bonded wafer supply.

Fig. 13 shows the shape and molding of KNJ's molding equipment. The test equipment is a 300-mm wafer-ready molding equipment of compression type with high flatness of under 10 μm and clamping capacity of at least 10 tons. Also, the equipment is fitted with 4-point automated leveling module and EMC automated spraying module for precise molding leveling tuning to enable the insertion of a fixed amount of EMC into the molding.

Fig. 14 shows the samples of 12-inch compression molding test results in which warpage occurs. The generated warpage is approximately 3 mm. The substrate material used for the test was SUS304 (1.2 mm thickness) with EMC (600 μm molding thickness). Finite element analysis was carried out with identical condition to compare with the test results. The properties of EMC and adhesive tape are identical to those in Table 1 and SUS304 has the Young's modulus

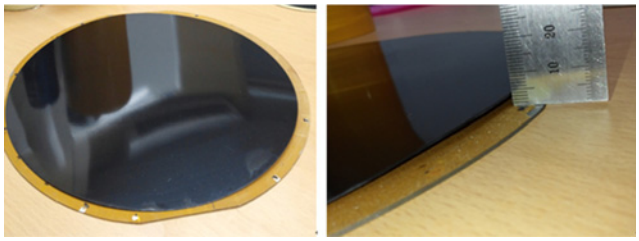

Fig. 14 Experiment result of compression molding

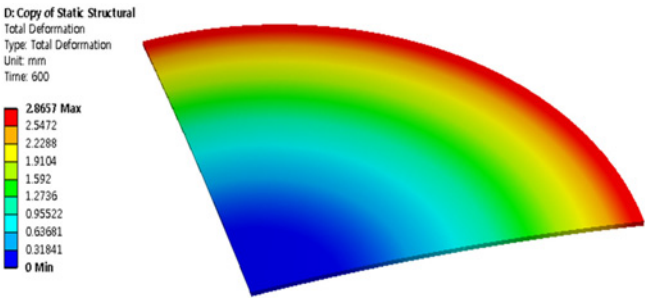

Fig. 15 Analysis result of warpage

of 193 GPa, Poison's ratio of 0.23, and CTE of 8 ppm/°C.

Fig. 15 shows the analysis result with the generated warpage of approximate 2.87 mm. The result shows the difference of approximate 0.13 mm from that of test results. Of course, there may have been bigger errors as the test results were measured using a ruler, but it is thought analysis results have similar values to test results. Moreover, the directions of warpage occurrences were both convex types.

8. Conclusion

This study carried out finite element analyses and analyzed the results statistically to find methods to minimize the warpage which is the most prominent problem occurring during molding processes in WLP technology. The conclusions are as following.

The analysis results of parameters according to different materials and thickness of substrate, and EMC thickness showed that the substrate materials with higher Young's modulus generate lower warpage and thinner EMC and thicker substrate reduce warpage occurrence when the EMC and substrate have similar CTE values. Moreover, die thickness variances confirmed that warpage is reduced when the EMC thickness is reduced.

It was found through distribution analysis that the variable with the largest impact on warpage is substrate thickness and EMC thickness was the second most important factor. Also, it was found that the impacts of variables on the interactions were not large. Moreover, it was possible to find the condition to minimize warpage by deriving regression equation based on RSM.

This study proves that selection of optimal package material and adjustment of component dimensions can minimize warpage occurring during contraction sufficiently.

ACKNOWLEDGEMENT

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