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Optimized stateful material implication logic for three-dimensional data manipulation

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ABSTRACT

The monolithic three-dimensional integration of memory and logic circuits could dramatically improve the performance and energy efficiency of computing systems. Some conventional and emerging memories are suitable for vertical integration, including highly scalable metal-oxide resistive switching devices ("memristors"). However, the integration of logic circuits has proven to be much more challenging than expected. In this study, we demonstrated memory and logic functionality in a monolithic three-dimensional circuit by adapting the recently proposed memristor-based stateful material implication logic. By modifying the original circuit to increase its robustness to device imperfections, we experimentally showed, for the first time, a reliable multi-cycle multi-gate material implication logic operation and half-adder circuit within a three-dimensional stack of monolithically integrated memristors. Direct data manipulation in three dimensions enables extremely compact and high-throughput logic-in-memory computing and, remarkably, presents a viable solution for the Feynman Grand Challenge of implementing an 8-bit adder at the nanoscale.

1 Introduction

Material implication (IMP) is a universal Boolean logic (Fig. 1(a)) that is particularly suitable for implementing "stateful" logic circuits [1]. At the core of stateful logic are memory devices that serve the dual roles of performing computation and storing (latching) the results. The implementation with the greatest potential is based on highly scalable memristors [2–8]. In the simplest case, memristors are two-terminal devices, whose conductance can be switched reversibly with relatively large (write) voltages, e.g., applying $V \geqslant V_{\text{set}}$ to switch the device to the ON state, which is characterized by high conductance G_{ON}, and $V \leqslant V_{\text{reset}}$ to switch it to the OFF state, which has low conductance G_{OFF} (Fig. 1(b)). The device's conductance remains unchanged when relatively small (read) voltages are applied. Specifically, in one realization of memristor-based IMP logic, logic states "0" and "1" are encoded using the low and high conductive states of a memristor,

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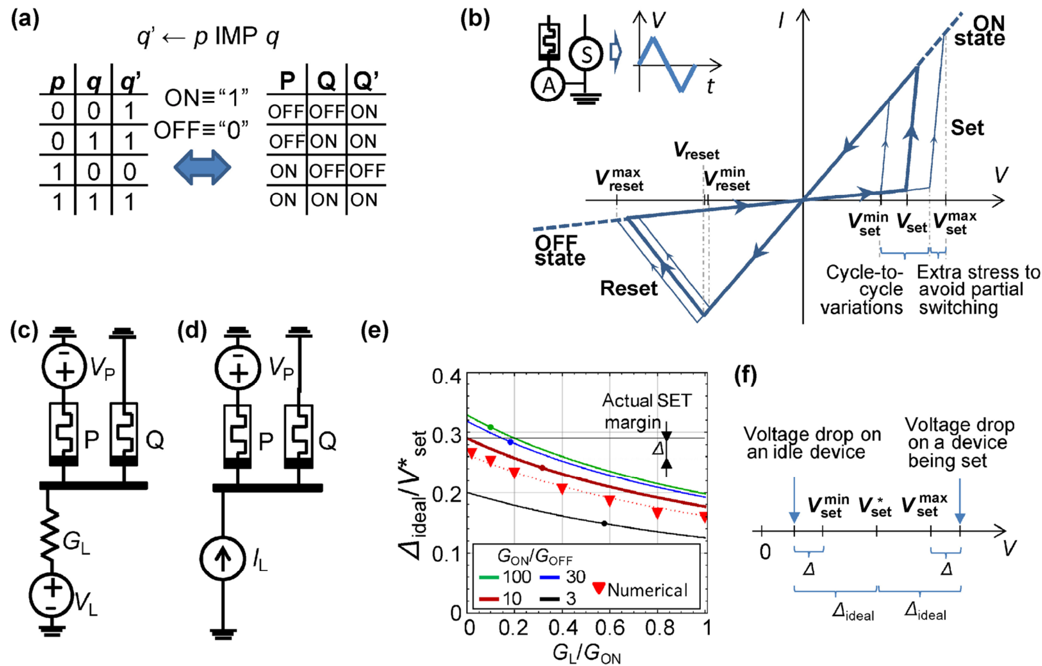


Figure 1 Memristor-based material implication logic. (a) Logic truth table and its mapping to memristor's states. (b) A sketch of simplified (linear) I–V switching curve for a memristor. The thick (thin) solid lines schematically show an I–V curve with average (maximum and minimum) set and reset thresholds. The inset shows the experimental setup. (c) Originally proposed [1] and (d) optimized IMP logic circuits with particular polarity of memristors. (Other possible configurations are shown in Fig. S6 in the ESM.) (e) The set margin as a function of the load conductance for several representative ON-to-OFF conductance ratios. For convenience, the margins and load conductances are normalized with respect to mid-range set voltages $V^*_{\rm set}$ and $G_{\rm ON}$, respectively. The solid dots show the margins for the previously proposed optimal load conductance $G_{\rm L}$', while the solid triangles are the margins that were obtained with numerical simulations using the fitted experimental device characteristics (shown in Fig. S4(b) in the ESM). The solid grey lines denote the maximum set margins, while the differences between the solid and dashed lines show the actual set margins when taking into account variations in the set threshold voltage extracted from the experimental data (shown in Fig. 3(b) inset). (f) A diagram showing the definition of margins in the context of set transition.

respectively. Using the divider circuit shown in Fig. 1(c), $q' \leftarrow p$ IMP q is an implication between logic variables q and p, stored in memristors Q and P, respectively, which is performed by applying specific "clock" voltage pulses $V_{\rm P}$ and $V_{\rm L}$, so that the result of the computation is placed in Q as a new conductive state. Similar to other nonconventional computing approaches [9, 10], voltage pulses $V_{\rm P}$ and $V_{\rm L}$ are effectively clock signals that do not carry any information. Their amplitudes are fixed and are chosen according to the load conductance $G_{\rm L}$ and memristor parameters, e.g., $G_{\rm ON}$, $G_{\rm OFF}$, $V_{\rm set}$, and $V_{\rm reset}$ for the ideal memristor without variations (Fig. 1(b)), such that device Q switches from the low to high conductive state only when device P is in the low conductive state.

The appealing feature of stateful logic is that the result of the logic operation is immediately latched. Thus, IMP logic circuits based on non-volatile memristors are immune to power supply shortages, which could be advantageous in the context of energy scavenging applications. Even more importantly, stateful logic does not draw static power and enables very high throughput information processing because of the possibility of fine-grained pipelining. In many respects, stateful IMP logic is similar to other logic-in-memory computing approaches [9–13] that do not suffer from the memory bottleneck problem of conventional Von Neumann architectures [14]. Several theoretical studies have predicted a significantly higher performance and energy efficiency for memristor-based IMP logic circuits (and very similar concepts) compared to conventional approaches for high-throughput computing applications [15–22].

Although IMP logic has already been implemented

with a variety of memory devices [22–29], prohibitively large cycle-to-cycle and device-to-device variations in memristors have limited experimental demonstrations to simple gates with stand-alone devices and typically just a few cycles of operations. (In addition, for practical, large-scale IMP logic circuits, the sneak-path problem is expected to be another major challenge [30–34] (see Fig. S9 in the Electronic Supplementary Material (ESM)). Device variations reduce the allowed V_P and V_L voltage range within which correct operation is assured. In fact, IMP logic is more prone to variations, and a demonstration of memory functionality does not guarantee that the same circuit can be adapted for performing logic operations (section S3 in the ESM). Extending IMP logic to more promising three-dimensional circuits [4–7, 35, 36] is even more difficult, because more sophisticated fabrication processes and a higher integration density can further aggravate the device variation problems. The main goal of this study was to address these challenges and ultimately demonstrate robust stateful IMP logic in monolithic three-dimensional metal-oxide memristor structures.

2 Theoretical and experimental

Significant switching voltage variations are a major challenge for implementing IMP logic. Therefore, it is natural to choose circuit parameters (i.e., G_L, V_L, and V_P) that maximize the range of variations (also referred as margins) that can be tolerated without comprising the correctness of the logic operation. Some earlier works suggested choosing $G_L' = (G_{ON} \cdot G_{OFF})^{1/2}$ for the most optimal design [30, 37].

However, our analytical and numerical analyses of IMP logic operations (see section S3 in the ESM for details) showed that the set margins monotonically increased as the load conductance decreased (Figs. 1(e) and 1(f) and Fig. S7 in the ESM). The largest margins were found for $G_L = 0$, which could not be implemented with the original circuit, although it could easily be realized by replacing the load resistance and voltage source with a current source (Fig. 1(d)). The transition from the original circuit with the earlier suggested G_L' to the modified one with an optimized current source I_L increased the set margins by more than 20% (Fig. 1(e)).

The performance of this circuit was tested on a two-level stack with four metal-oxide memristors. Two memristors were fabricated in the bottom level, and two others were monolithically integrated directly above, with all of the devices sharing a common middle electrode (Figs. 2(a)–2(c)). The major steps involved in the fabrication were the patterning of the Ta/Pt bottom electrode using e-beam evaporation and lift-off, patterning of the bottom device's Al_2O_3/TiO_{2-x} layer and Ti/Pt middle electrode using reactive sputtering and lift-off, planarization by chemical mechanical polishing and the etch-back of the plasma-deposited sacrificial silicon oxide, and patterning of the top device's Al_2O_3/TiO_{2-x} layer and Ti/Pt top electrode by reactive sputtering and lift-off (Figs. 2(d)–2(g)). The device structure, oxide film thicknesses, and titanium oxide stoichiometry, which was controlled by changing the oxygen to argon flow ratio during sputtering, were selected based on our earlier study [38], with the primary objective of lowering the forming voltages and improving the uniformity of the switching characteristics.

In particular, thin Ti and Ta layers were deposited to improve the electrode adhesion. The addition of Ti to the middle and top electrodes also ensured ohmic interfaces with the titanium dioxide layer, which was important for the device's asymmetry [2, 39]. Low forming voltages reduced the electrical stress during electroforming [38], while *in-situ* contacts between the titanium oxide and the metal electrodes, which were fabricated without breaking the vacuum, ensured high-quality interfaces [40], with both factors essential for improving the uniformity of the memristor's switching characteristics. Furthermore, planarization reduced the middle electrode roughness, which resulted from the residual sidewall deposition and was critical for lowering the variations in top-level devices (Figs. S1–S3 in the ESM). The absence of an annealing step, which is typically used for fine-tuning the defect profile in metal oxide memristors [8, 38], and the low-temperature (<300 °C) budget during the fabrication, simplified the three-dimensional integration and made the fabrication process compatible with conventional semiconductor technology. More details about the fabrication are provided in section S1 in the ESM.

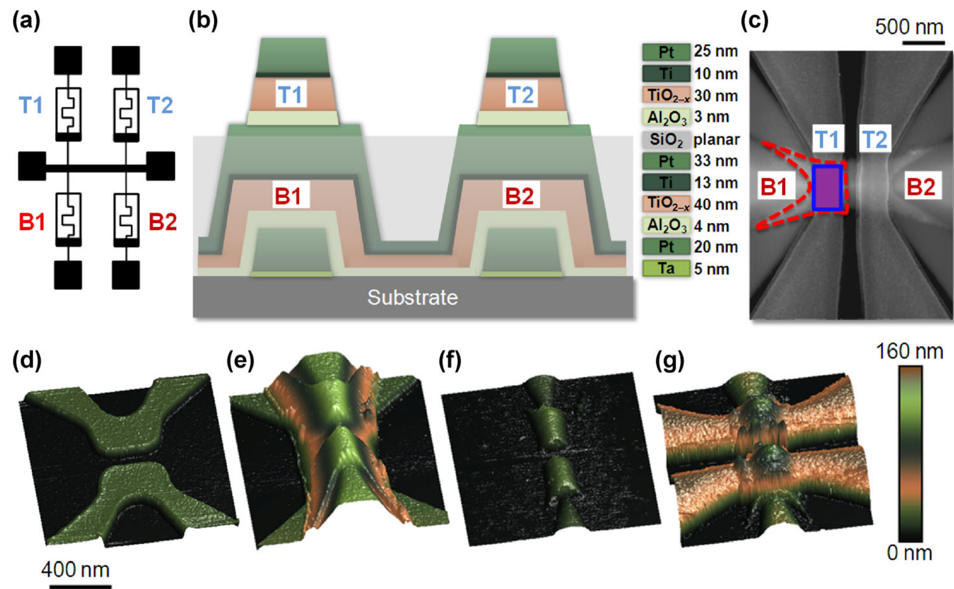


Figure 2 Stacked Al_2O_3/TiO_{2-x} memristor circuit: fabrication details. (a) An equivalent circuit. B1 and B2 denote bottom devices, while T1 and T2 are the top ones. (b) A drawing of the device's cross-section showing the material layers and their corresponding thicknesses. (c) A top-view scanning-electron-microscope image of the circuit. The red, blue, and purple colors were added to highlight the locations of the bottom and top devices, and their overlap, respectively. (d) and (e) Top-view atomic-force-microscope images of the circuit during different stages of fabrication, in particular showing: (d) the bottom electrode, (e) middle electrode, (f) middle electrode after the planarization step, and (g) top electrode.

Figures 3(a) and 3(b) show typical memristor *I*–*V* characteristics obtained by applying positive and negative quasi-direct current (DC) triangular voltage sweeps. The switching polarities of all the devices correspond to the bottom active interface, which is in agreement with the devices' asymmetric structure. For all the devices, the set switching was rather sharp, whereas the reset process was gradual. For example, the device B1 reset transition started at $V_{\text{reset}}^{\text{min}} \approx -1.5$ V; however, to avoid partial switching, voltage exceeding $V_{\text{reset}}^{\text{max}} \approx -2.2$ V had to be applied (Fig. 3(b)). A slightly thicker titanium dioxide layer for the bottom devices resulted in higher set threshold voltages compared to those of the top ones (Fig. 3(a) and Fig. S4 in the ESM). As Figs. 3(c) and 3(d) show, repetitive switching between the ON and OFF states of one device did not disturb the states of others, which suggested that the thermal crosstalk [41] was negligible in this system. The current ratios measured at 0.1 V between the ON and OFF states were well above one order of magnitude for all the memristors. Other characteristics such as the endurance and retention were close to those reported earlier for similar devices [37, 42].

3 Results and discussion

Because the set threshold voltage variations were non-negligible (Fig. S5 in the ESM), the 20% boost in variation tolerance provided by the proposed circuit design was critical for our experiment. It should be noted that, in principle, IMP logic can also be implemented using a memristor's reset transition, i.e., assuming that logic states "0" and "1" are represented by the ON and OFF states instead. However, this would not be helpful in our case, because the gradual reset transition presents an even larger problem (see section S3.1 in the ESM for more details).

Using the variation tolerant design with optimal values of I_L and V_P, which were obtained from accurate numerical simulations based on experimental (nonlinear) *I*–*V* curves, we successfully demonstrated IMP logic with the fabricated memristor circuit (Figs. 4 and 5, and Figs. S9 and S10 in the ESM). For simplicity, the current source used was the one provided by the source measurement unit (SMU) of the Agilent measurement equipment. In a hybrid complementary metal-oxide-semiconductor (CMOS)/memristor integrated circuit,

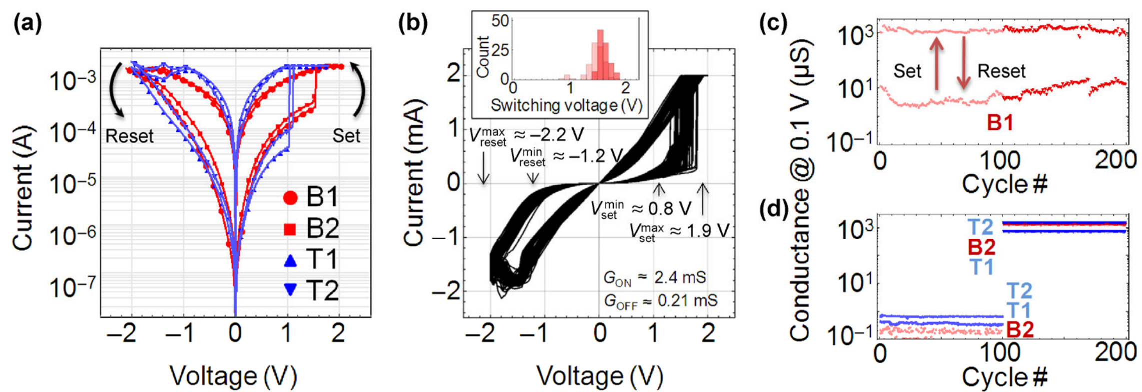


Figure 3 Stacked Al_2O_3/TiO_{2-x} memristor circuit: electrical characterization. (a) Representative *I*–*V* curves for all devices. (b) Switching *I*–*V* curves showing 100 cycles of operation for device B2. The light and dark color histograms in the inset show the corresponding cycle-to-cycle V_{set}^{min} and V_{set}^{max} statistics. (c) Conductance of device B1 that was repeatedly switched 200 times and (d) those of the other three devices in the circuit that were kept in the OFF states for the first 100 cycles, and then in the ON states for the remaining 100 cycles. In all the experiments, the memristors were switched by applying triangular voltage pulses to the corresponding top terminal of the device.

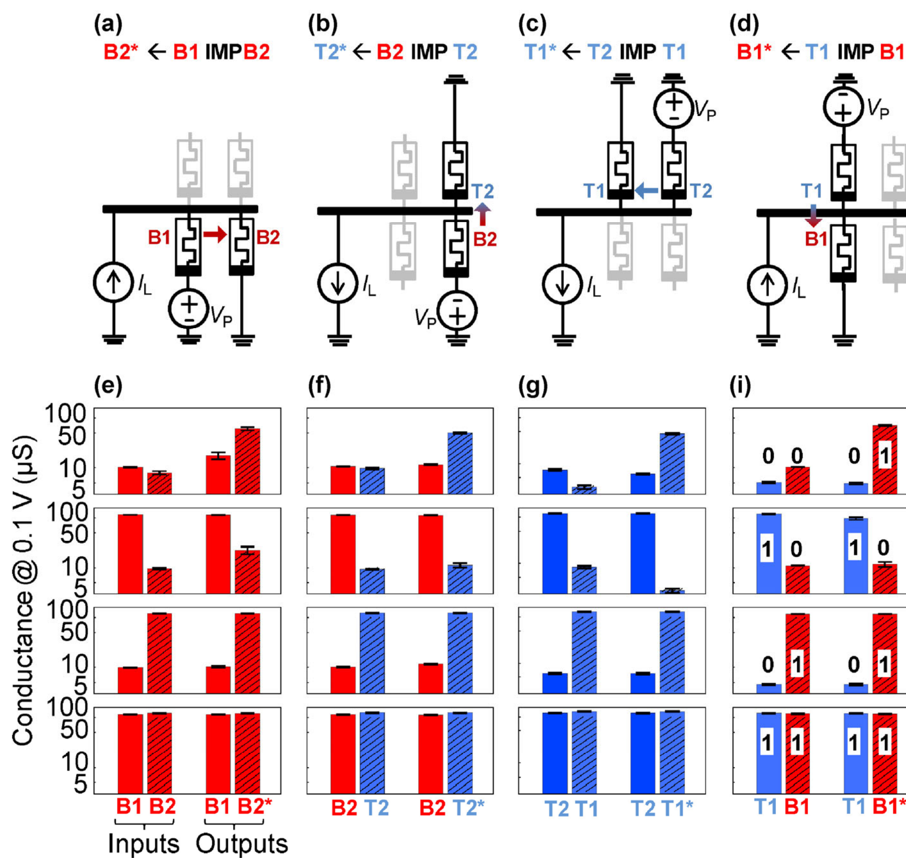


Figure 4 Three-dimensional data manipulation using optimized material implication logic circuit. (a)–(d) Circuit schematics and (e)–(i) corresponding experimental results showing device's conductances before and after IMP operation implemented with various initial states and pairs of memristors in a circuit. In (e)–(i), each graph shows the averaged conductances and their standard deviations for 20 experiments. IMP logic was performed by biasing the corresponding device with V_P = 0.25 V and applying a 10-ms I_L = 550 μA load current pulse for the cases in (a) and (d), i.e., when the result was written into the bottom device, and I_L = 200 μA when the output was one of the top devices ((b) and (c)).

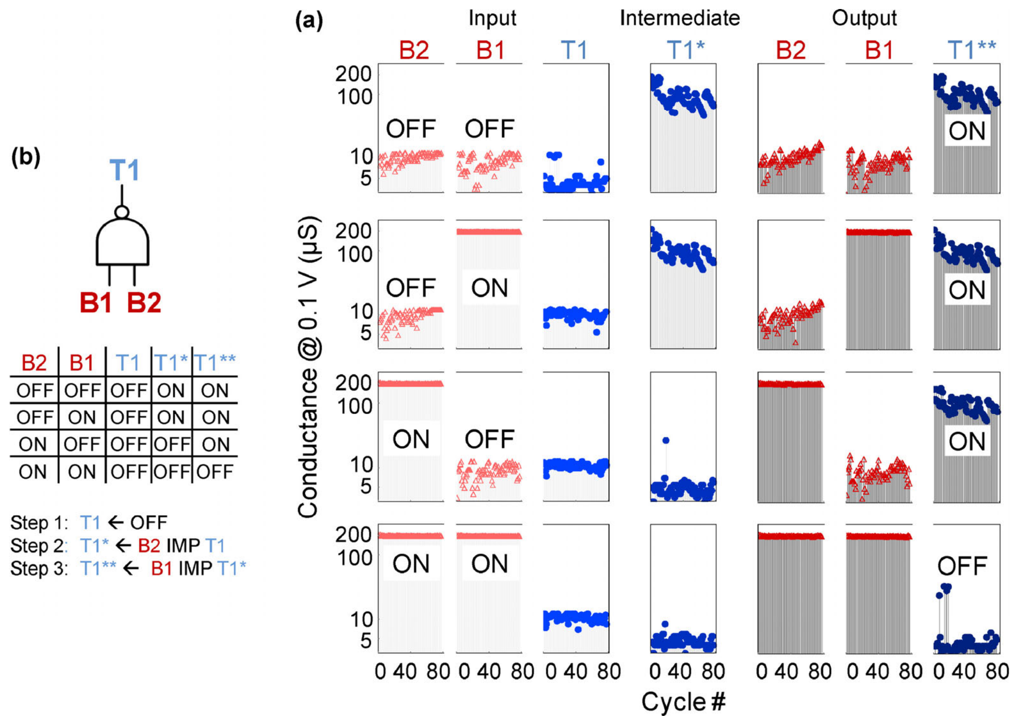


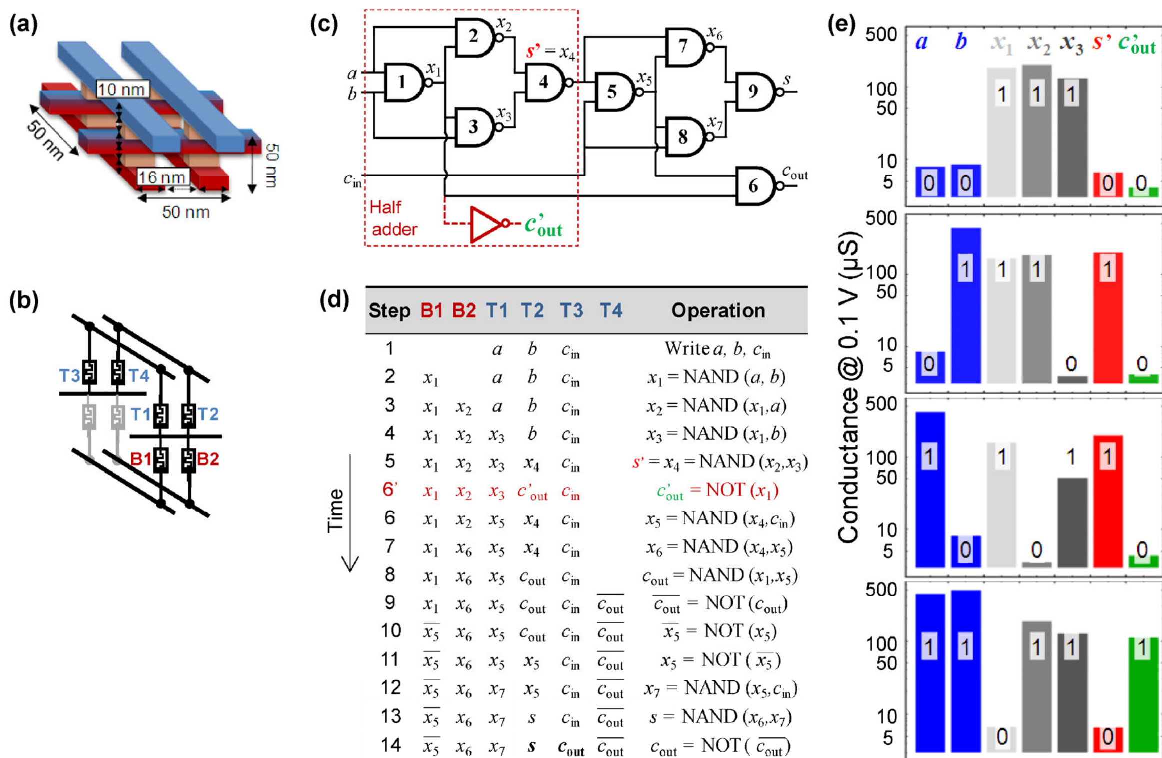
Figure 5 Three-dimensional NAND Boolean operation via optimized material implication logic. (a) Schematics and truth table showing intermediate steps. (b) Experimental results showing 80 cycles of operation with >93% yield for all four combinations of initial states. The initial states were set similar to those in the Fig. 4 experiments, while V_P = –0.15 V, and the applied load current was a 10-ms pulse with I_L = –550 μA.

the physical implementation could be based on a circuit as simple as just one CMOS field effect transistor working in its saturation regime. In the first set of experiments, a series of IMP operations were performed sequentially utilizing four different pairs of memristors (Fig. 4 and Fig. S9 in the ESM). Before each logic operation, the devices were always written to the specified initial states. Therefore, this experiment provided proof of memory and logic functionality implemented within the same circuit. Moreover, the considered pairs constituted all of the possible combinations of the memristor's polarities in an IMP circuit and hence were sufficient to compute and move information in any direction within the circuit.

Normally, during the first experiment, the output conductances are close to the extreme ON and OFF values. Thus, it should be possible to cascade IMP logic gates, i.e., use the output of one gate as an input for another. To confirm this, in the next series of experiments, we implemented the NAND Boolean logic operation, for which the inputs were the states of the bottom-level devices and the output was stored in one of the top-level memristors (Fig. 5 and Fig. S10 in the ESM). The NAND gate was realized in three steps: an unconditional reset, followed by two sequential IMP operations [1]. The result of the first IMP operation was stored in the top-level device, which was then used as one of the inputs to the second IMP gate. In some rare cases (~6.5% of the total IMP operations), there is some visible reduction in the ON-to-OFF conductance ratio. This is not desirable because the set margins decrease with the ON-to-OFF ratio (Fig. 1(e)). One plausible solution to restore the ratio is to read the state and write it back, i.e., similar to what was implemented in the first experiment. A better approach, which does not involve a read operation, is to apply a specific voltage pulse to the IMP logic circuit (see the experimental results on Figs. S11 and S12 and their discussion in section S4 in the ESM).

Interestingly, the approach based on 3D IMP logic enables a practical solution to one of the Feynman Grand Challenges—the implementation of an 8-bit adder that fits in a cube no larger than 50 nm in any

dimension [43]. The major building block—a full adder, which adds Boolean variables a, b, and c_{in} to calculate the sum s and carry-out c_{out}, requires six memristors and consists of two monolithically stacked 2 × 2 crossbars sharing the middle electrodes (Fig. 6(a)). Two of the memristors in the crossbar are assumed to be either not formed or always kept in the OFF state (Fig. 6(b)), which eliminates the typical leakage currents for crossbar circuits [30–34] and makes the IMP logic set margins similar to those of the demonstrated circuit. In particular, at the start of computation, a, b, and c_{in} are written to the specific locations in the circuit (Fig. 6(c)). A sequence of NAND operations, each consisting of one unconditional reset step and two IMPs (Fig. 5), is then performed to compute c_{out} and s according to the particular implementation of Fig. 6(d). Occasional NOT operations are implemented with one unconditional reset step and one IMP step and used to move variables within the circuit. In total, the full adder is implemented with nine NAND gates and four NOT gates, i.e., 13 unconditional reset steps and 22 IMP steps. The simplest way to read an output of an adder is to electrically measure the state of memristors T2 and T3 (Fig. 6(c)). Alternatively, the output can be sensed as a mechanical deformation of the upper metal electrodes, which is often observed in metal-oxide memristors [44] or using scanning Joule expansion microscopy [45]. A full 8-bit adder could be implemented in a ripple-carry style [46] by performing the full adder operation eight times. To verify that the proposed adder implementation is realistic, we experimentally demonstrated a half-adder circuit on a 2 × 2 vertical stack of memristors (Fig. 6(e)). Such a half-adder implementation requires one NOT and



Step	B1	B2	T1	T2	T3	T4	Operation
1			a	b	c_{in}		Write a, b, c_{in}
2	x_1		a	b	c_{in}		x_1 = NAND (a, b)
3	x_1	x_2	a	b	c_{in}		x_2 = NAND (x_1,a)
4	x_1	x_2	x_3	b	c_{in}		x_3 = NAND (x_1,b)
5	x_1	x_2	x_3	x_4	c_{in}		s' = x_4 = NAND (x_2,x_3)
6'	x_1	x_2	x_3	c'_{out}	c_{in}		c'_{out} = NOT (x_1)
6	x_1	x_2	x_5	x_4	c_{in}		x_5 = NAND (x_4,c_{in})
7	x_1	x_6	x_5	x_4	c_{in}		x_6 = NAND (x_4,x_5)
8	x_1	x_6	x_5	c_{out}	c_{in}		c_{out} = NAND (x_1,x_5)
9	x_1	x_6	x_5	c_{out}	c_{in}	$\overline{c_{out}}$	$\overline{c_{out}}$ = NOT (c_{out})
10	$\overline{x_5}$	x_6	x_5	c_{out}	c_{in}	$\overline{c_{out}}$	$\overline{x_5}$ = NOT (x_5)
11	$\overline{x_5}$	x_6	x_5	x_5	c_{in}	$\overline{c_{out}}$	x_5 = NOT ($\overline{x_5}$)
12	$\overline{x_5}$	x_6	x_7	x_5	c_{in}	$\overline{c_{out}}$	x_7 = NAND (x_5,c_{in})
13	$\overline{x_5}$	x_6	x_7	s	c_{in}	$\overline{c_{out}}$	s = NAND (x_6,x_7)
14	$\overline{x_5}$	x_6	x_7	s	c_{out}	$\overline{c_{out}}$	c_{out} = NOT ($\overline{c_{out}}$)

Figure 6 Adder implementation with 3D IMP logic. (a) Drawing of a structure with dimensions satisfying Feynman Grand Challenge and (b) its equivalent circuit. (c) and (d) The sequence of steps and specific mapping of the logic variables to the circuit's memristors for a particular implementation of the full/half adder shown in (d). In (d), steps 1 through 5 are common for the full and half adders. Step 6' is only required for the half adder, while steps 6 through 14 are only used for the full adder. In addition, the last step for the full adder, in which c_{out} is placed in the same location as c_{in}, is only required to ensure a modular design, but might be omitted in more optimal implementations. (e) An experimental demonstration of a half adder implemented following steps 1 through 5 and step 6' from (d). I_L = 800 μA and V_P = 0.6 V were used to perform steps 2 and 3, while I_L = –375 μA and V_P = –0.3 V were used for steps 4 and 5.

four NAND operations (Figs. 6(c) and 6(d)), i.e., about half of the complexity of a full adder implementation.

4 Conclusions

In summary, we demonstrated an optimized approach for logic-in-memory computing and proved its reliability by performing hundreds of cycles of three-dimensional data manipulation in monolithically integrated circuits. As the rapid progress of memristor technology continues, it will eventually become sufficiently advanced to enable large-scale integration of memristive devices with sub-nanosecond, pico-Joule switching capable of enduring > 10^{14} cycles with high nonlinearity, which has already been demonstrated for discrete devices [2, 3]. As a result, we expect that the presented approach will become attractive for high-throughput and memory-bound computing applications suffering from memory bottleneck problems. Furthermore, we showed how the presented approach establishes a realistic pathway toward resolving one of the Feynman Grand Challenges. The remaining challenge is to scale down the circuitry (Fig. 6(a)), which does not seem to be an unrealistic task given that discrete metal-oxide memristors with similar dimensions [8, 47] and much more complex (but less dense) memristive circuits [4, 5, 7, 38] have already been demonstrated.

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