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Threshold voltage tuning and printed complementary transistors and inverters based on thin films of carbon nanotubes and indium zinc oxide

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ABSTRACT

Carbon nanotubes (CNTs) have emerged as an important material for printed macroelectronics. However, achieving printed complementary macroelectronics solely based on CNTs is difficult because it is still challenging to make reliable n-type CNT transistors. In this study, we report threshold voltage (V_{th}) tuning and printing of complementary transistors and inverters composed of thin films of CNTs and indium zinc oxide (IZO) as p-type and n-type transistors, respectively. We have optimized the V_{th} of p-type transistors by comparing Ti/Au and Ti/Pd as source/drain electrodes, and observed that CNT transistors with Ti/Au electrodes exhibited enhancement mode operation ($V_{th} < 0$). In addition, the optimized In:Zn ratio offers good n-type transistors with high on-state current (I_{on}) and enhancement mode operation ($V_{th} > 0$). For example, an In:Zn ratio of 2:1 yielded an enhancement mode n-type transistor with $V_{th} \sim 1$ V and I_{on} of 5.2 μA. Furthermore, by printing a CNT thin film and an IZO thin film on the same substrate, we have fabricated a complementary inverter with an output swing of 99.6% of the supply voltage and a voltage gain of 16.9. This work shows the promise of the hybrid integration of p-type CNT and n-type IZO for complementary transistors and circuits.

1 Introduction

In the past decade, single-wall carbon nanotube (SWCNT) thin-film transistors (TFTs) have been extensively studied as a potential replacement of amorphous silicon TFTs due to their superior electrical performance in terms of field-effect mobility, on/off current ratio (I_{on}/I_{off}), small operation voltage and high-speed operation [1–4]. As-synthesized carbon nanotubes (CNTs) have capabilities of being either

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semiconducting or metallic depending on chirality [5, 6], and there have been a number of efforts to selectively eliminate metallic ones in order to increase I_{on}/I_{off} of CNT TFTs. Various approaches have been developed to remove metallic nanotubes from existing nanotube devices [7–11]. However, these methods cannot be easily scaled up and/or can degrade device performance or even severely damage devices. An important alternative is exploiting separated semiconducting CNT solutions, which are commercially available, by means of deposition techniques such as printing [4, 12], spin coating [13, 14], incubation [3, 15, 16], or drop casting [17]. In particular, printing has the advantage of allowing deposition of CNTs at room temperature, which makes device and circuit fabrication on flexible substrates possible. In addition, there is no photolithography process involved during the printing process, and hence it can reduce the cost of fabrication.

While p-channel TFTs have been demonstrated with SWCNTs as active channel materials [18, 19], metal oxide semiconductors are good candidates for n-channel transistors. These two kinds of semiconductors have noticeable advantages over traditional amorphous silicon and organic semiconductors, such as relatively high carrier mobility, high stability under ambient conditions, low manufacturing cost, high transparency, and room-temperature fabrication compatibility [20]. Indeed, there have been many reports, especially for metal oxides such as indium zinc oxide (IZO) [21–25], zinc oxide [26, 27], and indium gallium zinc oxide [28]. Due to the ease of precursor preparation, most studies of these materials have employed sputtering [21, 27] and spin coating [22, 23, 26, 28] techniques rather than solution-processed inkjet printing technique [24, 25]. However, the latter is more desirable since it offers scalability and cost efficiency with patterning, because there is no clean-room process required.

Combining p-type and n-type transistors to construct complementary logic circuits is preferred for the reason that they have low static power consumption, full voltage swings, and large noise margins [29, 30]. With these advantages, manufacturing of both p-type and n-type transistors on the same substrate giving an integrated complementary circuit is desired. Nevertheless, an inexpensive, uncomplicated process is a challenge. The inkjet printing technique is a good candidate, as it allows fabrication of TFTs without the involvement of masks or photolithography processes, which also results in reduced fabrication time. Thus, using inkjet printing is very effective as a low-cost technology to print both enhancement mode p-type and n-type semiconductors for complementary transistors and circuits.

In this paper, we report inkjet printed complementary transistors and inverters comprising p-type CNT and n-type IZO semiconductors, and threshold voltage (V_{th}) tuning of both p-type and n-type transistors. We have compared Ti/Au and Ti/Pd as source/drain (S/D) electrodes for p-type TFTs, and it was clearly demonstrated that Ti/Au metal contacts offered enhancement operation with $V_{th} < 0$. In addition, the effects of varying In:Zn ratios (1:1, 2:1 and 3:1) of the IZO precursor solution were studied. The optimized In:Zn ratio was found to be 2:1, as devices with this ratio exhibited relatively high on-state current (I_{on}) and enhancement mode operation ($V_{th} > 0$). Last but not least, we have achieved the printing of a complementary inverter with an output swing of 99.6% of the supply voltage (V_{DD}) and voltage gain of 16.9, made up of an enhancement mode CNT transistor (p-type) and an enhancement mode IZO transistor (n-type) on the same substrate.

During the preparation of this manuscript, we became aware of a recent publication, in which complementary ring oscillators were demonstrated using printed CNTs and another metal oxide, zinc tin oxide [31]. Both this work and our work demonstrate the great potential of printing CNTs and metal oxides (IZO in our work and zinc tin oxide in Ref. [31]) for complementary electronics, while our work presents more investigation on the V_{th} tuning of the transistors.

2 Experimental

2.1 IZO precursor solution preparation

Indium(III) nitrate hydrate ($In(NO_3)_3 \cdot xH_2O$) and zinc acetate dihydrate ($Zn(CH_3COO)_2 \cdot 2H_2O$) were dissolved in 2-methoxyethanol as precursors of indium oxide

and zinc oxide with a concentration of 0.6 and 0.3 M, respectively. These two solutions were stirred with a speed of 3,500 rpm at 50 °C for 1 h and then mixed to obtain In:Zn ratios of 1:1, 2:1, and 3:1. During the mixing process, ethanolamine (EA) was added to the mixture as a stabilizer to improve the uniformity and viscosity of the solution to meet the inkjet printing requirements. The volume concentration of the stabilizer added was found to be optimized at 32%. Lastly, the final solution was stirred at 50 °C at 3,500 rpm for 1 h and then aged overnight.

2.2 IZO TFT printing

First, 1 nm/50 nm Ti/Au S/D electrodes were patterned onto a Si/SiO_2 (50 nm) wafer by a photolithography process. Next, the well-sonicated IZO precursor solution was printed onto the channel region as the active material of n-type transistors via a GIX Microplotter Desktop (Sonoplot Inc.), followed by air annealing at 500 °C for 1 h.

2.3 CNT TFT printing

First, a Si/SiO_2 (50 nm) substrate was immersed into diluted aminopropyltriethoxysilane (APTES) solution (APTES/isopropanol alcohol (IPA) = 1/10) for 10 min, in order to form an amine-terminated monolayer on top of the substrate and improve the adhesion between CNTs and the substrates. Then, the substrate was rinsed with IPA and blown dry with N_2. After that, a density gradient ultracentrifugation (DGU)-separated 98% semiconducting enriched SWCNT solution (IsoNanotubes-S_DGU, 1.0 mg in 100 mL of aqueous solution, NanoIntegris Inc.) was printed in the channel region as the active material of p-type transistors via the inkjet printer. After printing, the samples were left in air for 30 min and then baked at 80 °C for 20 min to remove the solvent. Finally, they were aged overnight to improve the adhesion between CNTs and the substrate before being rinsed with deionized (DI) water to remove surfactant residue from the CNT film.

3 Results and discussion

Figures 1(a) and 1(b) show schematic diagrams of the inkjet printed integrated complementary inverter fabrication process. Figure 1(a) shows the printing process of a back-gated IZO TFT as the n-type transistor of the inverter. Briefly, the IZO precursor solution was printed on a Si/SiO_2 (50 nm SiO_2) substrate with pre-patterned photolithography Ti/Au (1 nm/50 nm) S/D electrodes. Post-printing annealing was performed in order to convert the printed precursor film into IZO, which acts as the active material in the n-type transistor. Similarly, Fig. 1(b) shows the printing process of an SWCNT TFT. A 98% semiconducting enriched SWCNT solution was printed as the active material for the p-type transistor of the inverter. Before the printing of CNT, the Si/SiO_2 substrate was functionalized with APTES to improve the adhesion between SWCNT and the Si/SiO_2 substrate, following our previously published recipes [3, 4, 15, 16].

Immediately after printing, the CNT film was inspected with an optical microscope to check the quality of the film. Figure 1(c) shows that the pre-annealed CNT film of the CNT TFT sample has good uniformity and no cracks. Then, a field emission scanning electron microscope (FESEM) was utilized to examine the uniformity and density of the CNT networks in the channel region of the TFT. From the FESEM image in Fig. 1(d), the density of CNT networks is approximately 26–35 tubes/μm^2, which is a viable density for TFT applications according to our previously published work [4, 15].

Figure 1(e) illustrates an optical image of a printed IZO TFT after annealing. It is evident that the IZO layer has good shape and uniformity. This well-controlled printing process was realized by optimizing the amount of EA added in the precursor ink to achieve the desired viscosity for inkjet printing. The FESEM image of an IZO TFT (Fig. 1(f)) shows the uniformity of the IZO film after air annealing at 500 °C for one hour.

Electrical measurements were carried out for the inkjet printed back-gated CNT TFTs. Histograms of normalized on-current (I_{on} x L/W), current on/off ratio and field-effect mobility of 20 CNT TFTs are shown in Figs. S1(a)–S1(c), respectively (in the Electronic Supplementary Material (ESM)). We found that most of the printed CNT devices exhibited I_{on} in the range between 0.8 and 9.5 μA with gate bias (V_G) of –10 V

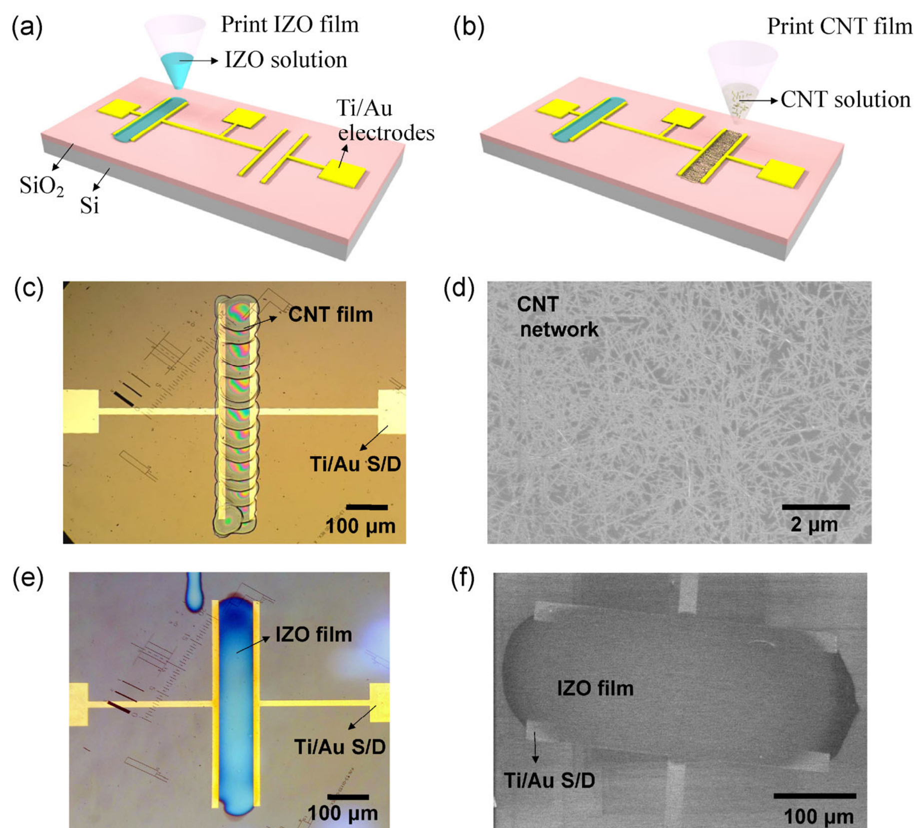

Figure 1 Schematic diagrams of the printed complementary inverter fabrication process, and optical and SEM images of printed back-gated CNT and IZO TFTs. Schematic diagrams demonstrate (a) the printed complementary inverter fabrication process, including printing of IZO precursor solution as the active material for n-type transistor and (b) printing of 98% semiconducting-enriched SWCNT solution as the active material for p-type transistor. (c) An optical image of a printed CNT TFT (before annealing). (d) An SEM image of the CNT network in the channel region. (e) An optical image of a printed IZO TFT (after annealing). (f) An SEM image of a printed back-gated IZO TFT.

and drain voltage (V_D) of 1 V. The devices possess I_{on}/I_{off} ratios of 10^4–10^6 with mobilities of 1–5 $cm^2/(V \cdot s)$ and V_{th} of –1.0—–3.0 V. These features are comparable with those demonstrated in our previously published works on printed CNT TFTs [4]. The electrical characteristics of one representative CNT device with channel length (L) of 100 μm and channel width (W) of 500 μm are presented in Figs. 2(a) and 2(b). As shown in Fig. 2(a), the output (I_D–V_D) characteristics of the representative CNT device exhibited a saturation behavior as V_D became more negative. Figure 2(b) shows the transfer (I_D–V_G) characteristics of the same device. The black curve represents the I_D–V_G characteristics on a linear scale. From this plot, one can see that I_{on} is 5.2 μA when V_G is –10 V and V_D is 1 V. In addition, one can find V_{th} to be around –1.4 V. The I_D–V_G characteristics on a logarithmic scale (the blue curve in Fig. 2(b)) indicate that I_{on}/I_{off} is 1×10^6. The transconductance–gate voltage (g_m–V_G) characteristics are also plotted in Fig. 2(b) in red, where the peak g_m and the mobility of this CNT device were extracted to be 1.5 μS and 4.38 $cm^2/(V \cdot s)$, respectively, based on the parallel plate model. Statistical V_{th} analysis was carried out for 20 printed CNT devices. As shown in Fig. 2(c), most devices show V_{th} between –1.0 and –3.0 V, which indicates that most CNT devices were operating in enhancement mode ($V_{th} < 0$).

The electrical performance of the printed IZO TFTs was also studied. Figure S2 (in the ESM) shows the histograms of normalized on-current (Fig. S2(a)), current on/off ratio (Fig. S2(b)) and field-effect mobility (Fig. S2(c)) of 20 IZO devices. It is found that most IZO TFTs showed I_{on} of 0.6–5.2 μA for a V_G of 10 V and V_D of 1 V, I_{on}/I_{off} of 10^4–10^6, mobility of 1.0–14.1 $cm^2/(V \cdot s)$

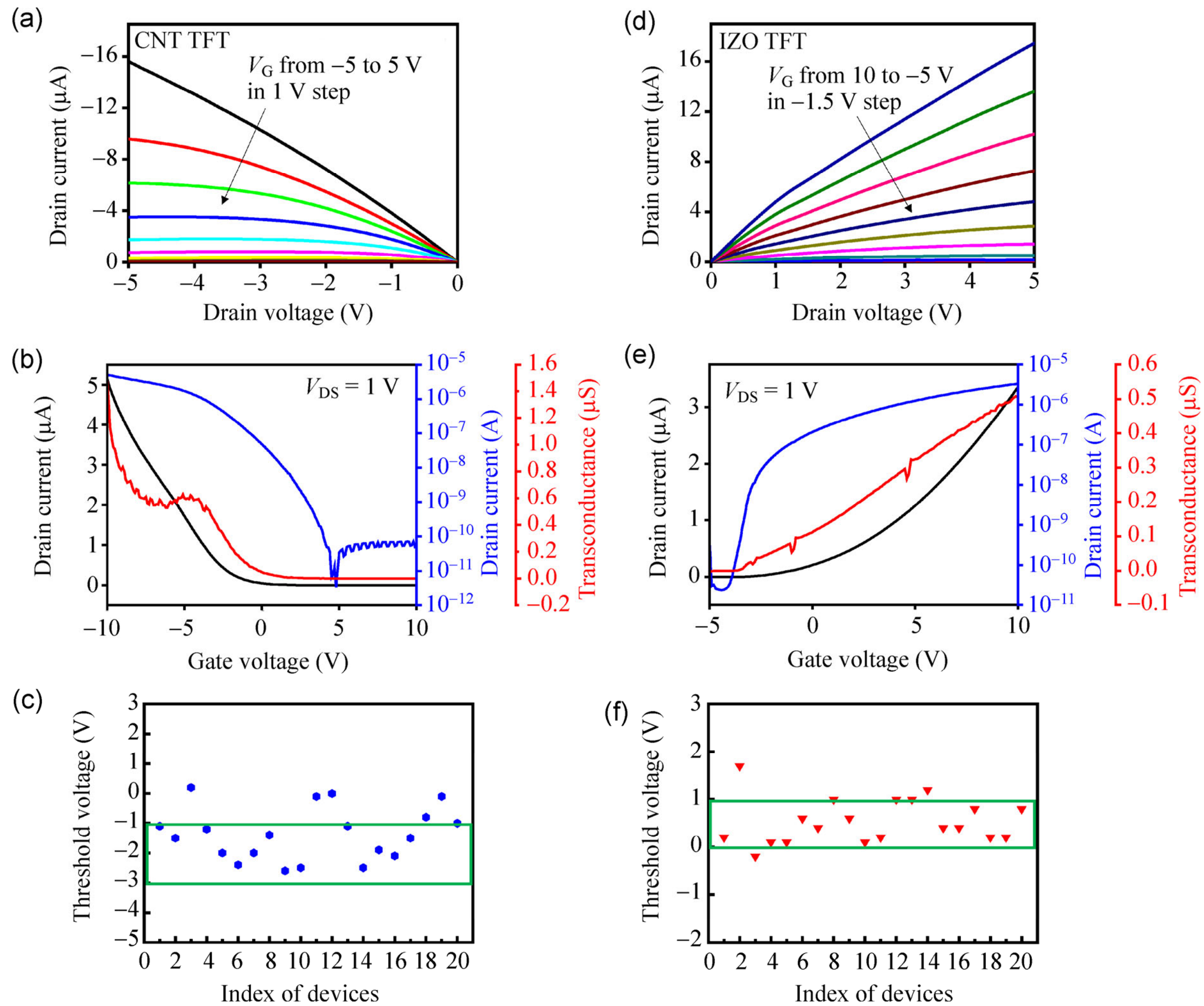

Figure 2 Characterization of printed back-gated p-type CNT TFTs and n-type IZO TFTs. (a) I_D–V_D characteristics of a representative CNT TFT (L = 100 μm, W = 500 μm). (b) I_D–V_G characteristics (black for linear scale; blue for logarithm scale) and g_m–V_G characteristics (red) of the same CNT TFT measured at V_D = 1 V. (c) Statistical analysis of the V_{th} distribution of 20 CNT TFTs. (d) I_D–V_D characteristics of a representative IZO TFT (L = 100 μm, W = 100 μm). (e) I_D–V_G characteristics (black for linear scale; blue for log scale) and g_m–V_G characteristics (red) of the same IZO TFT measured at V_D = 1 V. (f) Statistical analysis of V_{th} distribution of 20 IZO TFTs.

and V_{th} of 0–1 V, which are comparable with those in the literature for printed IZO [24, 25]. Figure 2(d) shows the I_D–V_D family curves of one representative IZO device with L = 100 μm and W = 100 μm. In Fig. 2(d), one can observe a saturation behavior as V_D becomes more positive. Figure 2(e) exhibits the transfer characteristics of the same IZO device on both linear (black curve) and logarithmic (blue curve) scales, and the plot of g_m versus V_G (red curve), from which one can extract values for this IZO device of I_{on} of 3.3 μA, V_{th} of 0.2 V, I_{on}/I_{off} of 1 × 10^5, peak g_m of 0.5 μS and mobility of 7.36 cm^2/(V·s). The V_{th} values of IZO TFTs were also collected and studied. The statistical results based on 20 inkjet printed back-gated IZO TFTs shown in Fig. 2(f) indicate that most IZO devices had V_{th} between 0 and 1.0 V, and were operating in enhancement mode (V_{th} > 0).

The outstanding benefits of a complementary circuit make it the preferred choice over many other configurations for the inverters presented in this work. We emphasize that it is significant to make sure that both p-type and n-type composites are operating in enhancement modes. Therefore, a study on the V_{th} tuning of both types of transistors was conducted. Here we demonstrate first the effects of different metal electrodes on V_{th} of the p-type devices. Besides the Ti/Au details given previously, Ti/Pd (1 nm/50 nm) was also used to fabricate S/D electrodes of printed

CNT TFTs. The majority of CNT devices with these Ti/Pd electrodes show I_{on} of 0.5–9 μA, I_{on}/I_{off} of 10^3–10^6, mobility of 0.50–2.39 cm^2/(V·s), and V_{th} of 1.0–3.0 V. Histograms of normalized on-current, current on/off ratio and field-effect mobility of 20 CNT devices are exhibited in Figs. S1(d)–S1(f), respectively (in the ESM). The normalized on-current and current on/off ratio, and mobility of these 20 CNT devices with Ti/Pd S/D contacts are comparable with ones with Ti/Au. The electrical characteristics of one of these devices (L = 100 μm, W = 500 μm) are shown in Figs. 3(a) and 3(b). The I_D–V_D family curves in Fig. 3(a) demonstrate a saturation behavior as V_D becomes more negative while the I_D–V_G family characteristics in Fig. 3(b) were investigated under V_D swept from 0.2 to 1 V in 0.2 V steps. In Fig. 3(b), I_{on} is apparently 2.45 μA when V_G is –10 V and V_D is 1 V, V_{th} is 1.2 V, and I_{on}/I_{off} is 1×10^5. The maximum g_m of this device was found to be 0.32 μS; subsequently, the mobility was calculated to be 1.38 cm^2/(V·s). In addition, Fig. 3(c) shows the statistics obtained from the V_{th} of 20 CNT TFTs with Ti/Pd as S/D metal contacts. Most of the devices have V_{th} of 1–3 V, indicating that the majority were operating in depletion mode (V_{th} > 0), unlike those with Ti/Au metal contacts (shown in Fig. 2(c)). It is concluded that Ti/Pd electrodes caused a right shift of the V_{th} of CNT TFTs relatively to that of Ti/Au electrodes. The reasons why the TFTs with Ti/Pd electrodes exhibit more positive V_{th} are: (1) The conduction of holes between the electrode and the CNT channel is dictated by the alignment between the Fermi energy level of the metal and the valence band of the CNT. The work function of Pd is around 5.1 eV, which is similar to the work function of CNT, and hence enables lower energy barrier between the metal electrode and the CNT. This results in a lower energy being required to lower the barrier for carrier conduction, and hence shifts the V_{th} to the right [32]. Therefore, Ti/Au S/D contacts are preferred in this work because CNT TFTs with Ti/Au metal contacts showed more negative V_{th}, which ensured the preferred enhancement mode (V_{th} < 0) p-type CNT TFTs for application in complementary circuits.

Likewise, the relationship between V_{th} of the n-type device with In-to-Zn molar ratio, which also affects the I_{on}/I_{off} and mobility of the devices, was investigated.

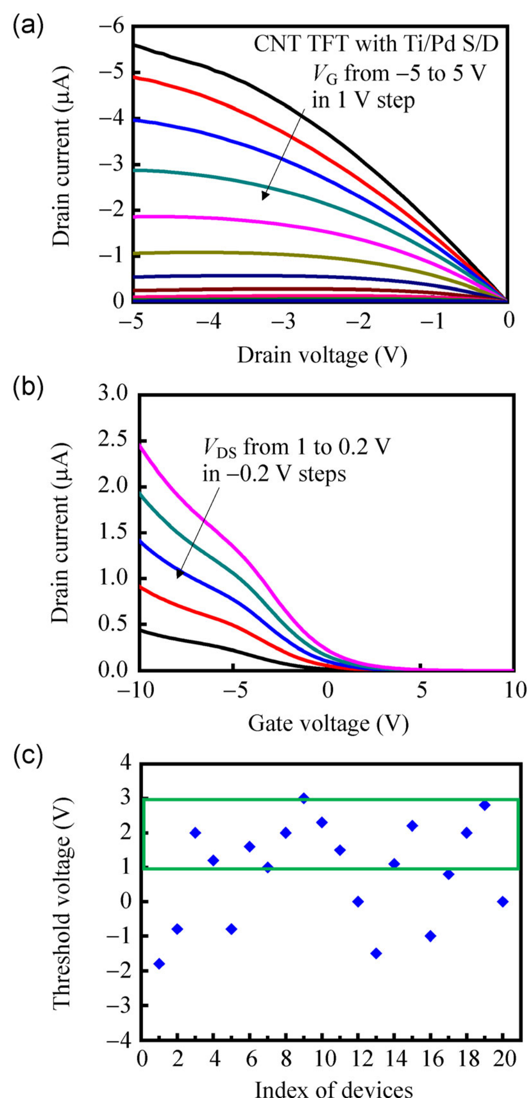

Figure 3 Characterization of printed CNT TFT with Ti/Pd (1 nm/50 nm) as S/D electrodes. (a) I_D–V_D characteristics of a representative CNT TFT (L = 100 μm, W = 500 μm). (b) I_D–V_G characteristics of the same CNT device. (c) Statistical analysis of V_{th} distribution of 20 printed CNT TFTs with Ti/Pd as S/D electrodes.

Figure 4(a) shows the transfer characteristics of the printed IZO devices with In:Zn ratios of 1:1, 2:1 and 3:1 represented by blue, red and black curves, respectively. Higher In:Zn ratios result in higher mobility and I_{on}, lower I_{on}/I_{off} and V_{th} apparently shifting to the left, which are consistent with previously published work [24]. As the amount of In was increased two- and threefold, the carrier mobility rose dramatically from 1.11 to 7.36 cm^2/(V·s) and to as high as 31.74 cm^2/(V·s) while I_{on} (at V_{DS} = 1 V and V_G = 10 V) increased correspondingly from 0.49 to 3.3 and 4.1 μA.

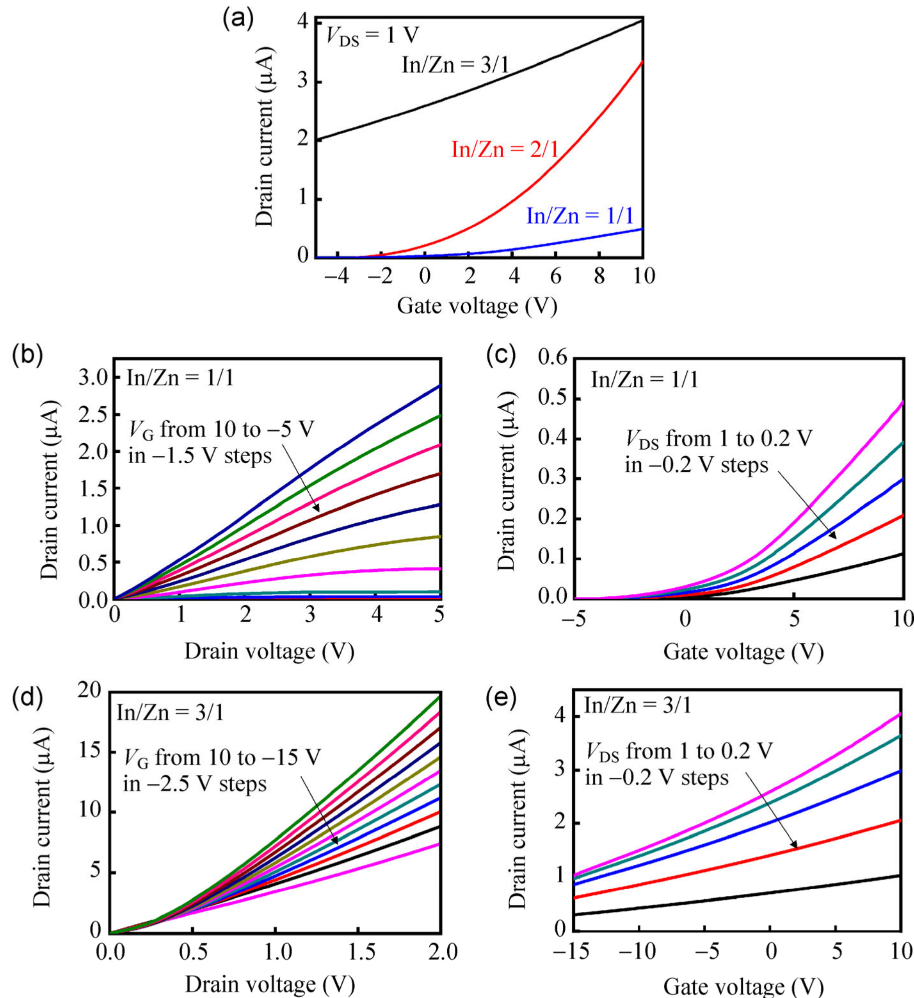

Figure 4 Characterization of printed IZO TFTs with various In:Zn ratio. (a) I_D–V_G characteristics of IZO TFTs with different In:Zn ratios including In:Zn = 1:1 (blue), In:Zn = 2:1 (red) and In:Zn = 3:1 (black), measured at V_D = 1 V. (b) I_D–V_D characteristics of a representative IZO TFT (L = 100 μm, W = 100 μm) with In:Zn = 1:1. (c) I_D–V_G characteristics of the same IZO TFT with In:Zn = 1:1. (d) I_D–V_D characteristics of a representative IZO TFT (L = 100 μm, W = 10 μm) with In:Zn = 3:1. (e) I_D–V_G characteristics of the same IZO TFT with In:Zn = 3:1.

Our devices with In:Zn = 1:1 and 2:1 had about the same values of I_{on}/I_{off} on average because I_{off} also increased along with I_{on}. However, when the In:Zn ratio was increased to 3:1, I_{off} increased much faster than I_{on}, resulting in poor I_{on}/I_{off}. As in Fig. 4(a), values of I_{on}/I_{off} of the 1:1 and 2:1 devices are about the same, ~10^5, whereas that of the 3:1 device drops abruptly to as low as 4. Moreover, the first two show positive V_{th} while the latter apparently has negative V_{th}, which indicates it is operating in depletion mode ($V_{th} < 0$). It can be concluded that IZO TFTs with In:Zn = 1:1 resulted in poor I_{on} while those with 3:1 had unacceptable I_{on}/I_{off} and depletion mode operation ($V_{th} < 0$). Therefore, it is clear that an In:Zn ratio of 2:1 offered the best overall performance, with the combination of desirable I_{on}, mobility, I_{on}/I_{off} and V_{th}. The IZO TFT with In:Zn = 2:1 shown in Fig. 2 has been discussed in the previous section of this paper. For comparison, Figs. 4(b) and 4(c) show I_D–V_D and I_D–V_G curves for a representative IZO device (L = 100 μm, W = 100 μm) with In:Zn = 1:1; this device shows I_{on} of 0.49 μA, V_{th} of 1 V, I_{on}/I_{off} of 10^5 and carrier mobility of 1.11 $cm^2/(V{\cdot}s)$. Figures 4(d) and 4(e) reveal that the IZO device with In:Zn = 3:1 cannot be fully depleted even at V_G = −15 V. As is evident from their high drain currents at relatively high negative V_G, most of the IZO devices with In:Zn = 3:1 operated in depletion mode ($V_{th} < 0$). According to previous studies

[24, 33], this phenomenon arises because indium oxide has the highest mobility among the oxides of In, Ga and Zn due to its large amount of oxygen vacancies, which contribute to high carrier concentrations. With such high carrier concentrations, it is challenging to bring down I_{off} so as to improve the poor I_{on}/I_{off}.

The capability of printing both CNT TFTs and IZO TFTs with desirable mobility, controlled V_{th} and good I_{on}/I_{off} enables us to construct high quality complementary digital circuits through the inkjet printing approach. As demonstrated, a printed complementary inverter was achieved based on thin films of CNT and IZO. The electrodes were Ti/Au (1 nm/50 nm) patterned by a photolithography process. The In:Zn ratio in the IZO precursor ink was selected to be 2:1, in accordance with the conclusion discussed above. Information about the static performance of the complementary circuit can be acquired from its voltage transfer (V_{out}–V_{in}) curves. In Fig. 5(a), the voltage transfer characteristics of one typical complementary inverter are illustrated at various V_{DD} ranging from 4 to 8 V in 1 V steps. Ideally, the output voltage switches from the “1” state (8 V) to the “0” state (0 V) in response to an input signal that is swept from the “0” state (0 V) towards the “1” state (8 V) and vice versa. As shown in Fig. 5(a), our inverter operates correctly. Its output levels are very close to the corresponding V_{DD} and the low output levels are approximately 0. Considering V_{DD} = 8 V as an example, the output swing reaches 7.97 V (99.6% of V_{DD}), which is much higher than the values for several previously published CNT-based inverters [34–39]. Ideally, one transistor of the complementary inverter is always off; however, during the switching state there will be a moment where both pull-up and pull-down circuits are on. As a result, there is a direct current flow from V_{DD} to ground causing a power dissipation called dynamic short-circuit power. This power dissipation is directly proportional to I_{Dmax}, which is the peak value of the drain current of the I_D–V_{in} curve. The I_D–V_{in} characteristic of the inverter displayed in Fig. 5(b) is as expected. When the inverter is operating in close proximity to either “0” or “1” states, its I_D is near zero, indicating infinitesimal power loss during this period. When switching, I_D dramatically rises and reaches a maximum before attenuating to nearly zero. The voltage gain of the same inverter measured at different V_{DD} ranging from 4 to 8 V in 1 V steps is shown in Fig. 5(c). At V_{DD} = 8 V, the inverter manifested a sharp turn at the switching threshold, where the gain is 16.9.

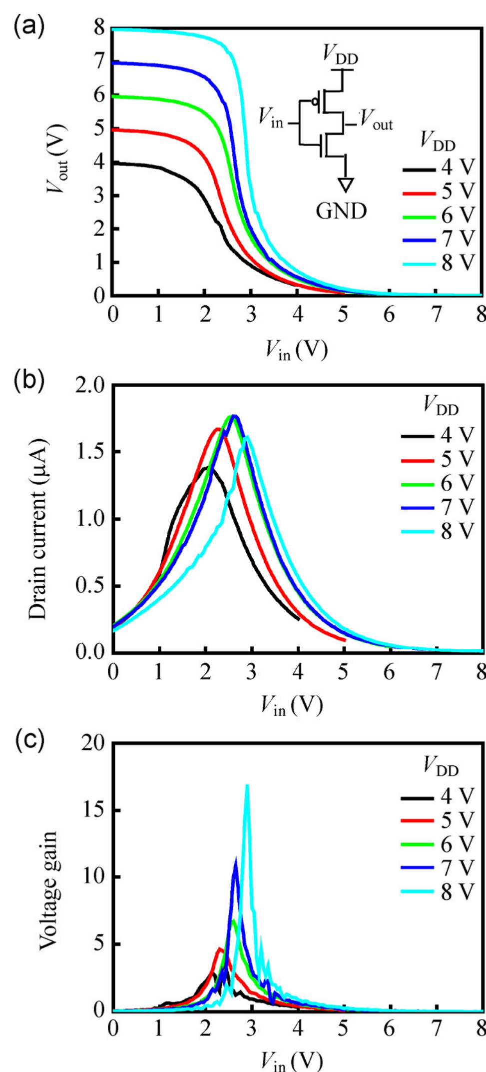

Figure 5 Characterization of a printed complementary inverter based on a p-type CNT TFT and n-type IZO TFT. (a) V_{out}–V_{in} characteristics of one representative inverter measured for V_{DD} = 4 (black), 5 (red), 6 (green), 7 (dark blue), and 8 V (light blue). (b) Switching current (I_D–V_{in}) curves of the same complementary inverter with V_{DD} = 4 (black), 5 (red), 6 (green), 7 (dark blue), and 8 V (light blue). (c) Gains of the same complementary inverter with V_{DD} = 4 (black), 5 (red), 6 (green), 7 (dark blue), and 8 V (light blue).

4 Conclusions

We have demonstrated desirable inkjet printed complementary transistors and inverters based on

CNT and IZO TFTs operated in enhancement modes. The CNT TFTs exhibited highest I_{on} of 9.5 μA, I_{on}/I_{off} of 10^4–10^6 and maximum mobility of 5 $cm^2/(V \cdot s)$, and the IZO TFTs attained a highest I_{on} of 5.2 μA, I_{on}/I_{off} of 10^4–10^6 and mobility as high as 14.1 $cm^2/(V \cdot s)$. In addition, experiments on alternative Ti/Pd electrodes showed that Ti/Pd metal contacts shifted the V_{th} of CNT TFTs to the positive side compared to devices with Ti/Au. Therefore, the Ti/Au electrodes were preferred for this work since they enabled the CNT devices to operate in enhancement mode. Moreover, IZO TFTs with various In:Zn ratios, namely 1:1, 2:1 and 3:1, were investigated, and the ratio of 2:1 gave the optimum combination of I_{on}, I_{on}/I_{off}, mobility and enhancement mode operation ($V_{th} > 0$). It is therefore the optimized composition of the IZO precursor solution. Finally, a complementary inverter was fabricated by sequentially printing IZO and CNT solutions as the active materials onto the same Si/SiO_2 substrate with pre-patterned Ti/Au electrodes. A maximum output swing of 99.6% of V_{DD} and voltage gain of 16.9 (with V_{DD} = 8 V) of the inverter were achieved. These results demonstrate that CNT and IZO are outstanding materials for p-type and n-type transistors, while inkjet printing technology allows the two types of materials to be patterned on the same substrate to form a complementary circuit through a simple, reproducible and low cost approach. Our work has paved the way for future research where printed complementary circuits with more sophisticated logic and even superior performance can be expected.

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Electronic Supplementary Material: Supplementary material (additional information about the statistical analysis of the performance of both CNT TFTs and IZO TFTs e.g. histograms of normalized on-current, current on/off ratio and field-effect mobility of both CNT devices and IZO devices) is available in the online version of this article at http://dx.doi.org/10.1007/s12274-014-0596-7.

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