

Reliability tests and improvements for Sc-contacted n-type carbon nanotube transistors

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ABSTRACT

Scandium (Sc) contacted n-type carbon nanotube (CNT) field-effect transistors (FETs) with back and top-gate structure have been fabricated, and their stability in air were investigated. It was shown that oxygen and water molecules may affect both the nanotube channel and Sc/nanotube contacts, leading to deteriorated contact quality and device performance. These negative effects associated with the instability of n-type carbon nanotube FETs can be eliminated through passivating the CNT devices by a thin layer of atomic-layer-deposition grown Al₂O₃ insulator. After passivation, the n-type carbon nanotube FETs are shown to exhibit excellent atmosphere stability even after being tested and exposed to air for over 146 days, and then much smoother output characteristics and reduced gate voltage hysteresis from 1 to 0.1 V were demonstrated when compared with devices without passivation. Lasting power-on tests were also performed on the passivated CNT FETs under large gate stress and high drain current in air for at least 10 h, revealing null device degradation and sometimes even improved performance. These results promise that passivated CNT devices are reliable in air and may be used in practical applications.

1 Introduction

As a competitive candidate for post-silicon nano-electronics, carbon nanotube (CNT) electronics has been studied for over 15 yr [1–3]. In particular CNT based high performance field-effect transistors (FETs) and their integrated circuits (ICs) have been the subject of intensive investigations and have made impressive progress in recent years [4]. Both p-type [5–7] and

n-type [8–10] CNT FETs have been pushed to their performance limit through optimization in both device structure and materials [6, 7, 9, 10], and various kinds of logic and arithmetic circuits [11–18], including full adder/subtractor [16–18], have been realized. Mainly benefiting from the dimensional and material advantages of CNTs, CNT FETs were predicted and proved to outperform FETs based on conventional bulk semiconductors [6, 9, 19, 20]. Among relevant

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electrical properties of CNTs, the ultra-thin body enables the device channel to be easily controlled by the field from the gate electrode, which in turn ensures that the sub-10 nm CNT FETs retain excellent device characteristics without suffering short channel effects [20, 21]. Such ultra-thin bodies also make CNT devices, especially FETs built on individual CNTs, be ultra-sensitive to their environment, leading to obvious current fluctuations in device properties [22–24]. It is thus highly desirable to know to what extent these fluctuations can be eliminated and how reliable the device can be. While some obvious phenomena related to device instability have been widely observed, in particular performance degradation in air, and increased hysteresis in transfer characteristics and current fluctuations [22–25], it is still not clear whether these instabilities could be eliminated. Very recently, stability in back-gated CNT FETs was investigated and it was shown that it may be improved through simple passivation [26–28], but for the more important top-gated FET geometry the problems have hardly been investigated. From a practical point of view, it is extremely important to know whether CNT FETs could continue to work for a long period of time under large current, which is likely to occur in practical applications. To develop CNT FET-based ICs, ways to determine and improve the stability and reliability of CNT FETs are urgently needed.

Comparing with p-type CNT FETs, the stability of n-type CNT FETs is an issue of even greater concern [29–32]. This is because contact electrodes made of metals with low work functions, such as Sc or Y, are more active and likely to be subject to chemical reactions in air. Although some methods have been tried to passivate n-type back-gated CNT FETs [33], for example depositing an Al film to isolate the contact electrode from the air and covering the channel by a layer of hexamethyldisilazane (HMDS), the current fluctuation was still obvious. In this paper we will explore the stability of Sc-contacted n-type CNT FETs through monitoring the time-evolution of several key performance parameters of the devices. We found that the performance of Sc-contacted n-type CNT FETs does degrade with time in air, which may be attributed to molecules such as O₂ or H₂O in air. In principle these molecules could affect both the Sc/CNT contacts and

CNT channel, but the stability of the CNT FETs can be significantly improved by suitable passivation, e.g., by covering the devices with a thin layer of Al₂O₃. After passivation, the reliability of CNT FETs is shown to have been significantly improved, exhibiting hardly any degradation in air for a long period of time, accompanied by a significantly reduced gate hysteresis and almost no current fluctuations. Furthermore, suitably passivated n-type FETs built on individual CNT are shown to be able to withstand large continuous currents of more than 10 μA for over 10 h, which is unlikely to occur in real complementary metal–oxide–semiconductor (CMOS) circuits.

2 Experimental and results

2.1 Air stability of back-gated n-type CNT FETs

We first consider the stability of back-gated n-type CNT FETs, since in this device geometry both contacts and channel are exposed to air, presenting the worst case for investigating the stability and various air-induced effects of CNT FETs. CNT FETs were fabricated directly on individual chemical vapor deposition (CVD) grown CNTs on Si substrates which were covered with 500 nm thermally grown SiO₂. For the back-gated FET, a Sc metallic layer of 60 nm was used as the source/drain electrodes, and n+ doped Si substrate used as back-gate. Such n-type CNT FETs were measured successively in vacuum and in air for comparison. Figure 1(a) shows that the Sc-contacted CNT FETs are excellent n-type devices regardless of whether the measurements were carried out in vacuum or in air, since in both cases electrons can be injected into the conduction band of the CNT with effectively small Schottky barrier at small bias, i.e., typically smaller than 100 mV [8]. Compared to device characteristics measured in vacuum, those measured in air exhibit two remarkable differences as shown in Figs. 1(a)–1(c). First, the threshold voltage V_{th} is shifted by up to 8 V toward the positive direction on exposure to air, suggesting the well-known p-doping effect of CNT channels which is induced by adsorbed oxygen or water molecules in air [23, 24]. Second, the channel resistance of the device is markedly increased, since the presence of adsorbed oxygen and water molecules

on the metal/CNT interface raises the workfunction of the metal and increases the barrier for electron injection through the interface [34]. As a result, peak transconductance of the CNT FET, i.e., the peak value of $\partial I_{ds}/\partial V_{BG}$ decreases from $0.86 \mu\text{S}$ in vacuum to $0.53 \mu\text{S}$ in air under $V_{ds} = 1.0 \text{ V}$. The increase in channel resistance can also be seen by comparing the output characteristics measured in vacuum and in air. Both current–voltage (I_{ds} – V_{ds}) characteristics show linear relation at low bias (Figs. 1(b) and 1(c)), but the slopes of these I – V curves become much smaller when measured in vacuum than when measured in air (Fig. 1(c)). Furthermore the on-state current of the device at large bias is seriously suppressed to a low level when measured in air since effective p-doping of oxygen or water molecules depletes electron density in the n-type channel of the device. Another remarkable characteristic for CNT FETs in air is that large fluctuations occur in the measured I_{ds} – V_{ds} curves, especially in the on-state current curves, while the current curves are smoother for those measured in vacuum (Fig. 1(b)).

At large current, adsorbed oxygen or water molecules on CNT channels may be randomly desorbed under large field, and meanwhile the adsorption processes continually occur in air. The large current fluctuations in air have been observed in almost all CNT FETs [22–28] and were mainly attributed to the random desorption and adsorption of oxygen or water molecules in air. It should be noted that the effect from oxygen or water in air degrades the performance of n-type CNT FETs, while it affects the performance of p-type CNT FETs to a much lesser extent.

Adsorbed molecules on CNT channels of moderate diameter generally do not directly induce chemical reactions, and thus performance degradation is mostly reversible for CNT FETs when exposed to air for a short period of time. Subsequent measurements in vacuum after being exposed to air demonstrate that the performance of n-type CNT FETs may recover to the original level after removal of adsorbed molecules in vacuum. Besides reversible performance degradation in air, Sc-contacted n-type CNT FETs also suffer from

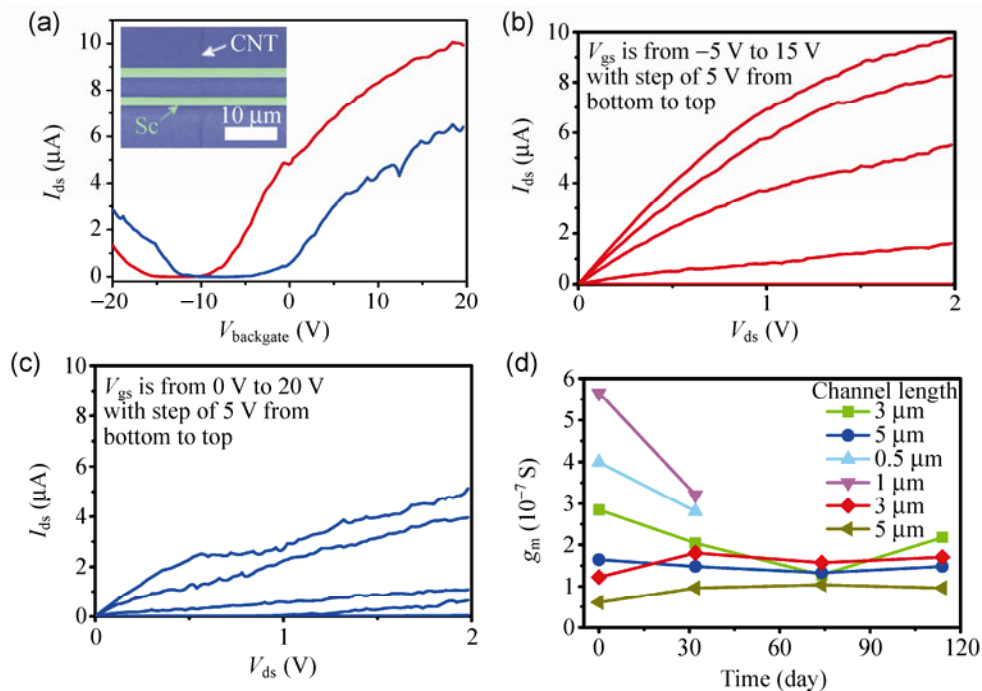


Figure 1 Stability tests of Sc-contacted n-type back-gated CNT FETs. (a) Transfer characteristics measured in vacuum (red) and in air (blue) of a CNT FET with a channel length of $5 \mu\text{m}$ under $V_{ds} = 1.0 \text{ V}$. Inset: SEM image of the device. Output characteristics measured (b) in vacuum and (c) in air. (d) Time-dependent peak transconductance g_m (at $V_{ds} = 0.1 \text{ V}$ and $V_{gs} - V_{th} = 10 \text{ V}$) evolution of six devices with different channel lengths. These FETs were exposed to air without any protection, and measured in vacuum on the planned days, i.e., 0, 30, 75, and 114 days after being fabricated.

time-dependent irreversible degeneration once being exposed to air for a long period of time without any protection. Six n-type devices with different channel lengths were tested for 114 days after being fabricated and exposed to air, and their performance evolution was followed and the results are shown in Fig. 1(d). All measurements were carried out in vacuum to exclude effects due to molecular absorptions during the measurements, and the device performance parameter g_m (transconductance) is chosen here as the key metric for evaluating on-state performance of CNT FETs. It can be seen from Fig. 1(d) that all six devices survived at the first 30 days tests after being exposed to air. However, performance degeneration occurred to various degrees. It is obvious that the devices with shorter channels suffered more serious performance degeneration. Such irreversible performance degeneration may be attributed to the oxidation of Sc contacts at the edges close to the CNT channel. The oxidation may reduce the effective size of the contacts and thus increases the effective length of CNT channel between S/D contacts, leading to larger transconductance decreases for devices with shorter channels than those with longer channels. For long channel devices, e.g., for those with a channel length larger than $3\ \mu\text{m}$, the performance was fairly stable. Two devices with the shortest channel were found to fail at the test after 30 days, owing to the unexpected electrostatic breakdown during measurements being carried out two months later, while the other four devices survived after being exposed to air for about 120 days and the device performance remained basically in a steady state after being tested for more than 60 days. This is because native Sc oxide layers developed completely after 30 days which prevented further penetration of such molecules as oxygen and water. The oxidation process typically develops rapidly at first and then to a stable level, in accordance with our time-dependent measurements as shown in Fig. 1(d).

2.2 Air stability of top-gated n-type CNT FETs

Compared with back-gated CNT FETs, top-gated FETs possess a more suitable device geometry for integrated circuits owing to their high performance and flexible controllability. Top-gated n-type CNT FETs with gate

stack made of 12 nm HfO_2 and 10 nm Pd were fabricated using the well-developed self-aligned gate structure on top of the previously discussed back-gated CNT FETs [9, 14]. Figure S1 in the Electronic Supplementary Material (ESM) displays the details of self-aligned structure with cross-section and 3D schemes. Figure 2(a) is a scanning electron microscopic (SEM) image showing a typical top-gated CNT. Both transfer and output characteristics of the top-gated CNT FETs were measured in vacuum and in air (Figs. 2(b)–2(d)). These top-gate devices show excellent n-type performance in vacuum, with typical transfer (see the solid blue curves, Fig. 2(b)) and output (Fig. 2(c)) characteristics measured from a device with a gate length L_g of about $3\ \mu\text{m}$. Compared with the back-gated FET (Fig. 1), peak transconductance of the top-gated FET is significantly improved and reaches up to $10\ \mu\text{S}$ owing to the high efficiency of the top gate, while the device still retains a large current ON/OFF ratio of up to 10^5 . The same device was measured in air subsequently, and its transfer and output characteristics are respectively shown in Fig. 2(b) (the dashed blue curves) and Fig. 2(d). Obviously exposure to air not only results in a large threshold voltage shift of about 0.5 V toward positive direction (Fig. 2(b)), but also leads to large performance degeneration via e.g., deteriorated contacts or large resistances, suppressed on-state current and large current fluctuations (Fig. 2(d)). These performance changes observed in the top-gated CNT FET in air are similar to those observed in the back-gated CNT FET (Fig. 1), indicating that oxygen or/and water molecules in air can penetrate the gate stack and reach the channel and CNT/Sc contact interface as shown in the inset of Fig. 2(d). Comparing measurement results in vacuum and in air reveals that the top-gated CNT FET is still sensitive to the environment, indicating that the gate stack consisting of 12 nm HfO_2 and 10 nm Pd is still not sufficient to isolate the device from air effectively. To isolate n-type CNT FETs from air and improve their stability, an additional passivation layer is necessary to cover the whole device. In fact passivation is a popular and widely used technology in the conventional semiconducting industry for the protection of devices and improvement of device performance.

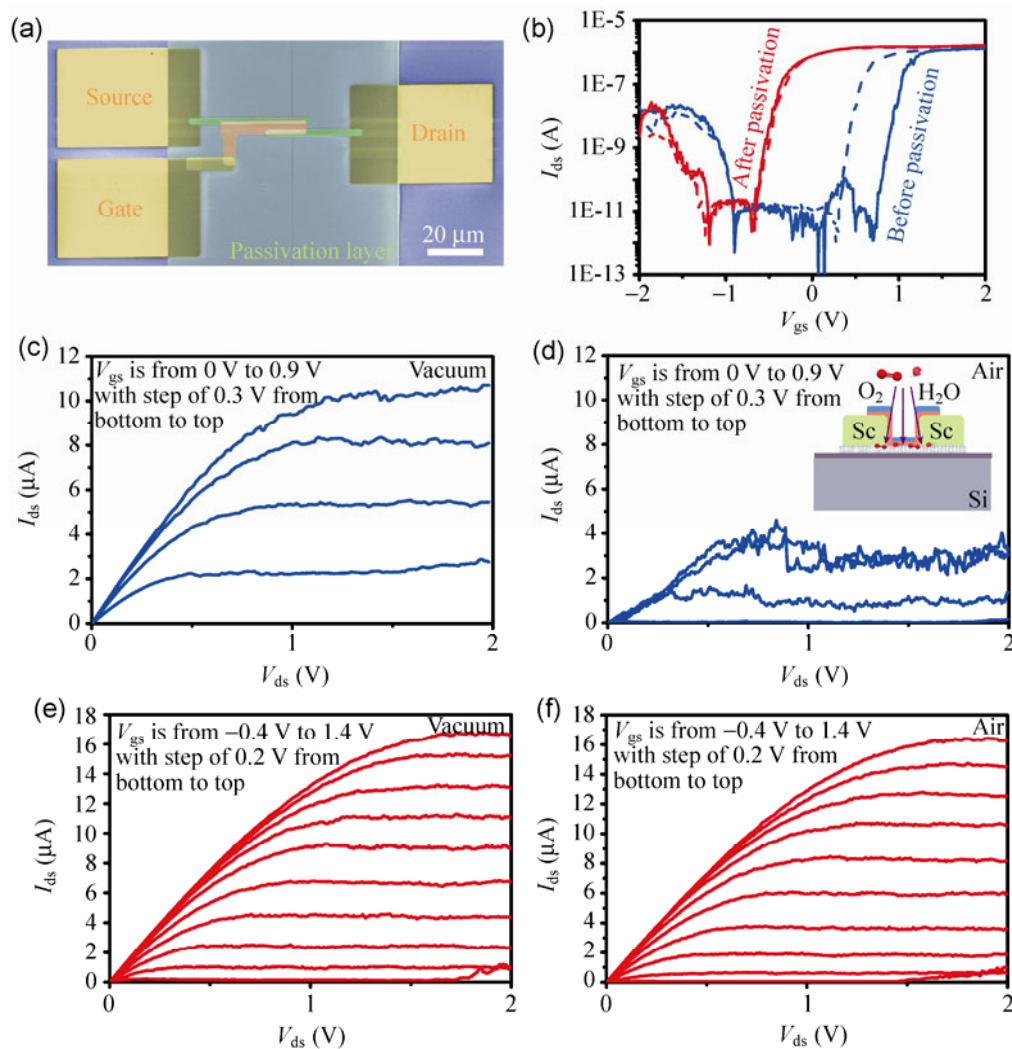


Figure 2 Stability test of a top-gated n-type CNT FETs before and after passivation. The diameter of the CNT is about 2.0 nm as measured by atomic force microscopy (AFM). (a) SEM image of the device with gate length of 3 μm. (b) Transfer characteristics of the FET before (blue)/after (red) passivation measured in vacuum (dashed line)/air (solid line) under $V_{ds} = 0.1$ V. (c) Output characteristics of the CNT FET before passivation in vacuum and (d) in air. Inset indicates how the oxygen or water molecules affect the CNT channel and contacts, while Fig. S1 (in the ESM) provides more detailed illustrations of device structures. Output characteristics of the CNT FET after passivation (e) in vacuum and (f) in air.

2.3 Reliability of top-gated n-type CNT FETs after being passivated

An aluminum oxide (Al_2O_3) layer with a thickness of 20 nm was grown via atomic layer deposition (ALD) to cover the whole CNT FET and protect the device. Al_2O_3 was chosen because its compactness is high enough to prevent the oxide layer from being penetrated by oxygen or water molecules, and ALD grown Al_2O_3 has proved to be an excellent passivation layer for p-type back-gated CNT FETs with obvious suppression of

both low-frequency noise and gate voltage hysteresis [28]. After passivation, the n-type top-gate CNT FET shows high-performance both in vacuum and air; its transfer and output characteristics are shown in Figs. 2(b), 2(e), and 2(f). The most striking features shown in these figures are the significantly improved signal to noise ratio, the significantly increased on-state current, and the obviously improved stability. In particular, the transfer characteristics measured in vacuum and in air are hardly distinguishable (the green curves in Fig. 2(b)), showing that the air-induced

threshold voltage drift is almost completely eliminated by passivation. This in turn means that the CNT FET has been effectively isolated from air, in particular from oxygen and water molecules. The peak field-effect mobility, which was estimated using a simple diffusive model [9], remains at a high level of about $4,200 \text{ cm}^2/\text{V}\cdot\text{s}$ after passivation compared to the original value of $4,500 \text{ cm}^2/\text{V}\cdot\text{s}$ before passivation, indicating that passivation introduces few additional scattering centers into the device. It should be noted that the extracted mobility is underestimated since the effect from contact resistances is not excluded. Output characteristics of the passivated CNT FET also show no obvious difference between those measured in vacuum (Fig. 2(e)) and those measured in air (Fig. 2(f)). Furthermore, after passivation, the n-type FET presents larger saturation current and much smoother output characteristics than before passivation, especially when compared to the device measured in air.

Another important feature that should be noted in the passivated FET is that an Al_2O_3 passivation layer results in a threshold voltage shift of more than 1.0 V toward negative gate voltage, leading to a large negative threshold voltage of about -0.4 V . The negative threshold voltage shift suggests that there exists a large amount of trapped positive charges in the Al_2O_3 film which is likely to be associated with O vacancies owing to the low temperature ALD growth process. It is well known that increased growth temperature may help to improve the quality of ALD-grown Al_2O_3 film which in turn may reduce the number of trapped positive charges [35]. An enhanced mode n-type CNT FET, i.e., with a positive threshold voltage, is expected via optimizing the growth conditions of Al_2O_3 in the future.

Hysteresis in transfer characteristics, an often observed phenomenon in CNT FETs, is another major instability for CNT FET [22, 27, 36, 37]. Although the mechanisms [22, 36] and optimizing methods [27, 37] of hysteresis in bottom CNT FETs have been explored, exploration in top-gate CNT FETs has not been reported. The transfer characteristics of another n-type CNT FET were measured before and after passivation and are shown in Fig. 3(a), where the top gate voltage V_{gs} was swept from -2 V to 2 V at a rate of 0.05 V/s and then backwards at the same rate. The device without

passivation presents a significant gate hysteresis as large as 0.7 V when measured in air between forward and backward sweeps of V_{gs} . It is well known that the gate voltage hysteresis results mainly from charge injection from nanotubes into nearby charge traps under a large gate voltage [22, 27]. Charge traps around CNT channels usually originate from two sources. One source is from the environment, e.g., adsorbed water molecules on the gate insulator around the CNT channel [22]. The other source is the device itself, i.e., charge traps on the oxide/CNT interface or in the HfO_2 gate insulator [38]. It is remarkable that the gate hysteresis is suppressed down to 0.1 V with the same gate swept range between -2 V to 2 V after the CNT device was passivated. Such a significant suppression of gate voltage hysteresis by passivation might be attributed to the fact that water molecules are effectively blocked by the Al_2O_3 layer which covered the entire device. For the CNT FET without passivation, when exposed to air, it can be estimated that the main charge traps (about 6/7) are due to adsorbed water molecules, and very few charge traps are from the device itself, leading only to a small (about 0.1 V) gate hysteresis. Of course the residual small gate voltage hysteresis after passivation can be further eliminated through optimizing the fabrication process, especially through improving the quality of the gate insulator and cleaning the interface between the CNT and oxide [9, 39]. Figure 3(b) shows the detailed gate voltage hysteresis evolution of a typical n-type CNT FET before and after passivation. Before passivation, the n-type FET presents a large gate voltage hysteresis of about 0.54 V . After passivation, hysteresis of the same device is suppressed to a small value, which typically remains less than 0.1 V even after being exposed to air for 146 days. Another six passivated devices were also measured in air, and all these devices exhibited small gate voltage hysteresis ranging from 0.08 to 0.28 V . These experimental results suggest that an Al_2O_3 passivation layer can effectively suppress the oxygen and/or water molecule induced gate voltage hysteresis over a very long period of time.

To further test the stability of the passivated CNT FETs in air, three devices were placed in air and measured on planned dates, which continued for 146 days. The peak transconductance of these devices

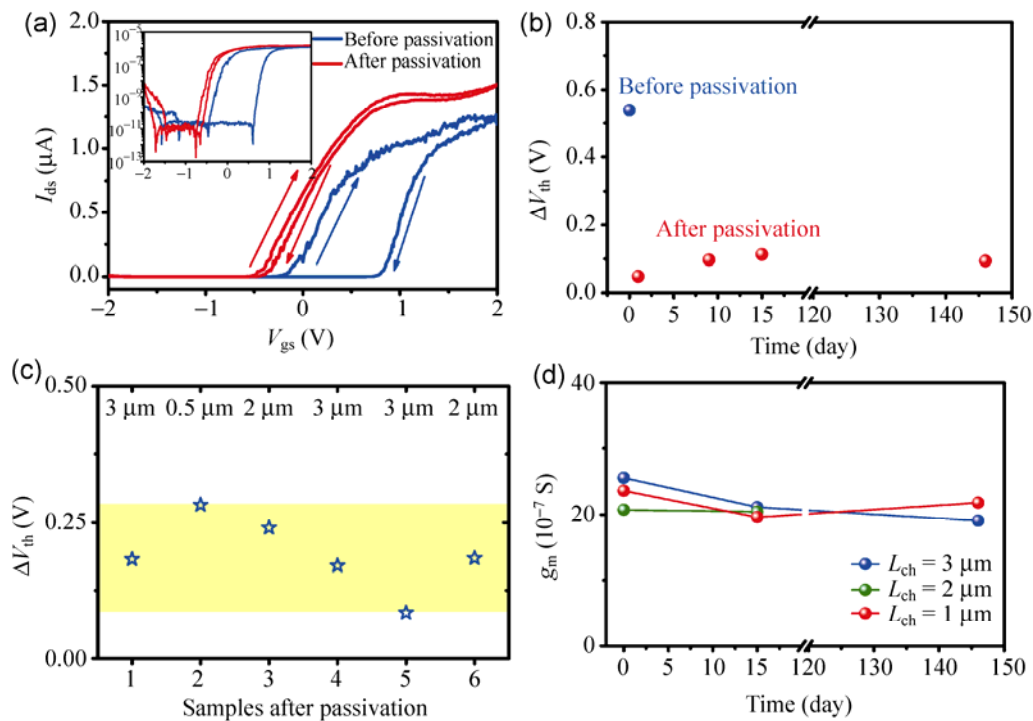


Figure 3 Effect of passivation on threshold voltage hysteresis and peak transconductance g_m . (a) Transfer characteristics (under $V_{ds} = 0.5$ V) of a top-gated n-type CNT FET measured in air before and after passivation by a layer of ALD-grown Al_2O_3 . Inset shows the same transfer characteristics in log scale. (b) Time-dependent gate voltage hysteresis of the device. The FET was exposed to air without any protection, and measured in vacuum. (c) Statistical gate voltage hysteresis distribution of six devices after passivation. (d) Time-dependent peak transconductance g_m (at $V_{ds} = 0.1$ V) of three passivated top-gated CNT FETs with different channel lengths. These FETs were exposed to air without any protection, and measured in vacuum on the planned days.

(at $V_{ds} = 0.1$ V) was shown to be weakly dependent on time (Fig. 3(d)). Although one device failed during the test owing to electrostatic breakdown at the 146th day, the other two devices survived without obvious performance degradation even after being exposed to air for 146 days. We thus conclude that the performance of Sc-contacted n-type CNT FETs remains stable in air after being suitably passivated.

In practical applications, electronic devices and ICs must work in air for a very long time, thus power-on tests for n-type CNT FET in air were carried out in order to evaluate its potential for practical applications. Figure 4 shows the results of power-on tests on a typical passivated n-type CNT FET in air with a large supply power. The device was biased with $V_{ds} = 1.0$ V and $V_{gs} = 1.0$ V in the first hour of the test. The drain current reached up to about 10 μA , and the power applied during the test on the CNT FET was 10 μW , which is equivalent to a power density of about

1,000 W/mm^2 when normalized by the area of the CNT channel of the device. The drain current of the device remained constant for the first hour, and the gate leakage current remained also roughly constant at less than 2 pA, demonstrating the good reliability of the gate dielectrics. At the beginning of the second hour of the test, the drain voltage was reversed to -1.0 V, while the bias applied on the gate remained at 1.0 V. The drain current I_{ds} increased to about 14 μA owing to the increased gate voltage relative to the CNT channel. At the beginning of the third hour of the test, the drain voltage was switched back to 1.0 V, and I_{ds} returned to about 10 μA . Figure 4(a) shows that the CNT FET can work in air for at least 3 h without obvious performance change. However, detailed comparison of the transfer characteristics of the same passivated n-type CNT FET before and after 3 h power-on test (Fig. 4(b)) shows that a small threshold voltage drift of about 0.2 V occurred toward negative

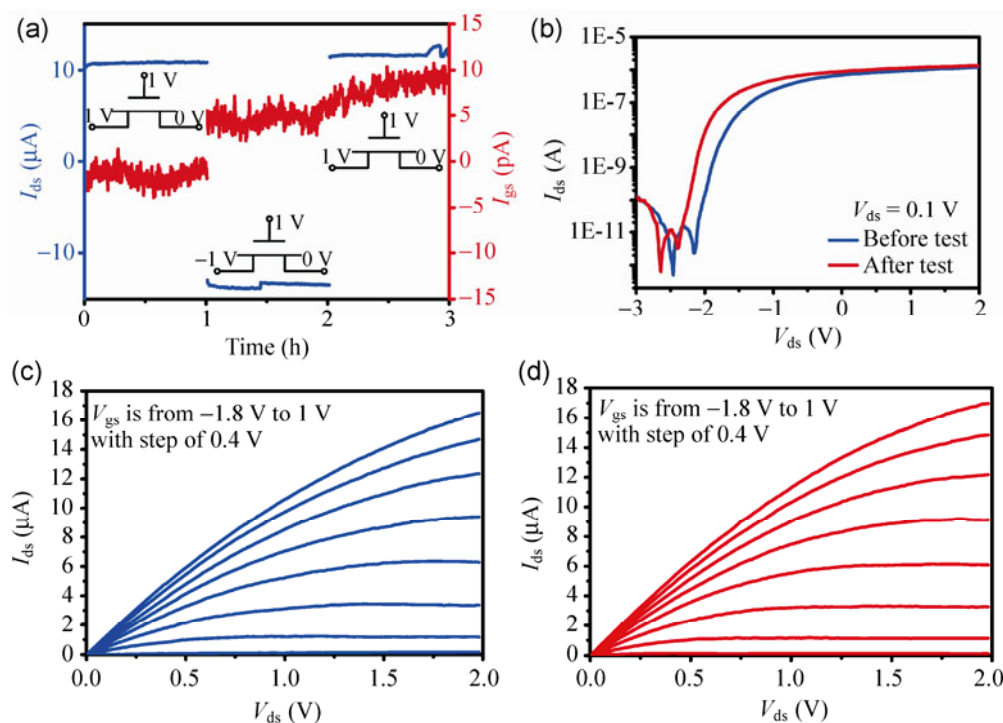


Figure 4 Power-on test of a top-gated n-type FET device with a $5 \mu\text{m}$ gate length and $45 \text{ nm Al}_2\text{O}_3$ passivation layer in air. (a) Time-dependent drain current (blue curve) and gate leakage current (red curve) during power-on test of the device with $V_{gs} = 1 \text{ V}$ and $V_{ds} = \pm 1 \text{ V}$. Inset: Bias conditions of the FET at different times. (b) Transfer characteristics of the device before (blue) and after (red) power-on test. (c) Output characteristics of the device before and (d) after 3 h power-on test. Before characteristics measurement (as for the results in (b) and (d)), the device was powered off for 20 min after being tested for 3 h.

direction after the power-on test. This power-on test induced threshold voltage drift results mainly from the gate insulator change under prolonged high-field (from the CNT into the dielectric) during the test, which is also manifested in the time-dependent gate leakage current as shown in Fig. 4(a). Further improvement of the growth conditions and thus the quality of HfO_2 insulator is expected to reduce or even remove such threshold voltage drift during long time power-on tests. Figures 4(c) and 4(d) compare the output characteristics of the passivated device before and after 3 h power-on test. Except for a small threshold voltage shift, there are no obvious difference between the two groups of curves, which are both much smoother and more stable than that observed in any other nanodevices.

Figures S2 and S3 (in the ESM) show the results for other passivated devices that were also measured with large gate bias and high drain current in air for an extended period of time (up to 10 h). These measurements revealed that most devices failed as a result

of gate insulator breakdown. These power-on tests demonstrate that n-type CNT FETs with an Al_2O_3 passivation layer may work in air with superb stability performance. Although minor performance changes may occur after extended power-on tests, CNT FETs are mostly reliable. The major failure comes from the effects of prolonged exposure to high-field destroying the HfO_2 insulator, but this situation could be improved by adopting better growth conditions thus giving better quality gate insulators. It should be noted that transistors in a power-on IC chip typically work alternately rather than continuously at full power for a long period of time. The tests discussed here thus present the worst case while in real application the time-average power density in the device should be much lower.

3 Conclusions

The reliability of Sc-contacted n-type CNT FETs has

been investigated. It was found that oxygen or water molecules may dope the CNT channel and increase the barrier for electron injection from Sc to CNT, thus n-type CNT FETs directly exposed to air suffer significantly lowered and unstable current as well as large threshold voltage shift and hysteresis. Top-gated CNT FETs show similar instability in air to back-gate FETs, suggesting that the gate stack used cannot prevent oxygen or water molecules from penetrating to the contacts and channel. When passivated with a layer of ALD-grown Al_2O_3 , CNT FETs are shown to be well isolated from air, and their stability and reliability are significantly improved. Furthermore, n-type CNT FETs with an Al_2O_3 passivation layer present smoother output characteristics and much smaller gate voltage hysteresis than those without passivation. Lasting power-on tests show that the passivated devices can work well under large bias and high current in air for a long period of time, which promises the possibility of practical applications of CNT FETs.

4 Methods

Heavily n-doped silicon wafers, covered with a 500 nm thermally grown SiO_2 layer, were used as substrates. Ultra-long carbon nanotubes were grown on Si wafers via copper catalytic CVD [40]. Source and drain contacts were patterned and formed via electron beam lithography (EBL), followed by evaporating a 60 nm Sc film via e-beam evaporation and a standard lift-off process. Semiconducting single-walled nanotubes were selected through standard field-effect measurements with an n⁺-doped substrate as back gate. For top-gated devices, gate windows were patterned via EBL, and a 12-nm (measured by an ellipsometer) HfO_2 film with a dielectric constant of approximately 15 (retrieved through C–V measurements) was grown by ALD at 90 °C, followed by deposition of a 10-nm Pd film by e-beam evaporation (EBE). A standard lift-off process was used to form a self-aligned HfO_2 /Pd gate stack to complete the fabrication of the n-type CNT FETs. Ti/Au pads with thickness of 5/45 nm were formed to connect S, D and Gate for probing through another EBL, EBE and lift-off process. An Al_2O_3 insulator layer with thickness of 20 nm or 45 nm was grown to cover CNT FETs as passivation layer through ALD at 90 °C.

Generally the fabricated devices were measured in vacuum at first and then measured in air. All electrical measurements were performed using Keithley 4200 Semiconductor Analyzer and at room temperature. Measurements in vacuum were carried using a Lakeshore TTP-4 probe station as soon as the pressure was reduced to 10^{-3} Torr.

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Electronic Supplementary Material: Supplementary material about power-on experimental details of another two devices, display that passivated devices with large gate bias and high drain current in air for an extended period of time (up to 10 h), is available in the online version of this article at <http://dx.doi.org/10.1007/s12274-013-0330-x>.

References

- [1] Tans, S. J.; Verschueren, A. R.; Dekker, C. Room-temperature transistor based on a single carbon nanotube. *Nature* **1998**, *393*, 49–52.
- [2] Martel, R.; Schmidt, T.; Shea, H. R.; Hertel, T.; Avouris, P. Single- and multi-wall carbon nanotube field-effect transistors. *Appl. Phys. Lett.* **1998**, *73*, 2447–2449.
- [3] Avouris, P.; Chen, Z.; Perebeinos, V. Carbon-based electronics. *Nat. Nanotechnol.* **2007**, *2*, 605–615.
- [4] Zhang, Z. Y.; Wang, S.; Peng, L. M. High-performance doping-free carbon-nanotube-based CMOS devices and integrated circuits. *Chin. Sci. Bull.* **2012**, 135–148.
- [5] Javey, A.; Guo, J.; Wang, Q.; Lundstrom, M.; Dai, H. J. Ballistic carbon nanotube field-effect transistors. *Nature* **2003**, *424*, 654–657.
- [6] Javey, A.; Guo, J.; Farmer, D. B.; Wang, Q.; Wang, D. W.; Gordon, R. G.; Lundstrom, M.; Dai, H. Carbon nanotube field-effect transistors with integrated Ohmic contacts and high- κ gate dielectrics. *Nano Lett.* **2004**, *4*, 447–450.
- [7] Javey, A.; Guo, J.; Farmer, D. B.; Wang, Q.; Yenilmez, E.; Gordon, R. G.; Lundstrom, M.; Dai, H. J. Self-aligned

- ballistic molecular transistors and electrically parallel nanotube arrays. *Nano Lett.* **2004**, *4*, 1319–1322.
- [8] Zhang, Z. Y.; Liang, X. L.; Wang, S.; Yao, K.; Hu, Y. F.; Zhu, Y. Z.; Chen, Q.; Zhou, W. W.; Li, Y.; Yao, Y. G. et al. Doping-free fabrication of carbon nanotube based ballistic CMOS devices and circuits. *Nano Lett.* **2007**, *7*, 3603–3607.
- [9] Zhang, Z. Y.; Wang, S.; Ding, L.; Liang, X. L.; Pei, T.; Shen, J.; Xu, H. L.; Chen, Q.; Cui, R. L.; Li, Y. et al. Self-aligned ballistic N-type single-walled carbon nanotube field-effect transistors with adjustable threshold voltage. *Nano Lett.* **2008**, *8*, 3696–3701.
- [10] Wang, Z. X.; Xu, H. L.; Zhang, Z. Y.; Wang, S.; Ding, L.; Zeng, Q. L.; Yang, L. J.; Pei, T.; Liang, X. L.; Gao, M. et al. Growth and performance of yttrium oxide as an ideal high- κ gate dielectric for carbon-based electronics. *Nano Lett.* **2010**, *10*, 2024–2030.
- [11] Javey, A.; Wang, Q.; Ural, A.; Li, Y. M.; Dai, H. J. Carbon nanotube transistor arrays for multistage complementary logic and ring oscillators. *Nano Lett.* **2002**, *2*, 929–932.
- [12] Derycke, V.; Martel, R.; Appenzeller, J.; Avouris, P. Carbon nanotube inter- and intramolecular logic gates. *Nano Lett.* **2001**, *1*, 453–456.
- [13] Bachtold, A.; Hadley, P.; Nakanishi, T.; Dekker, C. Logic circuits with carbon nanotube transistors. *Science* **2001**, *294*, 1317–1320.
- [14] Zhang, Z. Y.; Wang, S.; Wang, Z. X.; Ding, L.; Pei, T.; Hu, Z. D.; Liang, X. L.; Chen, Q.; Li, Y.; Peng, L. M. Almost perfectly symmetric SWCNT-based CMOS devices and scaling. *ACS Nano* **2009**, *3*, 3781–3787.
- [15] Chen, Z. H.; Appenzeller, J.; Lin, Y. M.; Sippel-Oakley, J.; Rinzler, A. G.; Tang, J. Y.; Wind, S. J.; Solomon, P. M.; Avouris, P. An integrated logic circuit assembled on a single carbon nanotube. *Science* **2006**, *311*, 1735–1735.
- [16] Ding, L.; Zhang, Z. Y.; Liang, S. B.; Pei, T.; Wang, S.; Li, Y.; Zhou, W. W.; Liu, J.; Peng, L. M. CMOS-based carbon nanotube pass-transistor logic integrated circuits. *Nat. Commun.* **2012**, *3*, 677–677.
- [17] Ding, L.; Zhang, Z. Y.; Pei, T.; Liang, S. B.; Wang, S.; Zhou, W. W.; Liu, J.; Peng, L. M. Carbon nanotube field-effect transistors for use as pass transistors in integrated logic gates and full subtractor circuits. *ACS Nano* **2012**, *6*, 4013–4019.
- [18] Ding, L.; Liang, S. B.; Pei, T.; Zhang, Z. Y.; Wang, S.; Zhou, W. W.; Liu, J.; Peng, L. M. Carbon nanotube based ultra-low voltage integrated circuits: Scaling down to 0.4 V. *Appl. Phys. Lett.* **2012**, *100*, 263116.
- [19] Chau, R.; Datta, S.; Doczy, M.; Doyle, B.; Jin, B.; Kavalieros, J.; Majumdar, A.; Metz, M.; Radosavljević, M. Benchmarking nanotechnology for high-performance and low-power logic transistor applications. *IEEE Trans. Nanotechnol.* **2005**, *4*, 153–158.
- [20] Franklin, A. D.; Chen, Z. H. Length scaling of carbon nanotube transistors. *Nat. Nanotechnol.* **2010**, *5*, 858–862.
- [21] Franklin, A. D.; Luisier, M.; Han, S. J.; Tulevski, G.; Breslin, C. M.; Gignac, L.; Lundstrom, M. S.; Haensch, W. Sub-10 nm carbon nanotube transistor. *Nano Lett.* **2012**, *12*, 758–762.
- [22] Kim, W.; Javey, A.; Vermesh, O.; Wang, Q.; Li, Y. M.; Dai, H. J. Hysteresis caused by water molecules in carbon nanotube field-effect transistors. *Nano Lett.* **2003**, *3*, 193–198.
- [23] Bradley, K.; Gabriel, J. C. P.; Star, A.; Grüner, G. Short-channel effects in contact-passivated nanotube chemical sensors. *Appl. Phys. Lett.* **2003**, *83*, 3821–3823.
- [24] Kang, D. H.; Park, N.; Ko, J. H.; Bae, E.; Park, W. J. Oxygen-induced P-type doping of a long individual single-walled carbon nanotube. *Nanotechnology* **2005**, *16*, 1048–1052.
- [25] Moriyama, N.; Ohno, Y.; Kitamura, T.; Kishimoto, S.; Mizutani, T. Change in carrier type in high- k gate carbon nanotube field-effect transistors by interface fixed charges. *Nanotechnology* **2010**, *21*, 165201.
- [26] Kaminishi, D.; Ozaki, H.; Ohno, Y.; Maehashi, K.; Inoue, K.; Matsumoto, K.; Seri, Y.; Masuda, A.; Matsumura, H. Air-stable N-type carbon nanotube field-effect transistors with Si₃N₄ passivation films fabricated by catalytic chemical vapor deposition. *Appl. Phys. Lett.* **2005**, *86*, 113115.
- [27] Franklin, A. D.; Tulevski, G. S.; Han, S. J.; Shahrjerdi, D.; Cao, Q.; Chen, H. Y.; Wong, H. S. P.; Haensch, W. Variability in carbon nanotube transistors: Improving device-to-device consistency. *ACS Nano* **2012**, *6*, 1109–1115.
- [28] Kim, S. K.; Xuan, Y.; Ye, P. D.; Mohammadi, S.; Back, J. H.; Shim, M. Atomic layer deposited Al₂O₃ for gate dielectric and passivation layer of single-walled carbon nanotube transistors. *Appl. Phys. Lett.* **2007**, *90*, 163108.
- [29] Kim, H. S.; Jeon, E. K.; Kim, J. J.; So, H. M.; Chang, H.; Lee, J. O.; Park, N. Air-stable N-type operation of Gd-contacted carbon nanotube field effect transistors. *Appl. Phys. Lett.* **2008**, *93*, 123106.
- [30] Noshu, Y.; Ohno, Y.; Kishimoto, S.; Mizutani, T. N-type carbon nanotube field-effect transistors fabricated by using Ca contact electrodes. *Appl. Phys. Lett.* **2005**, *86*, 073105.
- [31] Ding, L.; Wang, S.; Zhang, Z. Y.; Zeng, Q. S.; Wang, Z. X.; Pei, T.; Yang, L. J.; Liang, X. L.; Shen, J.; Chen, Q. et al. Y-contacted high-performance N-type single-walled carbon nanotube field-effect transistors: Scaling and comparison with Sc-contacted devices. *Nano Lett.* **2009**, *9*, 4209–4214.
- [32] Cavin, R. K.; Lugli, P.; Zhirnov, V. V. Science and engineering beyond Moore's law. *Proc. IEEE* **2012**, *100*, 1720–1749.

- [33] Shahrjerdi, D.; Franklin, A. D.; Oida, S.; Tulevski, G. S.; Han, S. J.; Hannon, J. B.; Haensch, W. High device yield carbon nanotube NFETs for high-performance logic applications. *2011*, 23.3.1–23.3.4.
- [34] Cui, X. D.; Freitag, M.; Martel, R.; Brus, L.; Avouris, P. Controlling energy-level alignments at carbon nanotube/Au contacts. *Nano Lett.* **2003**, 3, 783–787.
- [35] Wilk, G. D.; Wallace, R. M.; Anthony, J. M. High- κ gate dielectrics: Current status and materials properties considerations. *J. Appl. Phys.* **2001**, 89, 5243–5275.
- [36] Kar, S.; Vijayaraghavan, A.; Soldano, C.; Talapatra, S.; Vajtai, R.; Nalamasu, O.; Ajayan, P. M. Quantitative analysis of hysteresis in carbon nanotube field-effect devices. *Appl. Phys. Lett.* **2006**, 89, 132118.
- [37] Estrada, D.; Dutta, S.; Liao, A.; Pop, E. Reduction of hysteresis for carbon nanotube mobility measurements using pulsed characterization. *Nanotechnology* **2010**, 21, 085702.
- [38] Wang, S.; Sellin, P. Pronounced hysteresis and high charge storage stability of single-walled carbon nanotube-based field-effect transistors. *Appl. Phys. Lett.* **2005**, 87, 133117.
- [39] Jin, S. H.; Islam, A. E.; Kim, T. I.; Kim, J. H.; Alam, M. A.; Rogers, J. A. Sources of hysteresis in carbon nanotube field-effect transistors and their elimination via methylsiloxane encapsulants and optimized growth procedures. *Adv. Funct. Mater.* **2012**, 22, 2276–2284.
- [40] Zhou, W. W.; Han, Z. Y.; Wang, J. Y.; Zhang, Y.; Jin, Z.; Sun, X.; Zhang, Y. W.; Yan, C. H.; Li, Y. Copper catalyzing growth of single-walled carbon nanotubes on substrates. *Nano Lett.* **2006**, 6, 2987–2990.