

Synthesis and Device Applications of High-Density Aligned Carbon Nanotubes Using Low-Pressure Chemical Vapor Deposition and Stacked Multiple Transfer

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ABSTRACT

For nanotube-based electronics to become a viable alternative to silicon technology, high-density aligned carbon nanotubes are essential. In this paper, we report the combined use of low-pressure chemical vapor deposition and stacked multiple transfer to achieve high-density aligned nanotubes. By using an optimized nanotube synthesis recipe, we have achieved high-density aligned carbon nanotubes with density as high as 30 tubes/ μm . In addition, a facile stacked multiple transfer technique has been developed to further increase the nanotube density to 55 tubes/ μm . Furthermore, high-performance submicron carbon nanotube field-effect transistors have been fabricated on the high-density aligned nanotubes. Before removing the metallic nanotubes by electrical breakdown, the devices exhibit on-current density of 92.4 $\mu\text{A}/\mu\text{m}$ and normalized transconductance of 13.3 $\mu\text{S}/\mu\text{m}$. Moreover, benchmarking with the aligned carbon nanotube transistors in the literature indicates that our devices exhibit the best performance so far, which is attributed to both the increased nanotube density and scaling down of channel length. This study shows the great potential of using such high-density aligned nanotubes for high performance nanoelectronics and analog/RF applications.

KEYWORDS

Aligned carbon nanotubes, chemical vapor deposition, high-density, high performance transistors

1. Introduction

The application of carbon nanotubes in solid-state electronic devices has stimulated considerable interest due to the extraordinary electronic properties carbon nanotubes can offer [1–5]. Among various types of devices, carbon nanotube field-effect transistors have been extensively used in the demonstration of digital [6–10], analog, and radio-frequency (RF) [11–16] integrated circuits. Transistors using single nanotubes

have been studied and found to offer way better performance compared to silicon transistors in terms of drive-current density, normalized transconductance, mobility etc., when the performance metrics are normalized to the nanotube diameter. Besides single nanotube transistors, another approach is to employ multiple parallel aligned nanotubes and treat them as a thin-film transistor. Among many nanotube synthesis techniques, aligned carbon nanotube growth [17–23] is most desirable for electronic devices owing to its

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advantages of registration-free fabrication, high device yield, superior device performance, and small device-to-device variation. For aligned nanotubes, one of the most important metrics is the nanotube density. High-density aligned nanotubes can be extremely helpful in improving the current driving capability, transconductance, and cut-off frequency of devices.

Inspired by the superior electronic properties of carbon nanotubes and the significant advantage aligned nanotubes can offer, field-effect transistors using aligned nanotubes have been reported by many research groups including our own [21–24]. However, the nanotube density has typically been restricted to 5 to 10 tubes/ μm , which greatly limits the electrical performance such as drive-current and transconductance of the nanotube transistors. As a result, producing high-density aligned nanotubes has become one of the greatest challenges, and significant effort has been devoted to optimized one-step synthesis [25] and the recently-reported two-step synthesis [26]. On the other hand, little has been done to investigate the potential applications of such high-density aligned nanotubes for high performance nanotube transistors.

In this paper, we report another method of producing high-density aligned nanotubes, as well as their application in high performance submicron nanotube transistors. We report the use of low-pressure chemical vapor deposition (LPCVD) to reproducibly achieve perfectly aligned nanotubes with density as high as 30 tubes/ μm . A stacked multiple transfer technique was then used to transfer the aligned nanotubes from multiple starting samples to one target substrate, thus, allowing us to double, triple, or quadruple the nanotube density. A density of 55 tubes/ μm has been demonstrated and further increases can be envisioned. Carbon nanotube field-effect transistors were then fabricated on the high-density aligned nanotubes. Electrical measurements found that for the devices with channel length $L = 0.5 \mu\text{m}$, the increase in nanotube density leads to five-fold and eight-fold increases in the on-current density (I_{on}/W) and normalized transconductance (g_{m}/W), respectively, compared with our previous devices fabricated on nanotubes with a typical density of 5 tubes/ μm [24].

Moreover, benchmarking with the aligned carbon nanotube transistors in the literature indicates that our devices exhibit the best performance so far, which is attributed to both the increased nanotube density and scaling down of channel length. The electrical measurements also suggest the great potential of using our high-density aligned nanotubes for analog and RF devices and circuits.

2. Results and discussion

High-density aligned nanotubes were synthesized using LPCVD with an ethanol bubbler and was carried out at 500 Torr. We have tested various growth conditions within the range $850 \text{ }^\circ\text{C} < T < 950 \text{ }^\circ\text{C}$, $300 \text{ Torr} < P < 760 \text{ Torr}$, and found $900 \text{ }^\circ\text{C}$ and 500 Torr to be the optimum growth condition for our chemical vapor deposition (CVD) system. More details about the nanotube synthesis process are described in the experimental section. After synthesis, field-emission scanning electron microscopy (FE-SEM) was used to inspect the sample, and an image of the as-grown nanotubes on a quartz substrate is shown in Fig. 1(a). The image shows high-density uniform aligned nanotube growth between the catalyst stripes. The width of the catalyst stripe is $4 \mu\text{m}$ and the distance between two different stripes is $100 \mu\text{m}$. Our LPCVD synthesis process is very reproducible, and uniform growth can be achieved throughout the sample. Using this LPCVD recipe, a typical nanotube density of 15–20 tubes/ μm can be achieved throughout the sample, while a density of 30 tubes/ μm can be achieved under optimal growth conditions at certain locations of the sample. Figure 1(b) shows an FE-SEM image of the aligned nanotubes at higher magnification, and the average nanotube density is measured to be around 27 tubes/ μm . Atomic force microscopy (AFM) was used to quantify the nanotube diameter, and the AFM image of the high-density aligned nanotubes is shown in Fig. 1(c). The nanotube density is around 19 tubes/ μm in this image and the diameter distribution is plotted in Fig. 1(d), from which the nanotube diameter is measured to be $1.388 \pm 0.457 \text{ nm}$.

Carbon nanotube structural defects and impurities play an important role in determining the ultimate transport properties of nanotube-based devices. We

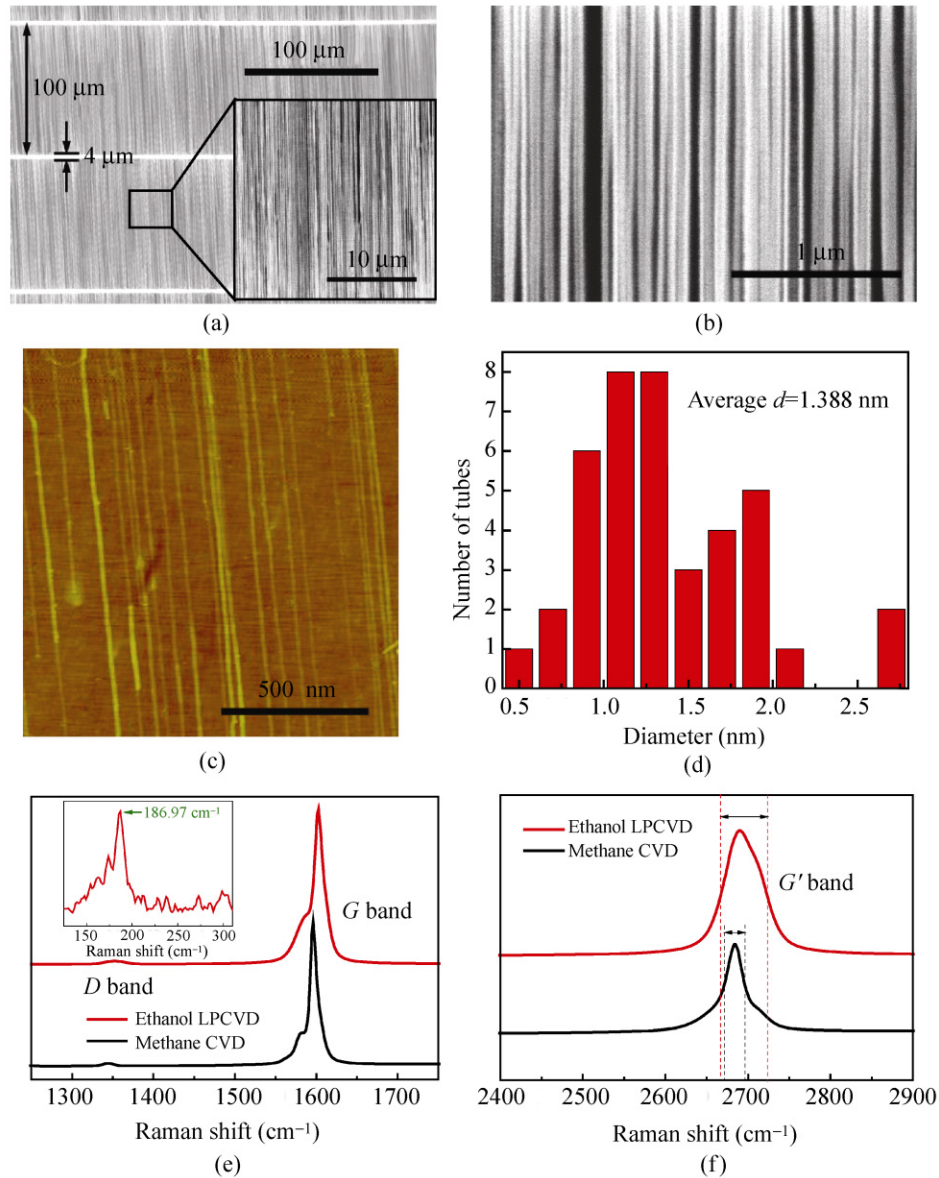


Figure 1 High-density aligned carbon nanotubes synthesized by LPCVD. (a) FE-SEM image showing the aligned nanotubes grown on quartz substrate. (b) FE-SEM image at high magnification showing the as-grown aligned nanotubes with an average density of 27 tubes/ μm . (c) AFM image showing the aligned nanotubes with an average density of 19 tubes/ μm . (d) Diameter distribution of the nanotubes extracted from the AFM image. The diameter is 1.388 ± 0.457 nm. Raman spectra showing the (e) D-band and (f) G'-band of the as-grown aligned nanotubes with high-density (30 tubes/ μm) using ethanol LPCVD and typical density (5 tubes/ μm) using methane CVD. (e) Inset: Radial breathing mode (RBM) of the high density nanotube sample

performed micro-Raman spectroscopy measurements using an excitation laser energy of 2.32 eV on the high-density aligned nanotubes as well as on the nanotube arrays with regular nanotube density (~ 5 tubes/ μm) that were obtained using methane as the carbon source. Typical normalized stacked Raman spectra of high and low nanotube density samples show a nearly identical D-band to G-band intensity ratio (I_D/I_G) of

0.017 (Fig. 1(e)), which suggests that the use of ethanol during high-density nanotube synthesis did not yield increased structural defects or additional oxygen functionalities on the nanotubes. However, a significant broadening of the Raman G'-band of around 31.6 cm^{-1} gives evidence of an increased inter-tube interaction for high-density nanotubes (Fig. 1(f)). This can be attributed to the formation of nanotube bundles or to

the close proximity of certain nanotubes forming the parallel arrays on the high-density sample. Moreover, the radial breathing mode (RBM) frequency of the high density sample (shown in the inset of Fig. 1(e)) is 186.97 cm^{-1} . This corresponds to a nanotube diameter of 1.326 nm , which is consistent with the AFM measurement results.

Compared with the density of $5\text{ tubes}/\mu\text{m}$ reported in our previous publications [23, 24], the above-reported nanotube density of $30\text{ tubes}/\mu\text{m}$ using ethanol LPCVD is a significant improvement. To further improve the nanotube density, multiple transfer can be used which allows us to transfer nanotubes from multiple quartz samples to one target substrate thus, multiplying the density. The multiple transfer technique utilizes the gold film plus thermal release tape method reported in our previous publications [23, 24], which allows the transfer of the as-grown nanotubes from quartz substrates to Si/SiO₂ substrates or many other substrates. More details of our nanotube transfer method are discussed in the experimental section. We have previously reported the layer-by-layer multiple transfer technique [23], in which we transfer the nanotubes to Si/SiO₂ substrates using gold film, etch away the gold, and then repeat the transfer. However, this technique was limited to two samples, beyond which the adhesion between the gold film and the substrate became problematic. Here, in order to overcome the adhesion problem, we developed a stacked multiple transfer method, in which the gold film containing the aligned nanotubes can be repeatedly transferred on top of the previous gold film, and etched at the same time using the gold etchant, so that the nanotubes collapse onto the substrates. We have tested our stacked multiple transfer technique and found that the same transfer process can be repeated up to four times without any adhesion problem. The above-mentioned multiple transfer process is illustrated schematically in Fig. 2(a), and the FE-SEM images of the aligned nanotubes before transfer, after one-time transfer, two-time transfer, and four-time transfer are shown in Figs. 2(b)–2(e), respectively. The corresponding densities are $15\text{ tubes}/\mu\text{m}$, $15\text{ tubes}/\mu\text{m}$, $29\text{ tubes}/\mu\text{m}$, and $55\text{ tubes}/\mu\text{m}$. From the SEM images, one can find that the multiple transfer process indeed increases

the nanotube density effectively.

We have found that in order to achieve high-yield transfer, it is crucial to use thin gold film and keep the perturbation during the gold etching process to a minimum. Moreover, as the density increases, the demands on the orientational alignment increases. Therefore, it is crucial to use accurately diced samples and perform careful alignment during the multiple transfer process. Additional information about the stacked multiple transfer process can be found in Fig. S-1 of the Electronic Supplementary Material (ESM). We also note that the nanotubes after transfer are not as straight as before, which can be attributed to the perturbation experienced by the nanotubes during the gold etching and deionized (DI) water rinsing step. This slight waviness can lead to increased tube-to-tube interactions, and may result in unwanted cross-talking and limit the high-frequency performance of the nanotube transistors. Therefore, methods to improve the straightness of the transferred nanotubes such as the use of supercritical drying during the etching process are worthy of further investigation. Moreover, by combining our LPCVD and stacked multiple transfer technique, it should be possible to achieve a nanotube density of $100\text{ tubes}/\mu\text{m}$ or $200\text{ tubes}/\mu\text{m}$ in the future, which is critical in order to ensure sufficient performance gains over state-of-the-art silicon complementary metal-oxide-semiconductor (CMOS) transistors with shrinking lithographic dimensions [27].

High-density aligned carbon nanotubes are very important and desirable for analog and RF applications where the frequency response of the device matters [28, 29]. Intuitively, higher nanotube density will result in higher drive-current and larger transconductance. Since the cut-off frequency of the device is $f_T \approx g_m / [2\pi \times (C_{gs} + C_{gd})]$, increasing the nanotube density should increase the device cut-off frequency approximately proportionally [29]. Moreover, if we define the nanotube filling ratio as nanotube density times nanotube diameter divided by one micron, as the nanotube density increases, the filling ratio increases. Ideally, we want the device channel to be covered with closely packed aligned carbon nanotubes with a filling ratio of 100%. This will increase the

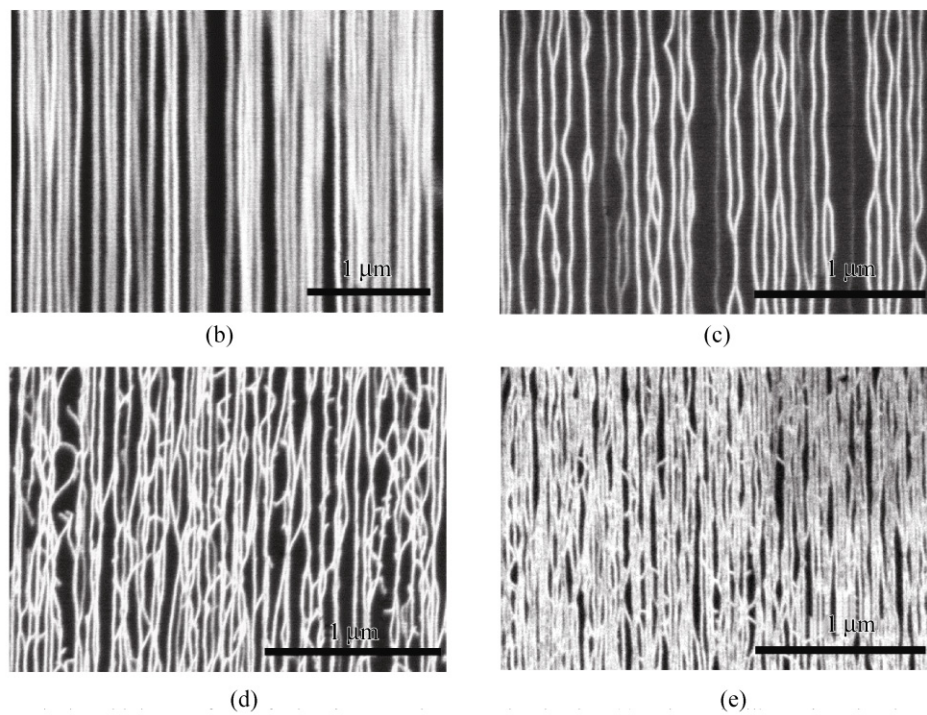
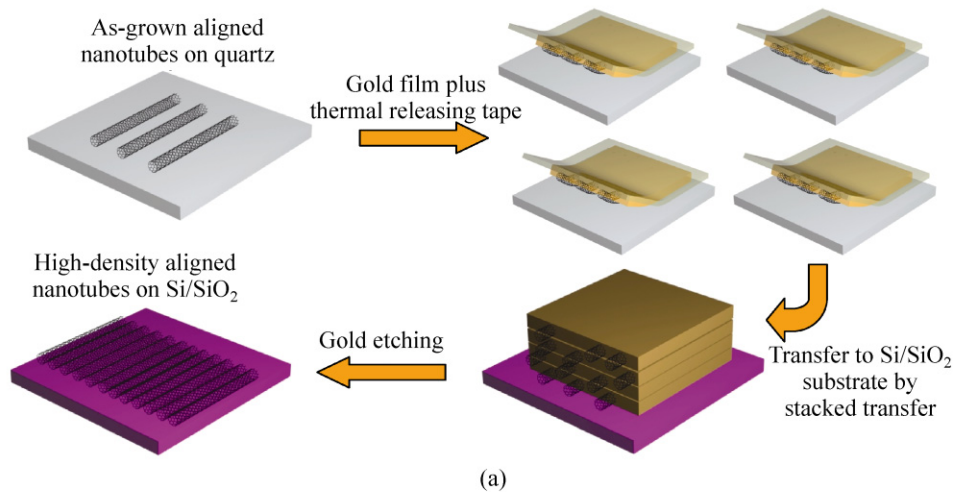


Figure 2 Using stacked multiple transfer to further increase the nanotube density. (a) Schematic illustration showing the stacked multiple transfer process. (b) FE-SEM image of the as-grown aligned nanotubes on a quartz substrate with a density of 15 tubes/ μm . (c, d, e) FE-SEM images showing the aligned nanotubes transferred to Si/SiO₂ substrates with one-time, two-time, and four-time transfer, respectively. The corresponding average densities are 15 tubes/ μm , 29 tubes/ μm , and 55 tubes/ μm

transconductance (g_m) without a significant increase in the parasitic capacitance, allowing the maximum RF performance to be achieved [29].

To evaluate the electrical performance of such high-density aligned nanotubes based on multiple transfer, back-gated transistors were fabricated. 50 nm SiO₂ was used as the back-gate dielectric, and the source/drain electrodes were patterned by photolithography.

2 nm Ti and 60 nm Pd were deposited by e-beam evaporation, followed by a lift-off process to form the source and drain metal contacts. Photolithography plus O₂ plasma was used to remove the unwanted nanotubes outside the device channel region in order to achieve accurate channel length and width, and to remove any possible leakage between the devices. A schematic illustration of the back-gated nanotube

transistor used in this study is shown in Fig. 3(a). Such back-gated transistors were made with channel width (W) of 10, 20, 50, 100, and 200 μm , and channel length (L) of 4, 10, 20, 50, and 100 μm .

We have carried out electrical measurements on

such back-gated nanotube transistors with various channel lengths, channel widths, and different nanotube densities. The results are summarized in Fig. 3. Figure 3(b) exhibits the variation of on-current densities (I_{on}/W) with channel length (L) for transistors

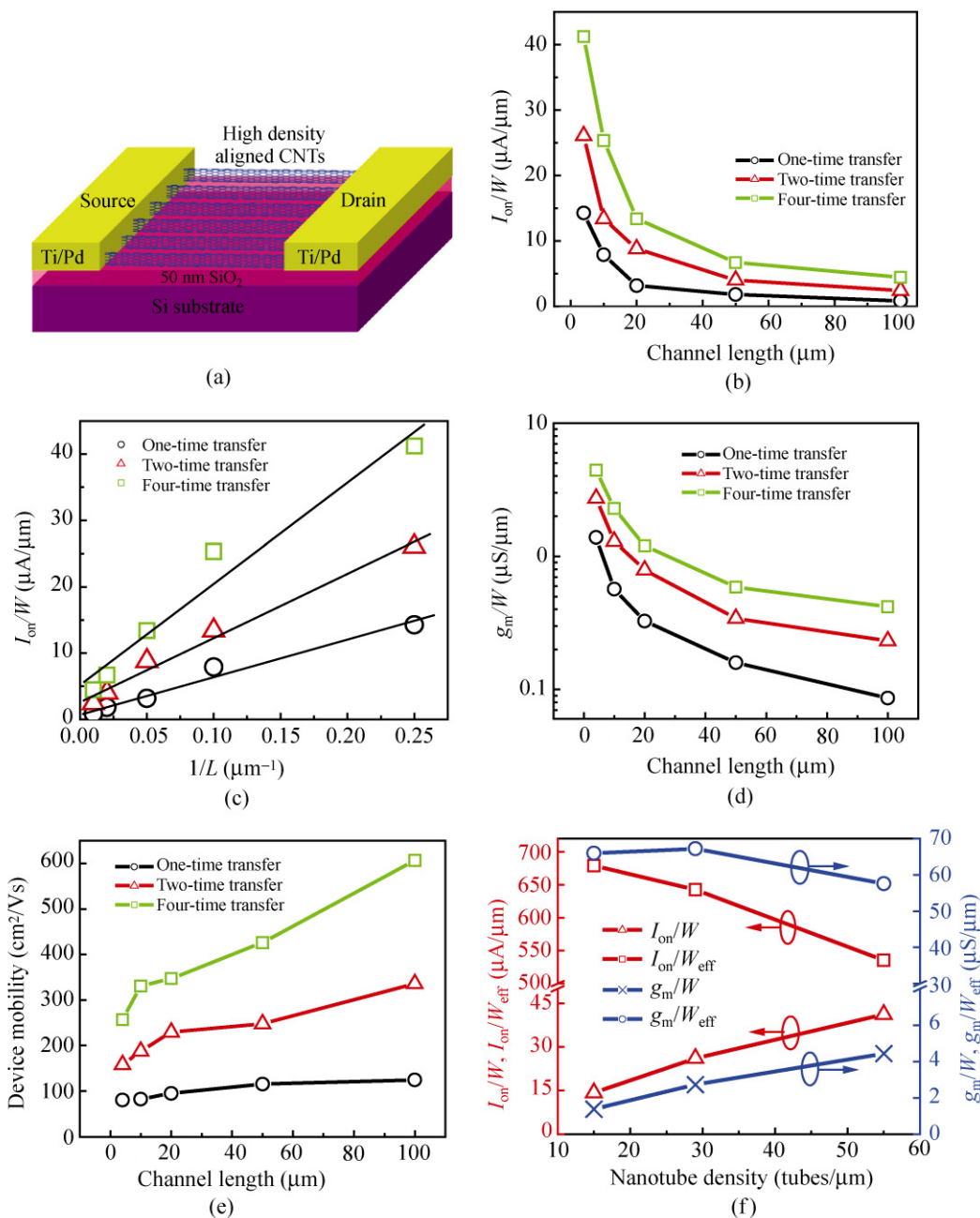


Figure 3 Electrical measurements of the back-gated nanotube transistors using nanotubes with one-time, two-time, and four-time transfer. (a) Schematic illustration of the back-gated transistor with high-density aligned nanotubes. (b) Plot of the current density (I_{on}/W) versus channel length (L) for devices fabricated using nanotubes with different density. (c) Plot of I_{on}/W versus the reciprocal of channel length ($1/L$) for devices fabricated using nanotubes with different density. Plots of (d) the normalized transconductance (g_m/W) and (e) device mobility (μ_{device}) versus channel length for devices fabricated using nanotubes with different density. (f) Plot showing variation of I_{on}/W , $I_{\text{on}}/W_{\text{eff}}$, g_m/W , and g_m/W_{eff} with nanotube density for the high-density aligned nanotube transistors

with different times of transfer and thus, different densities. The definition of on-current here is the drain-current measured at $V_D = 1\text{ V}$ and $V_G = -10\text{ V}$. This figure indicates that as the nanotube density increases, the drive current also increases, as expected. The highest on-current density is around $41\ \mu\text{A}/\mu\text{m}$ and is achieved in the devices with four-time transfer and channel length of $4\ \mu\text{m}$. To give more insight into the relationship between the on-current density and channel length, the on-current density is plotted against the reciprocal of channel length, as shown in Fig. 3(c). From the figure, one can find that the on-current density is approximately inversely proportional to the channel length.

Transconductance (g_m) is another important figure of merit for nanotube field-effect transistors as it dictates the cut-off frequency of the devices. The normalized device transconductance (g_m/W) of devices with various channel lengths is plotted in Fig. 3(d). In this figure, g_m is extracted from the maximum slope of the transfer characteristics measured at $V_D = 1\text{ V}$, and is normalized to device channel width. From the figure, one can find that as channel length increases, g_m/W decreases, which is because g_m/W is inversely proportional to the channel length. Moreover, similar to the on-current density, the normalized transconductance is also approximately proportional to nanotube density.

The device mobility can be further extracted based on the normalized transconductance. When $V_D = 1\text{ V}$, devices operate in the triode regime, so that the device mobility can be calculated from the following equation

$$\mu_{\text{device}} = \frac{L}{V_D C_{\text{ox}} W} \cdot \frac{dI_d}{dV_g} = \frac{L}{V_D C_{\text{ox}}} \cdot \frac{g_m}{W} \quad (1)$$

where L and W are the device channel length and width, $V_D = 1\text{ V}$, and C_{ox} is the gate capacitance per unit area. C_{ox} can be calculated using the parallel plate model and the effective device mobility can thus, be derived. We note that a more rigorous model can be used by considering the electrostatic coupling between nanotubes to derive the nanotube mobility [21, 30]. However, the model assumes that the nanotubes are equally spaced. In order to obtain the capacitance accurately, non-ideal effects such as nanotube bundling,

uniformity of nanotube density across the device channel, and percentage of nanotubes bridging the source/drain electrodes has to be taken into consideration, and those are difficult to model rigorously. We have calculated the effective device mobility of transistors with various channel length, width, and nanotube density, and the results are plotted in Fig. 3(e). It is worth noting that we did not attempt to account for the contact resistance between the nanotubes and the source/drain electrodes. Therefore, we observe that as the channel length increases, the device mobility increases, indicating that there is certain amount of contact resistance in the metal/nanotube contacts. As the channel length increases, the effect of metal/nanotube contacts become less significant and the mobility increases [21]. The highest effective device mobility from the back-gated transistors is around $607\text{ cm}^2\text{ V}^{-1}\text{s}^{-1}$ achieved in devices with four-time transfer and $100\ \mu\text{m}$ channel length.

To further elucidate the properties of the nanotubes, we define effective channel width (W_{eff}) as the average nanotube diameter multiplied by the total number of nanotubes in the channel. Figure 3(f) summarizes the variation of I_{on}/W , g_m/W , effective on-current density ($I_{\text{on}}/W_{\text{eff}}$), and effective normalized transconductance (g_m/W_{eff}) as a function of nanotube density. The effective on-current density and effective normalized transconductance are defined as the I_{on} and g_m of the devices normalized by the effective channel width. $I_{\text{on}}/W_{\text{eff}}$ and g_m/W_{eff} are good measures of performance per nanotube and can be calculated from the equations below

$$I_{\text{on}}/W_{\text{eff}} = \frac{I_{\text{on}}/W}{D \cdot d}, \quad g_m/W_{\text{eff}} = \frac{g_m/W}{D \cdot d} \quad (2)$$

where D stands for the nanotube density in tubes/ μm and d is the nanotube diameter which is measured to be around $0.0014\ \mu\text{m}$ for our nanotubes. From Fig. 3(f), we can find that I_{on}/W and g_m/W , which represent the device performance, increase monotonically with nanotube density, while $I_{\text{on}}/W_{\text{eff}}$ and g_m/W_{eff} , which represent the nanotube performance, decrease with nanotube density. The $I_{\text{on}}/W_{\text{eff}}$ decreases by about 21.1% and g_m/W_{eff} decreases by about 12.7% as the nanotube density increases from 15 tubes/ μm to 55 tubes/ μm . The slight decrease in nanotube performance



can be attributed to the formation of nanotube bundles during the multiple transfer process, and is found to be not detrimental to overall device performance.

Similar to the silicon metal-oxide-semiconductor field effect transistors (MOSFETs) widely used in current semiconductor industry, nanotube field-effect transistors with better performance can also be achieved by scaling down the channel length to the submicron regime as well as by increasing the gate strength by adopting high- κ dielectric layer. A schematic illustration of such a high performance submicron nanotube transistor is shown in Fig. 4(a), and the device fabrication processes are briefly described as follows. First, individual back-gates are patterned using photolithography on top of the Si/SiO₂ substrate, and 5 Å Ti and 50 nm Au were deposited to act as the back-gate electrode. 50 nm HfO₂ was then deposited by atomic layer deposition (ALD) to act as the gate dielectric. High-density aligned nanotubes were then transferred to the substrate with a Ti/Au back-gate and HfO₂ gate dielectric. The rest of the fabrication steps including the source/drain electrodes patterning and unwanted nanotube etching are very similar to those used in the fabrication of the back-gate transistor discussed previously except that an I-line wafer stepper (GCA Autostep 200) was used to pattern the source/drain electrodes instead of a contact aligner. The use of a stepper allows us to achieve minimum channel length of 500 nm in a scalable manner. An FE-SEM image of the channel of a typical high performance submicron nanotube transistor ($L = 500$ nm) is shown in Fig. 4(b) where the average nanotube density is around 30 tubes/ μm .

The electrical performance of such high performance devices was characterized. Figures 4(c), 4(d), and 4(e) are the transfer characteristics (I_D - V_G curves) measured at $V_D = 1$ V for a transistor with $W = 50$ μm and $L = 500$ nm before and after electrical breakdown. From the curves, one can find that before electrical breakdown, the on-state current of the device (I_{on}) measured at $V_D = 1$ V and $V_G = -5$ V, is 4.62 mA, which corresponds to I_{on}/W of 92.4 $\mu\text{A}/\mu\text{m}$. To the best of our knowledge, this on-current density is the highest so far reported for aligned nanotube transistors. The maximum transconductance (g_m) of the device is

measured to be 663.3 μS , which corresponds to g_m/W of 13.3 $\mu\text{S}/\mu\text{m}$. We note that the on-off ratio of the device is only around 3 due to the coexistence of both metallic and semiconducting nanotubes. This result agrees with the typical 1/3 metallic nanotube ratio assuming equal conduction from metallic and semiconducting nanotubes.

By using automated electrical breakdown techniques as discussed in our previous work [23], metallic nanotubes were selectively removed and the on-off ratio of the device underwent a significant improvement to around 1000, accompanied by a degradation of the on-current of around 90% (Fig. 4(e)). Assuming a 1/3 metallic nanotube ratio, one should expect around 33% on-current degradation after electrical breakdown. The much higher observed degradation of 90% in our measurements can be explained by the unintentional damage of semiconducting nanotubes under large electrical stress during the electrical breakdown process. It is possible that along with the metallic nanotubes, some defective semiconducting nanotubes can also be damaged under high V_D biases. More importantly, besides the defective semiconducting nanotubes, there may be some large diameter semiconducting nanotubes which have small bandgaps and thus, will have small on/off ratios. These semiconducting nanotubes can also be destroyed during the electrical breakdown process since they cannot be turned-off completely. Both reasons mentioned above account for the degradation in the on-current of 90%, instead of the expected 33%.

From Fig. 4(d), after the electrical breakdown, I_{on}/W is 8.3 $\mu\text{A}/\mu\text{m}$ and g_m/W is 2.2 $\mu\text{S}/\mu\text{m}$. Compared with the results from devices fabricated using aligned nanotubes with typical density (5 tubes/ μm) reported in our previous publication ($I_{\text{on}}/W = 1.7$ $\mu\text{A}/\mu\text{m}$ and $g_m/W = 0.28$ $\mu\text{S}/\mu\text{m}$) [24], the values of I_{on}/W and g_m/W reported here are 5 times and 8 times better, respectively. The improvements are due to both the higher nanotube density and the adoption of a high- κ gate dielectric.

Figure 4(f) shows the output characteristics (I_D - V_D curves) of the device measured under different gate biases. Under small negative V_D biases, i.e., $|V_D| < |V_{\text{DSAT}}|$, the device operates in the triode regime, and the I_D - V_D curves appear to be linear, indicating that

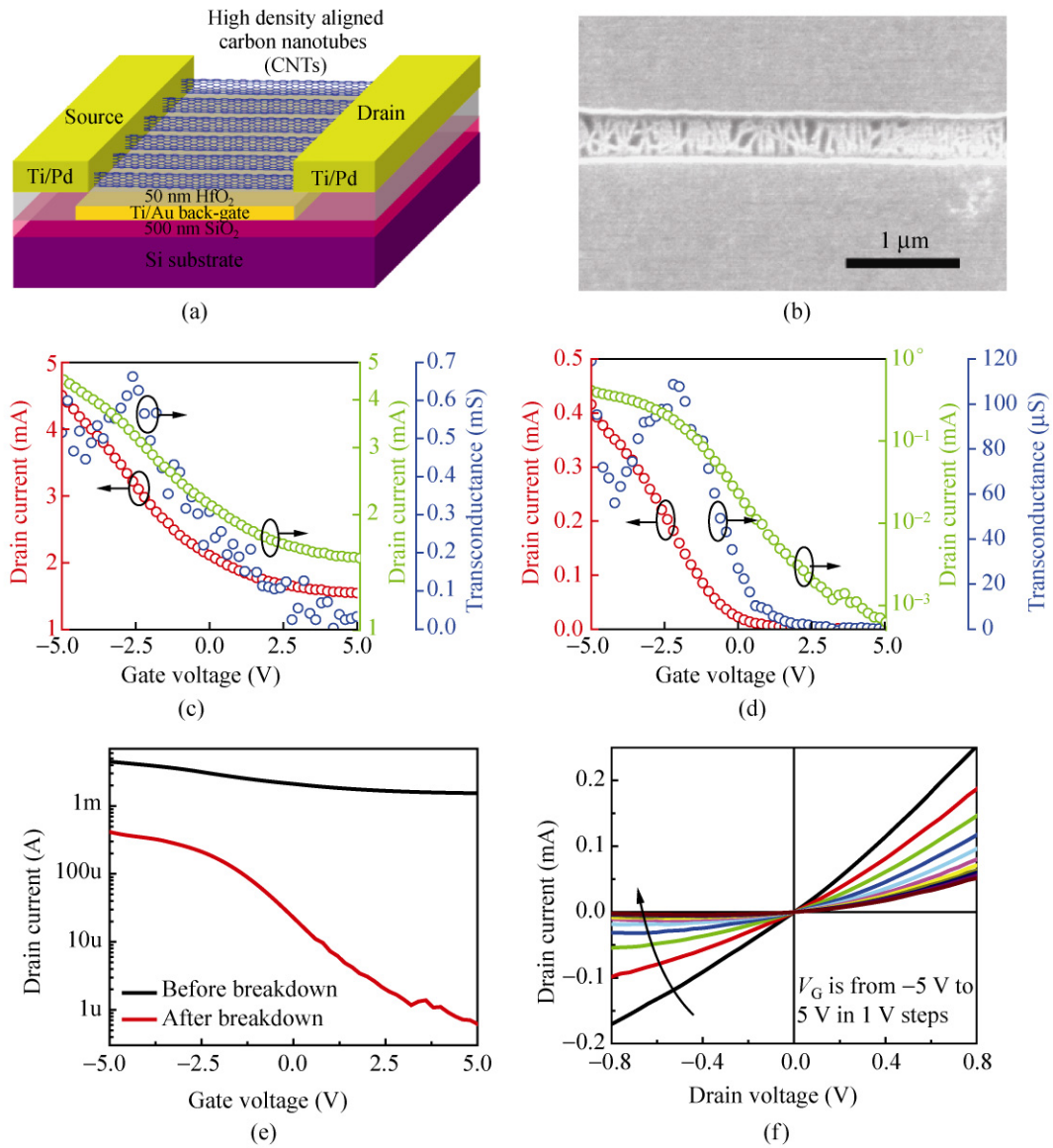


Figure 4 Electrical properties of high performance submicron transistors with high-density aligned nanotubes. (a) Schematic view of the high performance submicron nanotube transistor with Ti/Au individual back-gate and 50 nm HfO₂ high-κ dielectric. (b) FE-SEM image showing the channel of a submicron high performance transistor. The channel length is 0.5 μm and the aligned nanotubes in the channel have an average density of 30 tubes/μm. Transfer (I_D - V_G) characteristics (red: linear scale, green: log scale) and g_m - V_G characteristics (blue) of a high performance nanotube transistor ($L = 0.5 \mu\text{m}$ and $W = 50 \mu\text{m}$) measured at $V_D = 1 \text{ V}$ (c) before and (d) after electrical breakdown. (e) Comparison of the transfer characteristics of the same device before and after electrical breakdown. (f) Output (I_D - V_D) characteristics of the same device after electrical breakdown

Ohmic contacts instead of Schottky contacts are formed between the metal and the nanotubes. Under larger negative V_D biases, i.e., $|V_D| > |V_{DSAT}|$, the device enters the saturation regime, and the drain current begins to saturate. For curves with more negative V_G biases (black and red curves), no clear saturation behavior is observed from the output characteristics. The reason is that $|V_{DSAT}|$ is larger for

more negative V_G biases, so that the device stays in the triode regime within the V_D sweeping range. Moreover, the asymmetric behavior in the 1st and 3rd quadrants is due to different electrostatics for positive and negative V_D , as reported previously [31]. In the 1st quadrant, where “drain” voltage is positive and “source” is grounded, the source and drain terminals are actually swapped since the source for a



p-type transistor is the one with higher voltage. So as “drain” voltage increase, $|V_{GS}|$ increases so that the current increases approximately quadratically.

To justify the high performance of our high-density nanotube transistors, they were benchmarked with previously published work, and the results are shown in Fig. 5. The drive-current (I_{on}/W) is plotted versus year for the previously published aligned nanotube transistor work from University of Southern California (USC) [23, 32, 33], University of Illinois at Urbana-Champaign (UIUC) [15, 20, 26], Stanford University [34, 35], and Duke University [36]. From the figure, one can find that by increasing the nanotube density and scaling down the channel length, our devices with 0.5 μm channel length exhibit a drive-current of 92.4 $\mu\text{A}/\mu\text{m}$, which is the best reported performance to date. This indicates the great potential of using our approach for future beyond-silicon nanoelectronics and RF applications.

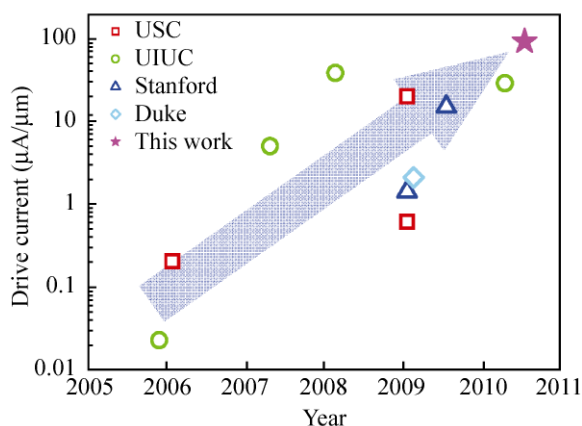


Figure 5 Benchmarking the high performance submicron nanotube transistors using high-density aligned nanotubes with the previously published work. The drive-current (I_{on}/W) is plotted versus year for the previously published aligned nanotube transistor work at USC, UIUC, Stanford, and Duke

3. Conclusions

In conclusion, we have developed a LPCVD and stacked multiple transfer technique to achieve high density aligned nanotubes with density up to 55 tubes/ μm . High performance submicron nanotube transistors have also been fabricated based on the high-density aligned nanotubes and electrical measurements show that the devices exhibit pronounced higher

performance in terms of I_{on}/W and g_m/W compared with devices fabricated on aligned nanotubes with typical density. Our approach holds great potential for high performance analog and RF applications.

Experimental

Aligned nanotube synthesis. Photolithography was used to pattern stripes on the stable-temperature (ST)-cut quartz substrate (Hoffman Materials Inc.). 2 \AA iron was then deposited using a thermal evaporator followed by the lift-off process to form the catalyst stripes. The samples were first annealed in air at 900 $^{\circ}\text{C}$ for 1 h, and LPCVD was then used to grow aligned nanotubes between the catalyst stripes at 900 $^{\circ}\text{C}$. The feed gases were 300 standard cubic centimeters per minute (sccm) H_2 and 120 sccm Ar flowing through an ethanol bubbler kept at 0 $^{\circ}\text{C}$. The furnace was connected to a mechanical pump and the pressure inside the quartz tube was kept constant at 500 Torr using a butterfly valve.

Nanotube transfer. 30 nm gold film was deposited onto the quartz substrates containing nanotubes, and thermal release tape (# 3198M from Nitto Denko) was used to peel off the gold film together with the nanotubes, which was then pressed with a polydimethylsiloxane (PDMS) stamp against the targeted substrates preheated on a hotplate at 140 $^{\circ}\text{C}$ for 10 seconds. After this process, the thermal tape was peeled off with the PDMS stamp. Finally, oxygen plasma was used to clean the tape residue and gold etchant was used to remove the gold film, leaving only aligned nanotubes on the target substrate.

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Electronic Supplementary Material: Additional information about the stacked multiple transfer process is available in the online version of this article at <http://dx.doi.org/10.1007/s12274-010-0054-0>.

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