Springer

KSME

Journal of Mechanical Science and Technology 28 (6) (2014) 2281~2285
www.springerlink.com/content/1738-494x
DOI 10.1007/s12206-014-0517-4

Negative electrode structure design in InSb focal plane array detector for deformation reduction †

Xiaoling Zhang[1], Qingduan Meng[2,*] Liwen Zhang[2] and Yanqiu Lv[3]

[1]*School of Information Engineering, Henan University of Science and Technology, Luoyang 471023, China*
[2]*School of Electrical Engineering, Henan University of Science and Technology, Luoyang 471023, China*
[3]*Luoyang Opto-electro Technology Development Center, Luoyang, 471009, China*

(Manuscript Received March 31, 2013; Revised February 3, 2014; Accepted February 18, 2014)

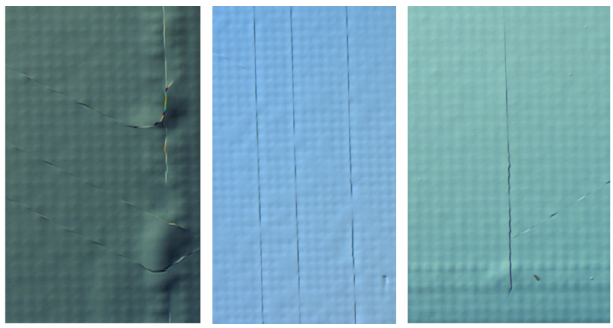
Abstract

When an indium antimonide (InSb) infrared focal plane array (IRFPA) is subjected to a thermal shock test, most of the cracks originate from the region over the negative electrode, which restricts its final yield. In light of the proposed equivalent modeling, three negative electrode structures are assessed to eliminate the accumulated deformation around the negative electrode. Simulation results show that when a thicker indium bump array is connected directly with negative InSb material, the accumulated thermal deformation is the minimum, the top surface of InSb chip is the smoothest, and the square checkerboard buckling pattern, present clearly in both gold buffer layer and sparse thicker indium bump array structure, seems to be unclear. All these mean that a thicker indium bump array structure is a good choice, which will benefit to reduce fracture probability of InSb IRFPAs under thermal shock.

Keywords: Crack; Infrared focal plane arrays; Modeling; Packaging

1. Introduction

Indium antimonide (InSb) PN junctions are widely used as infrared photovoltaic detectors and imaging sensors for the 3-5 μm spectral range. For higher spatial resolution of the image, an InSb staring infrared focal plane array (IRFPA) detector is commonly designed with larger format, such as 1024×1024 pixels (1024 columns, 1024 rows), and 2048×2048 or even more larger arrays [1-3]. To obtain higher signal to noise ratio, InSb IRFPA usually operates at liquid nitrogen temperature (77 K), yet assembled at room temperature (300 K). When its temperature rapidly decreases from 300 K to 77 K, due to thermal mismatch between neighboring components, the induced thermal strain and stress cause the InSb chip to fracture. Typical fracture photographs are shown in Figs. 1, and the fracture probability, just as the patterns appearing in Figs. 1(a), (b), and (c), is about 70%, 20%, and 10%, respectively. Apparently, in the typical fracture photographs of InSb IRFPA, the great majority of cracks initiate in the InSb chip, and the initiating positions are located over the negative electrode; all these imply that the negative electrode design may be a major cause to incur InSb fracture under thermal shock. So in this paper, three typical negative electrode designs are proposed to research their effect to InSb chip deformation.



(a) (b) (c)

Fig. 1. Typical fracture photographs presented in InSb IRFPA under thermal shock.

2. InSb IRFPas structure, fabrication process

The InSb IRFPA is usually composed of three layers, including the upper InSb photosensitive layer, the bottom silicon readout integrated circuit (ROIC) and the intermediate interconnecting layer, made of indium bump array and reticular underfill [2]. The InSb IRFPA is usually fabricated by flip-chip bonding technology, that is, indium bumps are formed first on both detector array and silicon ROIC, then detector array and silicon ROIC are aligned and force is applied to cause indium bumps to cold-weld together. In large format

*Corresponding author. Tel.: +86 379 6423 1157, Fax.: +86 379 6423 1910
E-mail address: qdmengly@163.com
† Recommended by Associate Editor Moon Ki Kim

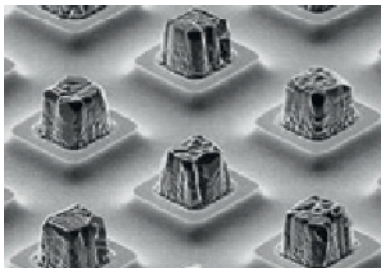


Fig. 2. SEM photo shows mesa photodiode array with indium bumps.

InSb IRFPAs, mesas are etched to make an array of photodiodes, just as shown in Fig. 2; here indium bumps have been attached to the positive electrodes of InSb photodiodes [2]. In InSb IRFPA structure, photodiodes are usually distributed uniformly in both the central and the outmost regions, and between them, the negative electrode exists. In this paper, three negative electrode connections are analyzed, which correspond to gold buffer layer structure, thicker indium bump array structure, and sparse thicker indium bump array structure, respectively. In gold buffer layer structure, the negative InSb is connected with indium bump by means of gold buffer layer, and all the indium bumps have the same thickness. In thicker indium bump array structure, the indium bump array is elongated to connect with negative InSb directly. And in sparse higher indium bump array, the thicker indium bump array is sparse.

3. Model creation and parameters selection

The structure of InSb IRFPAs is complex, and with characteristic sizes ranging from a few micrometers to several centimeters, so in the structure modeling creation, a large number of elements are needed, which leads to the stiffness matrix being too large to be solved. To overcome this problem, an equivalent modeling was proposed in Ref. [4], where a smaller array is employed to replace the larger array to create the structural modeling.

The CTE of material is strongly dependent on the temperature, usually decreasing with decreasing temperature. To calculate exactly the accumulated thermal strain in the layered structure, in this paper, the employed CTE models are all temperature-dependent. Both silicon ROIC and gold layer are homogeneous and isotropic linear elastic materials, InSb is an anisotropic linear elastic material, indium bump is a viscoplastic material and its Young's modulus increases with decreasing temperature. Underfill is a viscoelastic material in its glass transmitting region, once completely cured, and shows obviously linear elastic feature. The CTEs for different materials are plotted in Fig. 3 [5-10].

In the InSb chip, its thickness is only 10 μm, and there are four parallel or vertical isolation troughs around every mesa-junction with depth about 2-4 μm; besides, both median cracks (3-4 μm) and lateral cracks (1-2 μm) may appear in InSb chip backside thinning process [11], and all these factors

Table 1. Elastic material parameters at different temperatures.

Materials	Elastic modulus (E/GPa)	Poisson's ratio (μ)	Temperatures (T/K)
Silicon ROIC	163	0.28	77-300
InSb chip	409 (in plane)	0.35	77-300
	122.7 (out-of-plane)		
Indium bump	20.54	0.4326	76
	16.24	0.4408	187
	12.70	0.4498	300
Underfill	0.0002/α	0.30	77-300
Gold layer	79	0.44	77-300

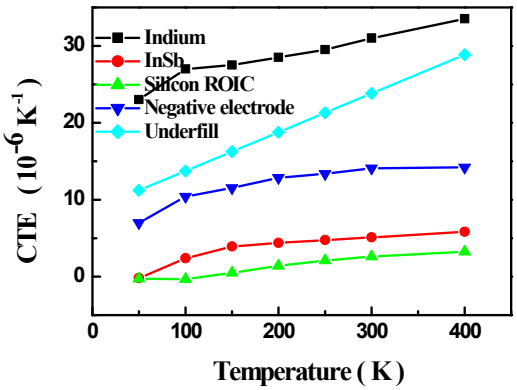


Fig. 3. Linear coefficients of thermal expansion as a function of temperature for InSb, indium bumps, underfill, negative electrode and silicon ROIC.

will weaken the toughness of InSb chip along its normal direction. In previous research, we found that when the out-of-plane elastic modulus of InSb chip is set with 30 percent Young's modulus, fracture initiating sites, cracks distribution and Z-component of strain distribution appearing in the simulating results are all well in agreement with the fracture statistics results of 128×128 InSb IRFPAs under thermal shock test [12].

All the employed mechanical property parameters are listed in Table 1, where E is Young's modulus, μ is Poisson's ratio, and CTE is the coefficient of thermal expansion.

From 50 K to 370 K, the linear thermal expansion coefficient of underfill α can be approximated by [5]

$$\alpha = 22.46\times10^{-6} + 5.04\times10^{-8}\times(T-273) \quad (1)$$

where T is in kelvin.

4. Results and discussions

In gold buffer layer structure, the negative InSb is connected with indium bump by means of gold buffer layer, and all the indium bumps have the same thickness. Here the normal Young's modulus of InSb is set at 30 percent of bulk

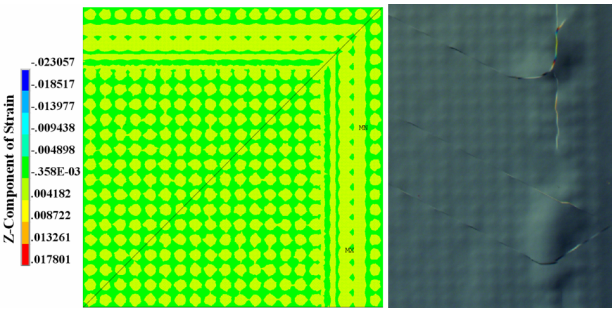


Fig. 4. (a) Simulated Z-component of strain distribution with gold buffer layer; (b) typical fracture photograph.

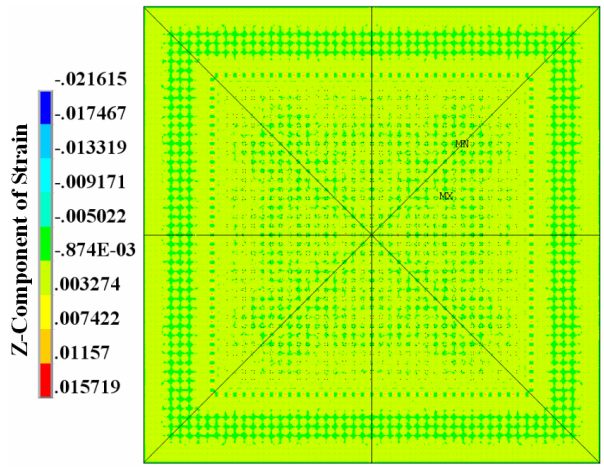


Fig. 5. Simulated Z-component of strain distribution with thicker indium bump array.

modulus, the simulated surface deformation in InSb IRFPAs is shown in Fig. 4(a), for comparison; here InSb IRFPA top surface deformation optical photograph is also shown in Fig. 4(b). Apparently, the simulated Z-component strain distribution not only presents both crack initiating spots and crack pattern, but also offers the overall surface deformation characteristic, and it almost contains completely all the typical fracture features appearing in the InSb IRFPA failure pattern. So in this paper, Z-component strain is selected as the criterion to assess the structural reliability of the InSb IRFPA.

To eliminate the strain concentrated in the region over the negative electrode, the indium bump array is elongated and connected with negative InSb material directly; thus the gold buffer layer is abandoned. Compared with the gold layer, Young's modulus of indium is smaller, and is almost one-fourth of gold. All these are aimed at reducing the accumulated thermal strain by means of the easier deforming ability of indium. The simulated Z-component strain is shown in Fig. 5. Compared with the Z-component strain appearing in Fig. 4(a), where the gold buffer layer is selected, the simulated Z-component strain with thicker indium bump array is more advantageous in the following aspects. First, the maximal Z-component strain is 0.01572, smaller than 0.01780, appearing in gold buffer layer structure; besides, its variation range also

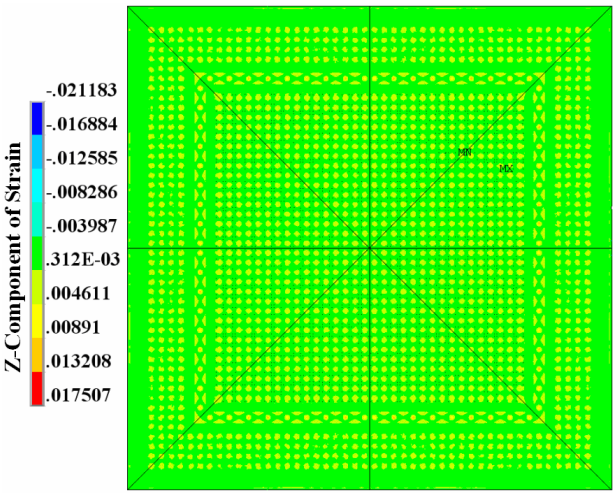


Fig. 6. Simulated Z-component of strain distribution with sparse thicker indium bump array.

reduces from 0.04086 to 0.03734, which means the peak to trough amplitude decreases. Correspondingly, the top surface of the InSb chip becomes flat. Secondly, the maximal Z-component strain moves from the region over negative electrode to central photodiodes array region, and the square checkerboard buckling pattern appearing clearly in Fig. 4(a) blurs, particularly in the central region of photodiodes array. Note that the strain concentrating effect in the region over the negative electrode is still obvious, and its extrema take on non-continuous distribution. On the regions connected with indium bump array, InSb chip shifts upward greatly, and on the locations contacting with meshy underfill, InSb chip shifts downward slightly.

In Fig. 4(b), we notice that the local thermal deformation is not manifest in the outmost region of the InSb IRFPAs, where InSb chip adheres well with silicon ROIC by means of underfill, and indium bump does not exist. Taking account of the fact in InSb chip, the regions where connected with indium bump array shifted upward, and connected with underfill shifted downward; thus the sparse thicker indium bump array structure is proposed to further reduce the accumulated thermal strain appearing around negative electrode. Here the number of higher indium bumps is reduced by half, and keeps other structural parameters unchanged; the simulated Z-component of strain is illustrated in Fig. 6. Compared with thicker indium bump array structure, its maximal Z-component of strain is still located in the central photodiode array. The strain concentrating effect in the region over the negative electrode seems to decrease, yet the square checkerboard buckling pattern also reappears clearly on the whole top surface of InSb chip, and at the same time, the peak to trough amplitude also increases. So the sparse thicker indium bump array structure is not a satisfactory design.

To assess thoroughly the above described three negative electrode structures, in Fig. 7, the maximal deformations in

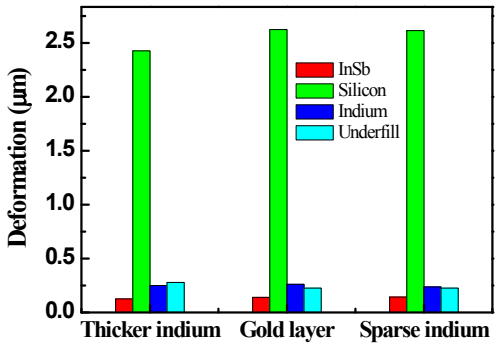


Fig. 7. Maximal Z-direction deformation obtained with different negative electrode structure.

different layers are plotted together [13]. Apparently, in the whole device, the maximal deformation amplitude, about 2.5 μm, appears on top surface of silicon ROIC, where the maximal thermal mismatch exists. When passing through the 10 μm intermediate layer, the deformation amplitude is significantly reduced to 0.25 μm, and after passing through InSb chip, the deformation amplitude is further decreased to 0.14 μm. This change trend has nothing to do with the negative electrode structure.

Up to now, we conclude that in both the central and outmost regions of the photodiode array, the interaction between neighboring materials is local, and around the negative electrode, the negative electrode structure has a great effect on the thermal strain accumulation; thus the uniform indium bump array should an acceptable design scheme.

5. Conclusions

Based on the proposed equivalent modeling, three negative electrode structures are assessed to reduce the thermal strain concentrated in the region over negative electrode, where the cracks originate. Simulation results show that when the thicker indium bump array is connected directly with negative InSb material, the top surface of the InSb chip is the smoothest and with the minimal thermal deformation. Neither sparse indium bump array nor gold buffer layer structure is an efficient design in eliminating the accumulated thermal deformation.

Acknowledgment

The research is supported by the Young Scientists Fund of the National Natural Science Foundation of China (Grant No.61107083, 61205090), the Aero Science Foundation of China (Grant No.20100142003) and the Opening fund of State Key Laboratory of Nonlinear Mechanics, Institute of Mechanics, Chinese Academy of Sciences, China.

References

[1] A. W. Hoffman et al., 2K×2K InSb for astronomy, *Proc. SPIE, Optical and Infrared Detectors for Astronomy*, 5499 (2004) 59-67.

[2] A. Rogalski, Progress in focal plane array technologies, *Progress in Quantum Electronics*, 36 (2012) 342-473.

[3] A. W. Hoffman, J. L. Peter and P. R. Joseph, Mega-pixel detector arrays: visible to 28 μm, *Proc. SPIE, Focal plane Arrays for Space Telescopes*, 5167 (2004) 194-203.

[4] Q. D. Meng, X. L. Zhang, L. W. Zhang and Y. Q. Lv, Structural modeling of 128 × 128 InSb focal plane array detector, *Acta Physica Sinica*, 61 (19) (2012) 190701.

[5] Y. He, B. E. Moreira, A. Overson, S. H. Nakamura, C. Bider and J. F. Briscoe, Thermal characterization of an epoxy-based underfill material for flip chip packaging, *Thermochimica Acta*, 357-358 (2000) 1-8.

[6] G. K. White and J. G. Collins, Thermal expansion of copper, silver, and gold at low temperatures, *Journal of Low Temperature Physics*, 7 (1-2) (1972) 43-75.

[7] X. Cheng, C. Liu and V. V. Silberschmidt, Numerical analysis of thermo-mechanical behavior of indium microjoint at cryogenic temperatures, *Computational Materials Science*, 52 (1) (2012) 274-281.

[8] R. W. Chang and M. F. Patrick, Constitutive relations of indium in extreme temperature electronic packaging based on Anand model, *Journal of Electronic Materials*, 38 (9) (2009) 1855-1859.

[9] D. F. Gibbons, thermal expansion of some crystals with the diamond structure, *Physical Review*, 112 (6) (1958) 136-140.

[10] Y. Okada and Y. Tokumaru, Precise determination of lattice parameter and thermal expansion coefficient of silicon between 300 and 1500 K, *Journal of Applied Physics*, 56 (2) (1984) 314-320.

[11] K. Wasmer, C. Ballif, C. Pouvreau, D. Schulz and J. Michler, Dicing of gallium-arsenide high performance laser diodes for industrial applications part I. scratching operation, *Journal of Materials Processing Technology*, 198 (1-3) (2008) 114-121.

[12] Q. D. Meng, Q. Yu, L. W. Zhang and Y. Q. Lv, Mechanical parameters selection in InSb focal plane array detector normal direction, *Acta Physica Sinica*, 61 (22) (2012) 226103.

[13] X. L. Zhang, Q. D. Meng, Q. Yu, L. W. Zhang and Y. Q. Lv, Thermal Buckling Analysis in Insb Focal Plane Arrays Detector, *Journal of Mechanical Science and Technology*, accepted.

XiaoLing Zhang received the B.S. degree in computer software from Zhengzhou University in 2000 and the M.S. degree in applied computer technology from Henan University of Science and Technology in 2008. Her research interests include pattern recognition, tunable devices simulation and IR detectors structural optimization.

QingDuan Meng received the B.S. degree in applied physics in 2000 and the M.S. degree in microelectronics and solid-state electronics in 2003 from Dalian University of Science and Technology, and the Ph.D. degree in condensed matter physics from Institute of Physics, Chinese Academy of Sciences (CAS), in 2006. His research interests are the design and fabrication of high temperature superconductor (HTS) filters, tunable ferroelectric devices, infrared (IR) detectors.

Liwen Zhang obtained her B.E. and M.S. degree in Physics from Zhengzhou University, Zhengzhou, from 1997 to 2004; then received her Ph.D. degree in Atomic and Molecular Physics at Wuhan Institute of Physics and Mathematics, Chinese Academy of Sciences, Wuhan, in 2008. Her major field of study is optoelectronics and structural stress analysis in IRFPA.