



Sensorless speed control of a laboratory fabricated SPM-BLDC motor prototype

PINAKI MUKHERJEE*, SOURABH PAITANDI and MAINAK SENGUPTA

Department of Electrical Engineering, Indian Institute of Engineering Science and Technology, Shibpur, India
e-mail: pinaki.mukherjee.besus@gmail.com; sourabh350@gmail.com; msg@ee.iests.ac.in

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Abstract. This paper presents a new sensorless speed control technique for a laboratory-fabricated PM-BLDC motor prototype. The technique utilizes 3rd harmonic components of phase-induced *emfs* to estimate rotor-position pulses and corresponding speed signal. The two-loop control technique employs PI controllers, feed-forward voltage principles and an estimated average DC-link current. Results are presented in detail for different intermediate stages.

Keywords. Position sensorless control; BLDC; 3rd harmonic; Synchronisation technique; Speed estimation; Average DC link current estimation; Speed control.

1. Introduction

This paper presents a state-of-the-art technique for the position and speed sensorless control of a closed-loop Brush-less DC (BLDC) drive. Obtaining accurate rotor position information is necessary for both open-loop and closed-loop control [1, 3, 4]. The challenges associated with shaft-mounted position/speed sensors [5] include operational failure, asymmetric placement of position sensors, reduced reliability of operation, and mechanical faults.

To address these challenges, the paper proposes a technique for estimating rotor position information from the feedback voltage and current signals [4] using the 3rd harmonic component of phase *emfs*. This method [6, 7] is more reliable, cost-effective, and suitable for a Surface-mounted Permanent Magnet (SPM)-BLDC motor with variable speed operation. The 3rd harmonic *emf* signal has lower filtering requirements compared to other back *emf*-based methods and is free from PWM switching frequency-induced noise [6, 7]. The paper also presents a synchronisation technique for the estimated rotor-position pulses with the line *emfs* to ensure the stability of the motor under all conditions. An appropriate speed estimation technique has also been implemented utilizing those estimated position pulses.

Overall, the proposed position sensorless control scheme is a novel contribution to the field of BLDC motor control. The technique has been implemented on a laboratory-fabricated 0.75 hp, 4-pole, 1500 r.p.m. SPM-BLDC motor prototype.

2. Position sensorless closed-loop speed control

To implement a position sensorless strategy, at first, the rotor-position pulses are estimated based on 3rd harmonic *emf* integration method with proper synchronisation technique. After that, using these estimated position pulses, the speed of the motor is estimated. Finally, using these position pulses and speed signal, the closed loop speed control scheme is implemented.

The closed loop speed control (CLSC) consists of an outer speed control loop (SCL) and an inner current control loop (CCL) [8] as shown in figure 1. The speed-loop is conventionally based on a PI-controller while for the inner current-loop is based on DC-link current feedback [10]. In this case, the DC-link current is estimated from the phase current signals. As the reference and feedback current signals both are DC, the PI-controller based current loop design and its tuning is easier.

2.1 Position estimation: 3rd harmonic *emf* integration based technique

A 3rd harmonic *emf* integration based position estimation technique [6, 9] for a SPM-BLDC motor has first also been implemented here. The summation of the three stator phase voltages requires access to the neutral point of the stator. The method implemented here is based on the fact that in symmetrical three phase Y-connected motor with trapezoidal air gap flux distribution, the summation of the three stator phase voltages results in an elimination of all fundamental and $6n \pm 1$ components and only the zero sequence triplen components ($3n$) remain.

*For correspondence

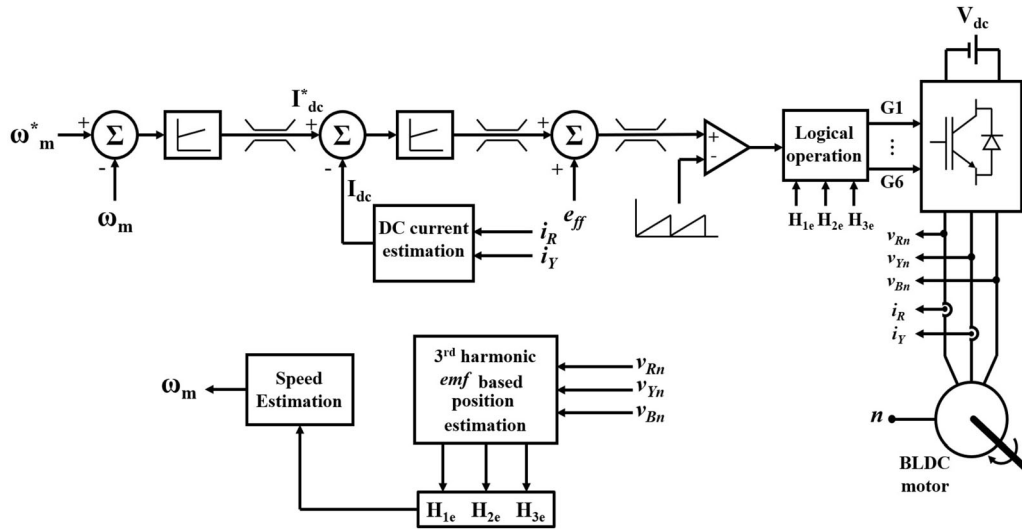


Figure 1. Schematic for the position sensorless closed loop speed control technique of a SPM-BLDC motor using an estimated DC current signal (AQ: Fig. should be written as figure).

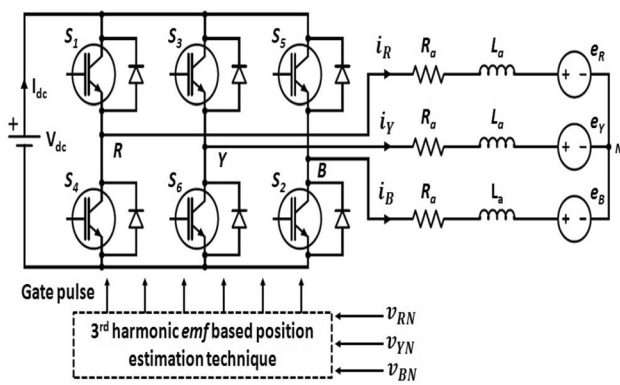


Figure 2. Equivalent circuit model of a SPM-BLDC motor along with the controlled 3-phase inverter.

The most important idea is that the zero sequence emf components with the 3rd harmonic emf (e_3) can be used to generate rotor-position information pulses with the help of sequential and combinational logic, based on the principle of inverter device commutation.

LPF ($\omega_c=500\text{Hz}$) used to reduce high frequency and switching frequency components from 3rd harmonic voltage.

HPF is used to reduce DC offset voltage by 6.66% of rated 3rd harmonic frequency (150 Hz). By integrating this voltage we obtain third harmonic flux linkage (λ_3)

The overall TF $T(s) = \frac{\lambda_3(s)}{v_3(s)}$ can be expressed as,

$$T(s) = \frac{1.95}{1 + s(318.3\mu)} \cdot \frac{s(15.92m)}{1 + s(15.92m)} \cdot \frac{1}{s + 32}$$

2.1.1 Generation of commutation signal: To generate commutation signal (CS), λ_3 is fed to a ZCD. To avoid

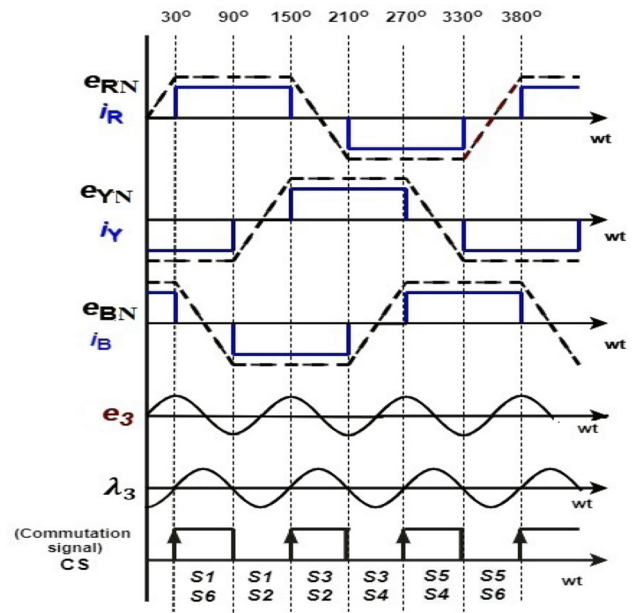


Figure 3. Notional waveforms of phase induced emfs and phase currents, 3rd harmonic induced emf, 3rd harmonic flux linkage and corresponding converter switching sequences for a BLDC motor corresponding to figure 2 [6].

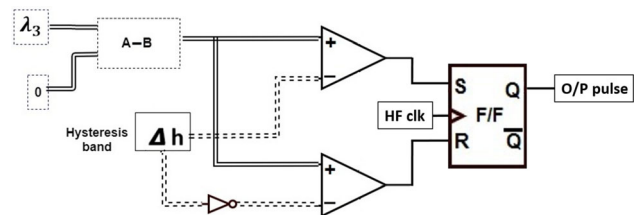


Figure 4. Hysteretic comparator based ZCD used to generate commutation signal.

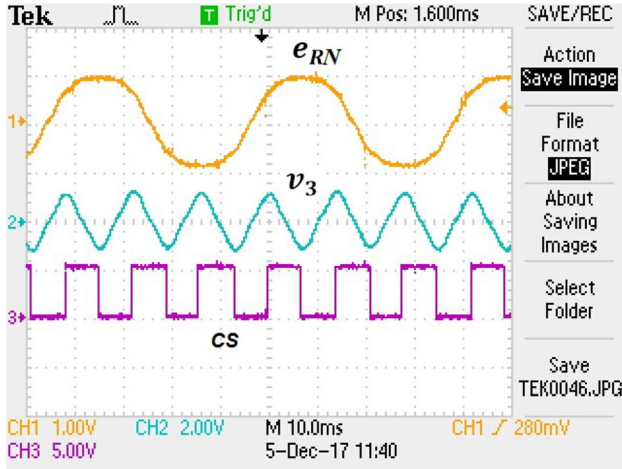


Figure 5. Experimental waveforms of R-phase induced emf (e_{RN}) and 3rd harmonic voltage (v_3) and commutation signal (CS).

multiple zero crossings, a SR flip-flop based comparator (with hysteresis band, figure 4) has been used here.

CS signals are used to generate rotor-position information pulses.

2.1.2 Estimation of rotor-position information pulses: The rotor-position information pulses are estimated from the CS using 2 sets of 3-bit Johnson Ring-Counter (JRC) and combinational logic.

$$H1_e = X2\bar{Y1} + \bar{X2}Y1, H2_e = X1\bar{Y0} + \bar{X1}Y0,$$

$$H3_e = X0Y2 + \bar{X0}Y0$$

Figure 6 shows the experimental waveforms of JRCs output pulses ($X2, Y2$), $H1_e$ and e_{RY} .

Now, using the estimated $H1_e, H2_e$ and $H3_e$, the appropriate logic pulses of the 3-phase VSI devices (six) have been generated, following, $Q_1 = H1_e\bar{H3}_e, Q_4 = \bar{H1}_eH3_e, Q_3 = \bar{H1}_eH2_e, Q_6 = H2_e\bar{H1}_e, Q_5 = \bar{H2}_eH3_e,$

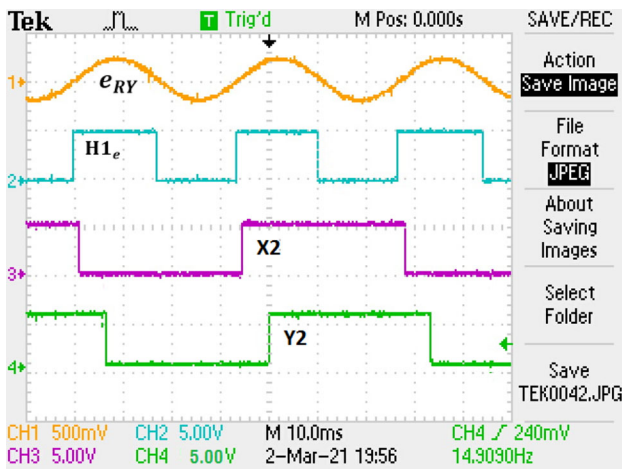


Figure 6. Experimental waveforms: $e_{RY}, H1_e, X2$ & $Y2$.

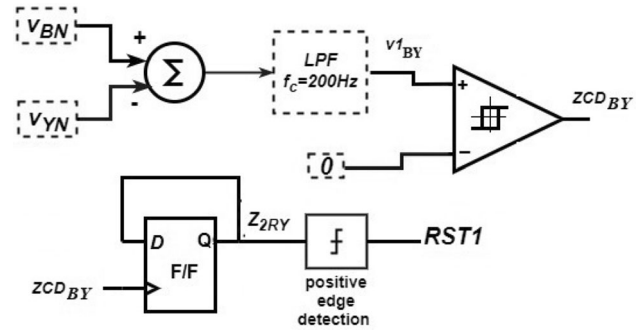


Figure 7. Logic and corresponding waveforms to generate $RST1$ pulse for position pulse synchronisation.

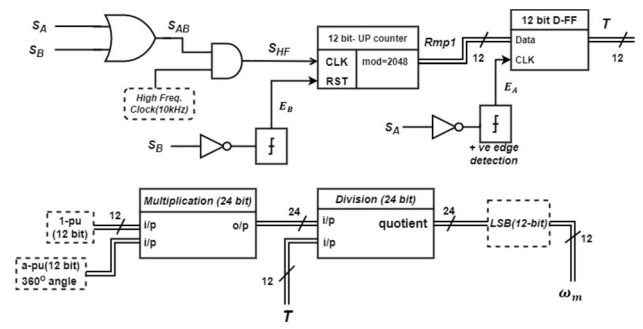


Figure 8. Schematic of speed estimation logic.

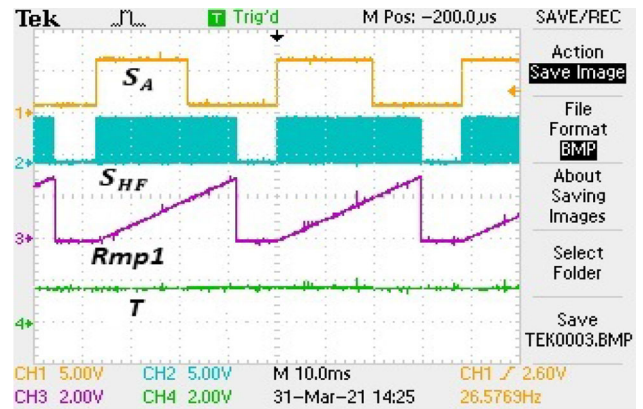


Figure 9. Experimental waveforms: $S_A, S_B, S_{HF}, Rmp1, T$ & ω_m for speed estimation.

$Q_2 = H2_e\bar{H3}_e$. The VSI is operated in synchronism with the rotor position and speed in closed loop mode, using logic-pulses as mainswitching pulses.

2.1.3 Synchronisation of position information pulses with the line emfs: The estimated position information pulses must be synchronised with the line emfs using external signals. The $X_{2,1,0}$ JRC can be reset using e_{BY1} emf and a low pass filter (LPF) at 200 Hz. $RST1$ and $RST2$

pulses ensure $H1_e$, $H2_e$ and $H3_e$ remain in synchronism with line induced emfs during sudden speed transients.

2.2 Speed estimation

Speed estimation [7] of a motor is essential for the closed-loop position sensorless control operation. We know that, angular speed, $\omega_m \triangleq \frac{\Delta\theta_m}{\Delta t} = \frac{2\pi m}{T}$. The value of time period T is calculated from the estimated position information pulses, which are OR'ed and then 'AND'ed with a high frequency pulse (HFP). The SHF pulse train is used as the clock input of an up-counter, which is reset by the falling edge of SB.

A low pass filter (LPF) with a cut-off frequency (f_c) of 100 Hz is introduced in the feedback loop to reduce the speed ripple.

2.3 Closed loop speed control of the BLDC motor

2.3.1 Estimation of average DC-link current [10]: The modulus of the individual current signal has been generated using a multiplexer and comparator pair with a small hysteresis band. The estimated current signal is proportional to the magnitude of the moving average over a switching time period of the DC-link current ($\langle i_{dc} \rangle_{T_{sw}}$). Feed-forward voltage is added to the PI-controller output and compared with a saw-tooth to generate the PWM signal, which is then 'AND'ed with the main logic pulses of VSI upper switches.

2.3.2 Modelling of a SPM-BLDC motor: The dynamic machine model [3] of a SPM-BLDC motor, during each 60° interval of VSI conduction, is described by in Laplace domain,,

$$\begin{aligned} V_{is}(s) &= 2(R_a + sL_d)I_{dc}(s) + E_b(s) \\ \Rightarrow V_{is}(s) &= 2(R_a + sL_d)I_{dc}(s) + K_b\Omega_m(s) \end{aligned} \quad (1)$$

$$M_e(s) = K_t I_{dc}(s) \quad (2)$$

$$M_e(s) = (Js + B)\Omega_m(s) + M_l(s) \quad (3)$$

Based on (1) to (3) the CCL and SCL have been designed

The details of the two-loop controller as implemented on the SPM-BLDC motor is given in table 1. The bandwidth of

Table 1. Details of the BLDC controllers (in figure 1).

Item	Value	Item	Value
K_{pc}	3.668	$K_{p\omega}$	8.042
K_{ic}	625.2 s^{-1}	$K_{i\omega}$	2.61 s^{-1}
BW_{c-lp}	500 Hz	$BW_{\omega-lp}$	10 Hz
e_{ff}/ω_m	26.54m	K_{inv}	84

current loop is 500Hz while the speed loop bandwidth is 10 Hz.

2.4 Results of the closed loop control

In this section, the experimental waveforms along with the experimental readings have been presented.

Figure 10 to figure 11 shows the simulated and experimental waveforms of the BLDC motor under CL control in the steady state (SS). For CL operation the estimated position pulses, $EPP (H1_e, H2_e \& H3_e)$ and speed signal (ω_m), estimated from position information, have been utilised.

The steady-state waveforms are taken at the rated speed of 1500 r.p.m (i.e., 157 rad(mech.)/s) with rated load (560W). Figure 10 shows the experimental waveforms of estimated position pulse ($H1_e$), R and Y-phase voltage (v_{RN} & v_{YN}) with a rms value of 164 V for the both cases. The

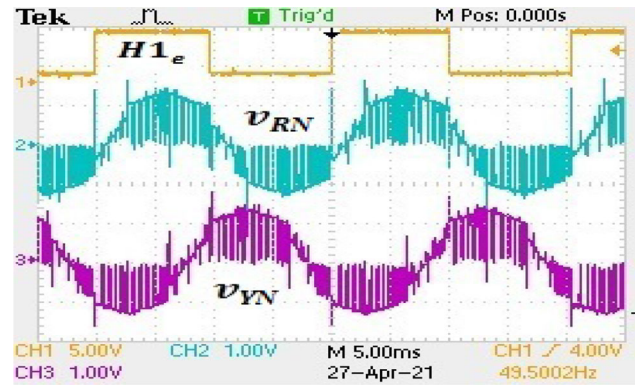


Figure 10. Experimental waveforms under closed loop control: Estimated position pulse ($H1_e$), R & Y-phase voltages (v_{RN} & v_{YN}) at rated speed (1500 r.p.m or 157 rad (mech.)/s) with rated load torque (3.56 N-m).

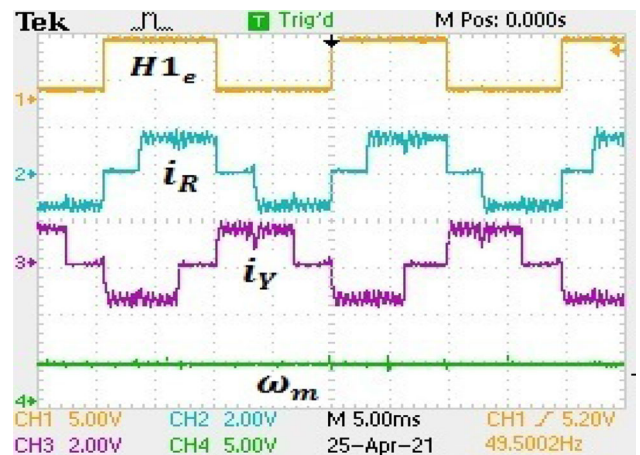


Figure 11. Experimental waveforms under closed loop control: Estimated position pulse ($H1_e$), & Y-phase current (i_R & i_Y) and estimated speed (ω_m) at rated speed (1500 r.p.m) with rated load torque (3.56 N-m) on the SPM motor.

phase current waveforms i_R & i_Y are quasi-square in shape with a *rms* value of 1.4 A (rated load current).

3. Conclusions

This paper presents a novel position sensorless closed-loop speed control method SPM-BLDC motor. The proposed method uses a 3rd harmonic emf integration based rotor-position estimation method, which is synchronized with line *emfs* to maintain transient stability during speed and load variations. A speed estimation method is also implemented using position pulses, suitable for low-resolution rotor-position pulses. The closed-loop control strategy involves outer speed and inner current loops with feed-forward voltage control and PI-controller for achieving fast response. The study highlights the synchronisation procedure of the rotor-position pulses, speed estimation technique, estimation of average DC-link current signal used as current feedback, and successful implementation in a closed-loop drive, which are hardly available in published literature.

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