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A new very high output resistance FVF based class-A super-cascode CCII

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Abstract. Second generation current conveyor (CCII) is a versatile fundamental building block that is used nowadays for designing of almost all kinds of current mode devises. A wide variety of CCII configuration offering diverse characteristics have been proposed in literature. However, not much effort has been put to improve the output resistance of this block. High output resistance is a very essential parameter that makes CCII a versatile block to be used in integrated circuits, without affecting its performance parameters. In this paper, an extensive survey has been carried out to explore high performance CCII topologies. Among these configurations flipped voltage follower (FVF) based class-A CCII architecture has been chosen because of its compact design, low voltage and current/voltage matching characteristics. Output resistance of this configuration has been increased by using super-cascode (SC) configuration and replacing the biasing circuitry by low voltage cascode current mirror. Small signal analysis of the proposed circuit has been carried out to mathematically validate the improvement achieved by this circuit. The proposed FVF based class-A SC-CCII offers very high output resistance while maintaining all the characteristics of FVF based class-A CCII. However, a small sacrifice has to be made in the required in supply voltage of the proposed design. The proposed CCII is simulated in LtSpice using 0.18 μm CMOS technology and is compared with various CCII configurations available in literature. The simulated results validate the high performance operation of the proposed SC-CCII and show that this block offers around 70 times increase in output resistance. The characteristic of this proposed SC-CCII makes it a versatile block to be used in wide applications with diverse characteristics.

Keywords. Current conveyor; flipped voltage follower; class-A; super-cascode; input and output resistance.

1. Introduction

The conventional operational amplifier (opamp) has been predominant block in analog and signal processing domain. Since the inception of idea of opmap in 1940, it has been extensively used for circuit realization and signal processing tasks. Researchers have explored its utility in designing almost each and every analog, digital and mixed mode circuit that is based on voltage mode (VM) operation. Though, it has been proved to be an effective and ingenious component in designing of circuits, however, it faces some major limitations like restricted slew rate and fixed gain bandwidth product (GBP) [1]. These features limit its performance at high frequencies.

To overcome these drawbacks, current mode (CM) approach has been introduced by researchers. In this methodology, active variable is current instead of voltage. The circuits designed using this approach do not have any high impedance node and thereby operate at high frequencies. Moreover, operation of these circuits are not restricted by GBP limitations [2]. In literature, various building blocks have been devised time to time based on CM approach. Current conveyor (CC) is one of the important blocks amongst them and was proposed in 1970 by Sedra and Smith [3]. It has been observed that CC show considerable improvements in bandwidth, power consumption, signal linearity and slew rate. Therefore, a lot of circuits have been proposed using CCs since 1970. Later on different generations of CCs have been introduced, based on its terminal characteristics [4, 5]. Due to the versatility and usage in designing basic circuits, second generation CC (CCII) has been chosen as a topic of study and investigation in the paper.

Since the introduction of CCII by Sedra and Smith in 1970, a dozen of CCII structures have been introduced in literature. Some of them are Wideband CCII [6], Controlled CCII [7], Second generation differential voltage current conveyor (DVCCII) [8], Inverting second generation

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current conveyor (ICCII) [9], Fully differential second generation current conveyor (FDCCII) [10], Dual-X current conveyor (DXCCII) [11], Class A CCII [12], Fully balanced current conveyor II (FBCCII) [13], Voltage and current gain second generation current conveyor (VCG-CCII) [14], CCII with low parasitic resistance R_x [15], Current controlled fully balanced second generation current conveyor (CFBCCII) [16], Differential current conveyor (DCCII) [17].

In this paper, basics of CCII have been presented in next the section. Based on the functionality and importance of the structure, some of high performance CCII topologies have been chosen for analysis and comparison. All these topologies have been discussed in detail in section 3. It has been analysed that not much work has been done to improve the output resistance of these configurations. High output resistance is very essential feature of CCII, especially when it has to be used in cascaded devices. Motivation behind this work has been to design a high performance CCII having high output resistance that can avoid any loading effect irrespective of the circuit it is used. In section 4, development of a new FVF based class-A super-cascode CCII offering very high output resistance has been presented. This CCII has been designed using super-cascode configuration at output terminal of FVF based class-A CCII and replacing the biasing circuitry with low voltage cascode current mirror. Small signal analysis has been carried out to mathematically analyse the improvement obtained in the configuration. Section 5 summarizes the simulation results of the proposed CCII and other CCII configurations discussed in section 3. These results have been obtained using LtSpice 0.18 μm technology. Finally, in section 6, the conclusions are provided.

2. Second generation current conveyor (CCII)

A second generation current conveyor (CCII) is a 3-port building module. Figure 1 shows its block diagram depicting various input and output nodes. CCIIs are generally characterized by terminal Y, which ideally has infinite input resistance. In a CCII, if a signal is applied at Y port, an identical voltage appears at terminal X. Similarly, port Z which possesses high output resistance (ideally infinite), reflects equal amount of current (I_Z) as fed at terminal X [4].

The port characteristics of CCII are expressed as:

$$\begin{bmatrix} V_X \\ I_Y \\ I_Z \end{bmatrix} = \begin{bmatrix} 0\,1\,0 \\ 0\,0\,0 \\ \pm 1\,0\,0 \end{bmatrix} \begin{bmatrix} I_X \\ V_Y \\ V_Z \end{bmatrix} \quad (1)$$

The above matrix equation describes two types of CCII: (i) CCII+ and (ii) CCII-. Basically these CCIIs are categorized by the direction of current I_Z. In CCII+ polarity of

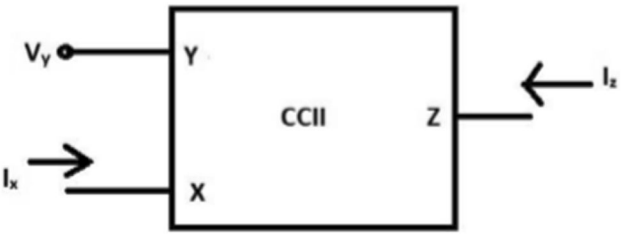

Figure 1. CCII block diagram.

I_Z is same as that of I_X and in CCII- this polarity gets reversed [4]. Current conveyors have been widely used in applications based on filtering. Several efforts and studies have been made in recent years to improve the design of universal filter. One such implementation involves use of three circuits of multi-output current controlled conveyors [16]. All filters namely low pass, bandpass, highpass, notch and all pass filters can be designed using current conveyors. Moreover, recently the possibilities of efficiently implementing floating inductors and inductors connected to ground using current conveyors is being explored [2]. Other important applications of CCII are: current amplifiers, voltage to current convertors, voltage and current amplifiers, integrators and differentiators, current summers, instrumentation amplifiers, full wave precision rectifiers, oscillators, etc. [3–5].

3. Various CCII architectures present in literature

3.1 *Wideband CCII*

WIdeband CCII was proposed by Cha and Watanabe in 1996 [6]. For signal processing under current mode using low power operation, translinear loop based wideband CCII was proposed by Ismail and Soliman in [18]. It has been observed that these translinear circuits show an outstanding current mirroring behaviour at port Z from port X for a wide range of input current. Though, their voltage mirroring property at port X from port Y is not that good and possess a high offset voltage.

The circuit of translinear loop based wideband CCII is shown in figure 2. This circuit consists of two differential pairs (M2-M4 and M1-M3). Here, the MOSFETs M3-M6 constitute first generation current conveyor (CCI). Assuming that differential pairs are perfectly matched, CCI operation of MOSFETs M3-M6, imitates the potential at source voltage of MOSFET M4 at the source terminal of M3. This arrangement ensures current across MOSFET M4 to be same as that flowing across M3 and make it independent of voltage Vy, applied at gate terminal of M2. Moreover, equal currents across M1 and M2 (due to similar biasing of MOSFETs M7 and M8) and their similar source

potentials lead to transfer of voltage Vy quite successfully at node X.

Furthermore, this arrangement causes current at node X to be mirrored at node Z without any help from current mirrors. Moreover, it is noticed that Vy is exactly followed by Vx and Vz is always greater than ($V_{ds2,sat}$ + Vy) for legitimate operation.

The circuit shown in figure 2, does not hold any high impedance node and thereby offers wide bandwidth. This wideband CCII circuit consists of a few transistors and has a very compact design. It consumes low power and is able to operate for a very wide range of frequencies. This wideband CCII is extensively used in high frequency applications, in designing of universal filters, sinusoidal oscillators, etc.

3.2 *Flipped voltage follower based class-A CCII*

Class-A CCII circuit was proposed by Naik *et al* in 2010 [12]. The architecture of this CCII is based on flipped voltage follower (FVF) current mirror and is shown in figure 3. FVF is basically an enhanced buffer cell that is widely employed for low voltage operations. Applications of FVF include multipliers, CCIIs, mixers, etc.

In CCII circuit shown in figure 3, MOSFETs MN1 and MN5 form the FVF cell. The required biasing current is provided by MOSFET MP1 and required gate voltage at MN5 is obtained via diode connected MOSFET MN4. Here, MOSFETs MN6 and MN7 are connected as current sink load. In this circuit, since MOSFETs MP1, MP2 and MP3 have same gate and source voltages, therefore they have same drain currents (say Ib). The architecture of this circuit ensures the same current (Ib) to flow across MN6 as well. This finally leads to similar current at nodes x and Z, that is Iz=Ix. Furthermore, this leads to Vx=Vy.

It is readily observed that complexity of the circuit is quite less and a precise voltage mapping is obtained from Y to X terminal. In this class A CCII circuit, current mirroring from node X to node Z is also satisfactory. Furthermore, this circuit offers numerous advantages like compact design, good slew rate, high output impedance and quite good operating range for both current and voltage. This circuit can readily be used to implement different types of filters, current amplifiers, instrumentation amplifiers, etc. [3, 12, 19].

3.3 *Controlled current conveyor II (CCCII)*

The controlled CCII (CCCII) was proposed by Fabre *et al* in 1995 [7]. CCCII has 3 nodes X, Y and Z. Its terminal current and voltage equations are given as:

$$\begin{bmatrix} V_X \\ I_Y \\ I_Z \end{bmatrix} = \begin{bmatrix} \mathrm{R}_X & 1 & 0 \\ 0 & 0 & 0 \\ \pm 1 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_X \\ V_Y \\ V_Z \end{bmatrix} \tag{2}$$

The circuit of CCCII is shown in figure 4. In this configuration one can electronically change the resistance seen at X terminal, hence the name controlled current conveyor (CCCII) [4, 5]. The circuit of CCCII mainly consists of a translinear loop (M1-M4) and a few current mirrors. Routine analysis of the circuit, considering current mirror action at different places, offers:

$$I_{M12} = I_b + I_X \tag{3}$$

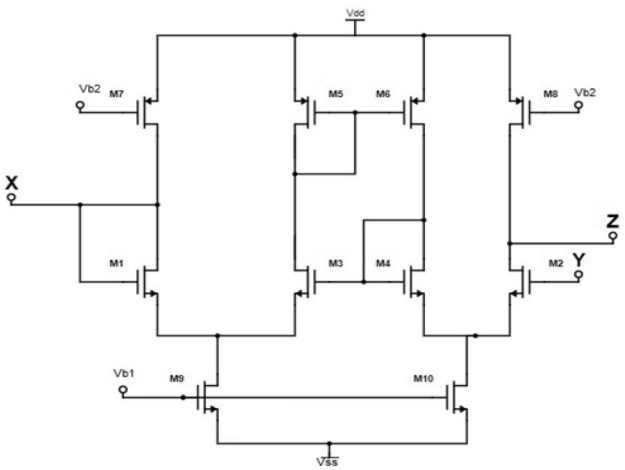

Figure 2. Wideband CCII circuit [18].

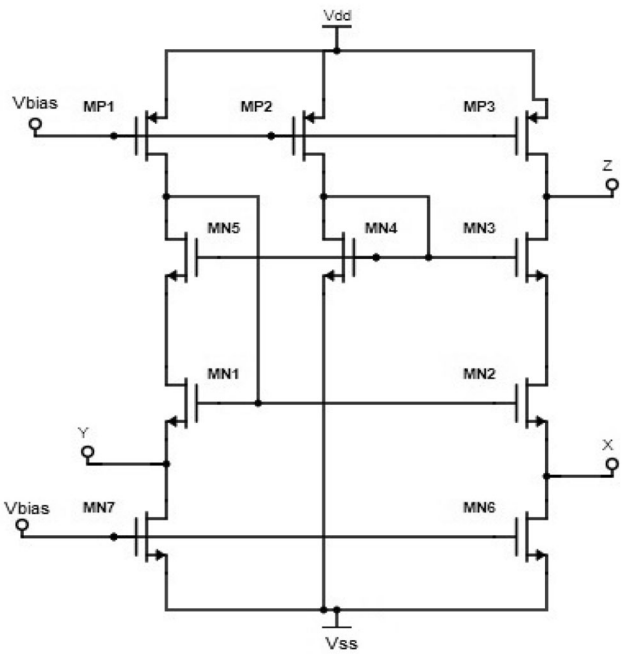

Figure 3. FVF based Class-A CCII [12].

here, I_b is the biasing current flowing across MOSFETs M8 and M9 and Ix is current injected in terminal X. Now, current mirror formed by MOSFETs M12 and M13 leads to current at Z terminal equal to I_X. Furthermore, the circuit configuration leads to Vx=Vy.

The circuit offers numerous advantages like: it requires low supply voltage, it operates on a wide range (for both current and voltage), it has good slew rate and it also offers low input impedance. This circuit can be used in high frequency applications, like in designing universal filters, sinusoidal oscillators, etc. [3, 5].

3.4 *CCII implementation with low parasitic resistance Rx*

Translinear loop based CCII shows the best high frequency performance while offering a high control on the design characteristics. To further improve the operating frequency of these translinear loop based CCII, a new implementation of CCII with low parasitic resistance at node X (Rx), was proposed by Dorra Sellami *et al* in 2004 [15]. Its circuit is given in figure 5.

Here, signal path for current has been separated from CCII current conveying path. This has been done by generating a new current transfer signal path between X and Z terminals, with the help of a current mirror. A voltage amplifier is used to lower the impedance at port X. Care has been taken to make the gain of this voltage amplifier dependent on controlling current of translinear loop. This helps in providing greater flexibilities to the designed structure. The architecture of Controlled CCII is shown in figure 5, mainly consists of a translinear loop (M1-M4) and a few current mirrors. Due to current mirror configuration, current through MOSFETs M9, M10 & M15 is same and current through MOSFETs M11, M12, M13 & M14 is also same. Moreover, same current is achieved in M7-M8 and M5-M6. These current mirrors and translinear loop ensure Iz=Ix and Vx=Vy.

Along with providing low parasitic resistance at port X, this CCCII offers numerous advantages like low power consumption, low input impedance and very good performance at high frequencies. This circuit can be used for design applications operating at high frequencies, including current controlled oscillators and fully integrable tunable band pass filters, etc.

3.5 *Differential CCII (DCCII)*

DCCII was first proposed by Metin *et al* in 2012 [17]. It has a unique current differencing property extracted from CCII's conventional models. DCCII architecture has been presented in figure 6 [17]. It has 3 input terminals (X_P, X_N and Y) and 1 output terminal (Z). In DCCII, difference of current at terminals X_P and X_N is replicated at Z terminal. Matrix equation describing the port behavior of DCCII is given by Eq. (4).

$$\begin{bmatrix} V_{XN} \\ V_{XP} \\ I_Z \\ I_Y \end{bmatrix} = \begin{bmatrix} 001 \\ 001 \\ 1-10 \\ 00\,0 \end{bmatrix} \begin{bmatrix} I_{XP} \\ I_{XN} \\ V_Y \end{bmatrix} \tag{4}$$

DCCII architecture is constituted by 3 sub-circuits. Mixed translinear loop formed by MOSFETs M8–M13 forms the core section of DCCII architecture. This loop helps in replicating the potential of terminal Y to other 2 inputs terminals (X_N and X_P). Current differencing is achieved through MOSFETs M14-M21. This sub-circuit replicates the difference of current flowing at X_N and X_P at terminal Z. Biasing required by the complete circuit is done by MOSFETs M1-M7.

This architecture of DCCII offers various advantages like providing an additional voltage terminal with high input resistance that makes it suitable for cascading operations.

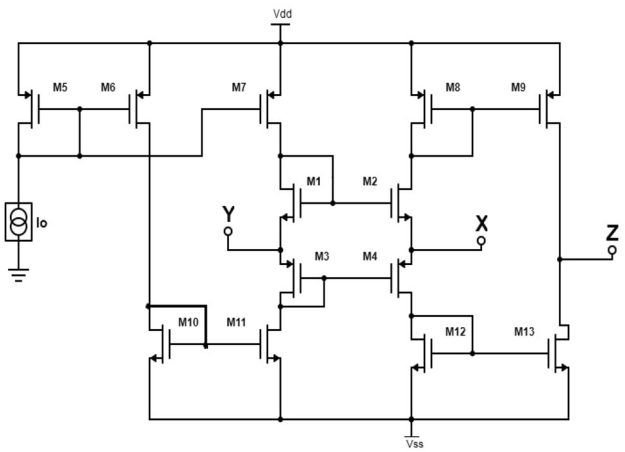

Figure 4. Current controlled conveyor (CCCII) [7].

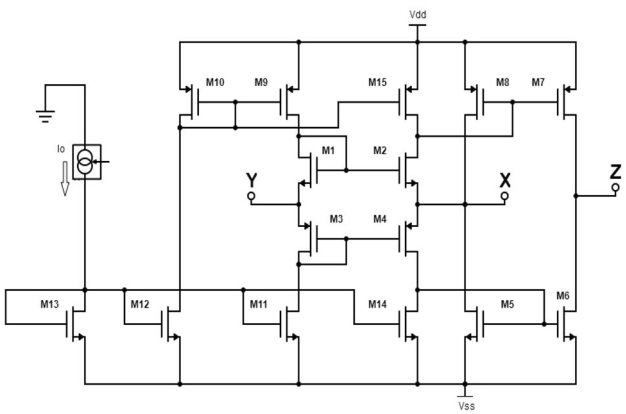

Figure 5. CCII with low parasitic resistance at node X [15].

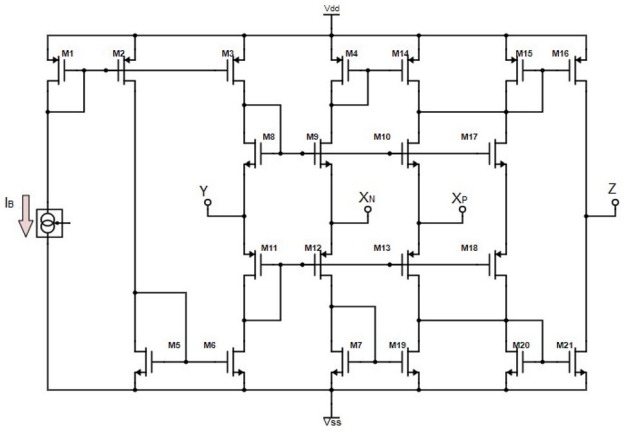

Figure 6. DCCII [17].

DCCII has been used in numerous applications like in square wave generators, various amplifiers, etc. [17].

4. Proposed FVF based class-A super-cascode CCII (SC-CCII)

FVF based class-A CCII shown in figure 3 is a compact current conveyor capable of performing at low supply voltage. It has a simple and compact structure that provides a precise voltage mapping from Y to X terminal. It also offers a satisfactory current mirroring from node X to node Z. Furthermore, this circuit offers numerous advantages like good slew rate, high output impedance and quite good operating range for both current and voltage.

However, output impedance offered by this circuit is not very high. This impedance can be increased by employing negative feedback. Super cascode configuration proposed in [20] can be used to improve the output resistance, without increasing the required supply voltage. Complete circuit of the proposed FVF based class-A super cascode CCII (SC-CCII) is shown in figure 7. In this circuit, MOSFETs MN8 and MN9 constitute the super cascode configuration and form the biasing circuitry for these super-cascode MOSFETs. Here, MN9 is the output cascode MOSFET. MN8 helps in driving the gate terminal of this cascode MOSFET, by supplying the required polarity of the signal at its gate terminal [20, 21]. MOSFETs MP4, MP5, MP11 and MP12 help in proper biasing of these MOSFETs. In the proposed configuration, to achieve the required goal, biasing circuitry of FVF based class-A CCII has been replaced by low-voltage cascode current mirror [22]. This configuration has been chosen to obtain high output resistance of biasing circuitry when seen from 'Z' terminal. This is required to get the expected improvement in output resistance, as resistance of biasing circuitry will appear in parallel. Proposed configuration helps in achieving very high output resistance at the output terminal, while maintaining the class-A response of FVF based CCII. However, this circuit needs a slightly higher supply voltage due to cascode configuration of current mirror. To maintain nowadays demand of low supply voltage operation, in the proposed configuration low voltage cascode current mirror has been used. This current mirror helps in attaining high output resistance with small sacrifice in voltage headroom [22]. The improvement achieved in output resistance of the proposed architecture is directly proportional to the gain provided by feedback path formed by cascode MOSFET MN9 and driving MOSFET MN8. Mathematical analysis for this circuit has been presented in sub-section 4.1.

4.1 *Output resistance*

Equivalent small signal model for deriving output resistance of the proposed CCII configuration has been shown in figure 8.

The low-frequency small-signal model for calculating output resistance of the proposed Class-A SC-CCII, looking from Z terminal (Rz) is shown in figure 8. This equivalent circuit has been drawn considering zero input signals at Y and X terminals. For this, the signal sources present at Y and X terminals have been replaced by their effective internal resistances. Here, g_m represents transconductance and r_0 represents small signal output resistance of the corresponding MOSFET. R_{O_CAS} represents the output resistance of cascode current mirror and can be given as:

$$R_{O\_CAS} = r_{0P5} + r_{0P12} + g_{mP5} r_{0P5} \cdot r_{0P12} \cong g_{mP5} r_{0P5} \cdot r_{0P12} = g_{mP} r_{0P}^2 \quad (5)$$

Above equation has been derived assuming all PMOS transistors forming current mirror configuration are symmetrical and considering for a MOSFET, $g_m r_0 >> 1$ [23].

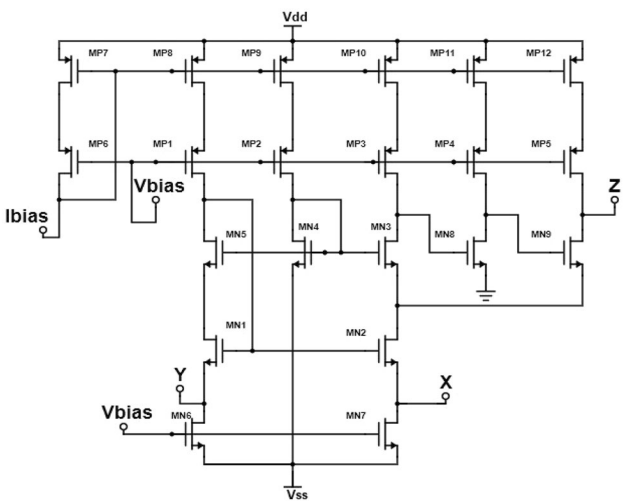

Figure 7. Proposed FVF based class-A super-cascode CCII.

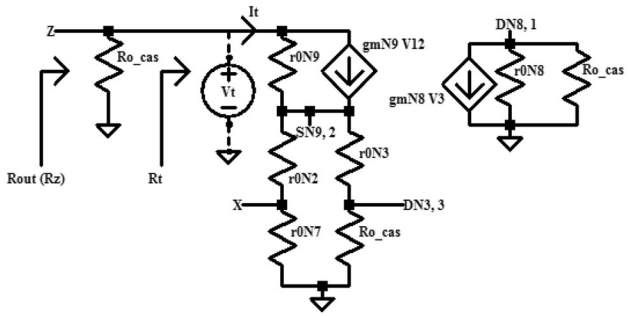

Figure 8. Low-frequency small-signal model for calculating Rz of proposed Class-A SC-CCII.

In the circuit, terminals marked DN8 and DN3 are the drain terminals of MOSFETs MN8 and MN3, respectively. SN9 node represents source terminal of MOSFET MN9. All these nodes have been numbered as well, in order to write mathematical expressions related to the circuit with more clarity. Voltage difference between any 2 terminals is marked as V_{ij}, where 'i' and 'j' represents the 2 nodes.

From small signal circuit shown in figure 8,

$$R_Z = R_{O\_CAS} || R_t \tag{6}$$

To calculate R_t, a test voltage source (V_t, shown dotted in figure) has been connected at Z terminal and analysis has been carried out to find current I_t. Routine analysis of this small signal model gives equations as follows:

$$I_t = g_{mN9} V_{12} + \frac{V_t - V_2}{r_{0N9}} \tag{7}$$

$$g_{mN8} V_3 = -\frac{V_1}{r_{0N8} || R_{O\_CAS}} \approx -\frac{V_1}{r_{0N8}} \tag{8}$$

$$\begin{aligned} V_2 &= I_t \cdot \{(r_{0N2} + r_{0N7}) || (r_{0N3} + R_{O\_CAS})\} \\ &\approx I_t \cdot (r_{0N2} + r_{0N7}) \end{aligned} \tag{9}$$

$$\begin{aligned} V_3 &= R_{O\_CAS} \cdot \left(\frac{r_{0N2} + r_{0N7}}{r_{0N2} + r_{0N7} + r_{0N3} + R_{O\_CAS}} \right) \cdot I_t \\ &\approx (r_{0N2} + r_{0N7}) \cdot I_t \end{aligned} \tag{10}$$

Eq. (9) shows that if R_{O_CAS} is very high, then no current will flow in this branch and $V_3 \approx V_2$.

Simplifying Eqs. (7) – (10), Rt can be obtained as:

$$\begin{aligned} R_t = \left| \frac{V_t}{I_t} \right| &= r_{0N9} + r_{0N2} + r_{0N7} + g_{mN9} r_{0N9} \cdot (r_{0N2} + r_{0N7}) \\ &\quad + g_{mN9} r_{0N9} \cdot g_{mN8} r_{0N8} \cdot (r_{0N2} + r_{0N7}) \end{aligned} \tag{11}$$

Considering for a MOSFET, $g_m r_0 >> 1$ [23], Eq. 11 can be simplified to:

$$R_t \approx g_{mN9} r_{0N9} \cdot g_{mN8} r_{0N8} \cdot (r_{0N2} + r_{0N7}) \tag{12}$$

Combining Eqs. (5), (6) and (12), R_Z can be calculated as:

$$R_Z = g_{mP} r_{0P}^2 || g_{mN9} r_{0N9} \cdot g_{mN8} r_{0N8} \cdot (r_{0N2} + r_{0N7}) \tag{13}$$

Eq. (13) shows that output resistance seen from terminal Z, looking towards base circuit observes an improvement of approximately $g_{mN9} r_{0N9} \cdot g_{mN8} r_{0N8}$, due to super cascode configuration and that looking towards biasing circuitry observes an improvement by a factor of $g_{mP} r_{0P}$. The component with lower value will dominate R_Z. This improvement is very significant and will help the circuit designers to use CCII effectively in their devices. Further, it has been observed that if biasing circuitry has very high output resistance, then super cascode configuration used in the proposed CCII can provide output resistance in hundreds of MΩ. Since a lot of research has been done for improving output resistance of a current mirror, various current mirror configurations with high output resistance are available in literature [21, 24]. Choice of the current mirror to be used will depend on the requirement of the circuit designer and will greatly help in improving the overall output resistance of the proposed CCII architecture.

5. Simulation results and analysis

In this section, simulation results of various CCII architectures have been presented. All the CCII architectures have been simulated in Ltspice using 0.18μm CMOS technology. To get a fair comparison among the results of different circuits, they have been simulated using same technology with W/L ratios of all MOSFETs of various architectures are summarized in table 1.

5.1 *DC analysis*

In this sub-section, DC analysis of the proposed CCII architectures has been shown and its comparison with other CCII architectures reported in literature has been presented. The current characteristics of the proposed circuit has been analysed by applying a varying DC current at input port X (Ix) and observing the variations in current at output port Z (Iz). The simulation results obtained in this case has been shown in figure 9. From this figure it can be observed that in the proposed CCII, Iz follows Ix with high accuracy for input current range of −500 μA to +500 μA. For comparison with other CCII architectures present in literature and discussed in the paper, DC simulations for these configurations have been carried out using aspect ratios listed in table 1. The operating current range obtained through simulations for these topologies have been mentioned in table 2. It has been analysed that the operating current range is maximum for the proposed FVF (±500 μA) based class-A SC-CCII. Further, curve showing % error in output

current (Iz) of the proposed FVF based class-A SC-CCII has been plotted in figure 10. This curve shows that the proposed CCII works for the entire operating current range with a maximum % error of ±0.9%. This error being maximum at input current (Ix) close to zero due to division by near zero values of Ix.

To verify the voltage operation of the proposed CCII, the variations in voltage at X terminal with that of voltage at Y terminal have been plotted in figure 11. This figure shows that Vx follows quite closely to Vy for a wide range of −500 mV to +500 mV. Similar curves for other CCII configurations have been obtained with the corresponding results tabulated in table 2. These results justify the wide operating voltage range of the proposed CCII architecture. To confirm the tracking of voltage at port X to the voltage applied at port Y, % error in Vx has been plotted in figure 12. This figure shows that Vx closely follows Vy with a maximum % error of ±0.9%. The error being maximum at input voltage (Vy) close to zero due to division by near zero values of Vy.

5.2 *AC analysis*

In this sub-section, AC analysis of the proposed CCII architecture has been presented and comparison with other CCII configurations discussed in the paper has been presented. AC Analysis has been done for a frequency range of 10 Hz to 5 GHz. Frequency plots for current gain and voltage gain of the proposed class-A SC-CCII have been shown in figures 13 and figure 14, respectively. From these curves it is observed that −3 dB bandwidth for the proposed CCII configuration is 20 MHz and 25.43 MHz for current gain and voltage gain, respectively. For comparison, respective bandwidths of other CCII architectures obtained through simulations have been listed in table 2. These values show that bandwidth of the proposed CCII architecture is lower in comparison to other CCII architectures. This is due to the high output resistance of the proposed architecture.

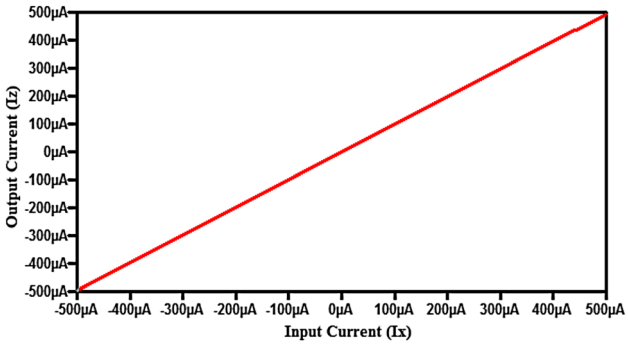

Figure 9. Current characteristics of proposed FVF based class-A SC-CCII.

Main objective of the proposed CCII configuration has been to achieve a good design having high output resistance. Output resistance of the proposed architecture observes a significant boost compared to rest of the high performance architectures discussed in the paper. This improvement achieved in present design can be observed form the output resistance (Rz) waveforms shown in figure 15. This waveform clearly shows that the proposed design offers very high output resistance of the order of MΩ. The improvement observed in output resistance is due to super-cascode configuration used in the proposed configuration. Plot for input resistance looking through X terminal is shown in figure 16. This curve shows that input resistance of the proposed CCII is quite low (1.12 kΩ). Simulations for other CCII configurations have been carried out and the respective values of their output and input resistances have been summarized in table 2. From this table it can be analysed that the proposed architecture significantly increases the output resistance from a few kΩs to MΩ range. This has been the main contribution of the

Table 1. Aspect ratios of MOSFETs of various CCII architectures.

Type of CCII	MOSFET	W/L (µm)	MOSFET	W/L (µm)	MOSFET	W/L (µm)
Wideband CCII [18]	M1-M4	35/1.4	M5-M8, M12	49/3.5	M9-M11	35/2.8
Class A CCII [12]	MP1-MP3	200/1	MN1-MN5	400/1	MN6, MN7	300/3
CCCII [7]	M1, M2	60/0.18	M3, M4	90/0.18	M5, M6	20/0.18
	M7	22/0.18	M8, M9	28/0.18	M10, M11	2/0.18
	M12, M13	17/0.18				
CCII with low parasitic resistance Rx [15]	M1, M2	12/0.35	M3, M4	36/0.35	PMOS current mirrors	18/0.35
	NMOS current mirrors	6/0.35				
DCCII [19]	M11-M13, M18	50/0.35	M1-M3	30/2	M4, M14, M15	30/1
	M16	50/2	M8-M10, M17	20/0.35	M5, M6	10/2
	M7, M19, M20	10/1	M21	20/2		
Proposed FVF based class-A SC-CCII	MP1-MP12	200/1	MN1-MN5	400/1	MN6, MN7	300/3
	MN9	4/1	MN8	16/2		

Table 2. Comparison summary of different parameters of proposed and all CCIIs on various parameters.

Parameters	Wideband CCII [18]	FVF based Class-A CCII [12]	CCCII [7]	CCII with low parasitic resistance Rx [15]	DCCII [19]	Proposed FVF based class-A SC-CCII
Operating range (current)	−150 µA to 150 µA	−120 µA to 120 µA	−250 µA to 250 µA	−300 µA to 300 µA	−200 µA to 200 µA	−500 µA to 500 µA
Operating range (voltage)	−180 mV to 180 mV	−200 mV to 200 mV	−300 mV to 300 mV	−450 mV to 450 mV	−300 mV to 300 mV	−500 mV to 500 mV
Bandwidth (current)	34.05 MHz	120 KHz	1.06 GHz	1.64 GHz	435 MHz	20 MHz
Bandwidth (voltage)	532.5 MHz	12 MHz	1 GHz	2.53 GHz	3.88 GHz	25.43 MHz
Capacitor (C_L)	1 pF	1 pF	1 pF	1 pF	1 pF	1 pF
Slew rate (SR+) (V/µs)	91.67	91.9	95.56	96.49	36.87	90.34
Slew rate (SR−) (V/µs)	91.47	91.2	93.9	93.6	36.35	89.33
Input resistance	149.16 Ω	373.94 Ω	122 Ω	41 Ω	117 Ω	1.12 KΩ
Output resistance	22.56 KΩ	35 KΩ	20 KΩ	18 KΩ	66.7 K	2.44 MΩ
Supply voltage	±2.5 V	±1.1 V	±1 V	±2.4 V	±2.5 V	±1.3 V
Bias voltage (if any)	±1.8 V	1.5 V	–	–	–	0.741 V and −0.8 V
Bias current (if any)	100 µA	–	120 µA	100 µA	400 µA	500 µA

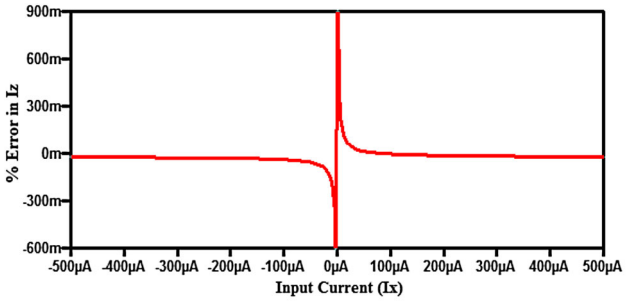

Figure 10. % Error curve for output current (Iz) of proposed FVF based class-A SC-CCII.

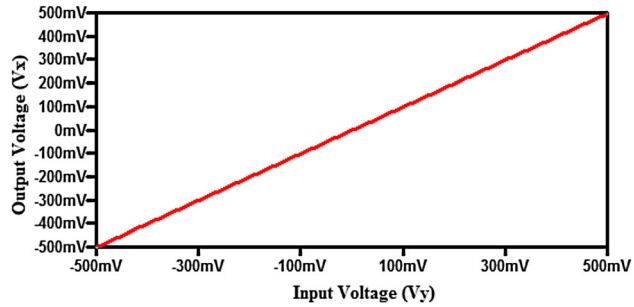

Figure 11. Voltage characteristics of proposed FVF based class-A SC-CCII.

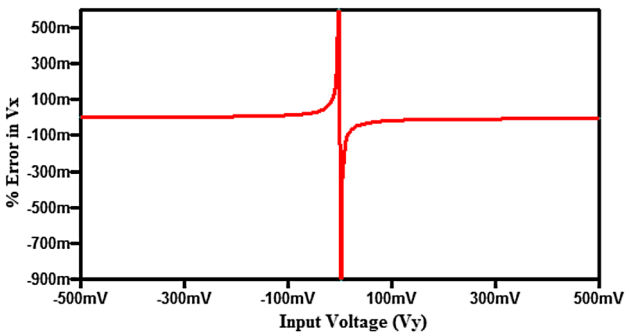

Figure 12. % Error curve for output voltage (Vx) of the proposed FVF based class-A SC-CCII.

proposed CCII and is achieved due to super-cascode configuration used in this circuit.

5.3 *Transient analysis*

Transient analysis of the proposed CCII architecture has been shown in this sub-section. A pulse signal of 25 MHz frequency has been applied at X terminal. The output obtained for a capacitive load of 1pF for the proposed CCII has been shown in figure 17. Positive slew rate (SR+) is calculated by observing the slope of the rising edge as

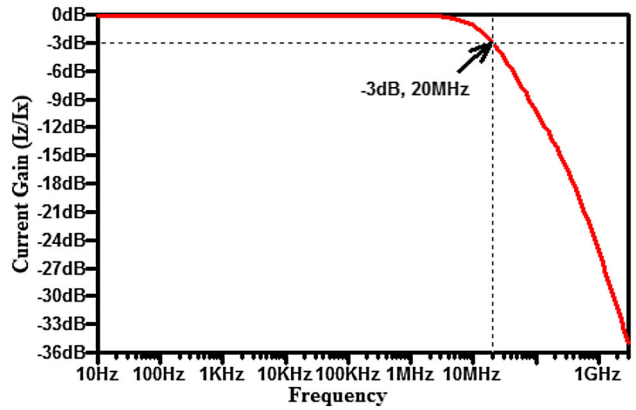

Figure 13. Frequency response showing variations in current gain of proposed class-A SC-CCII.

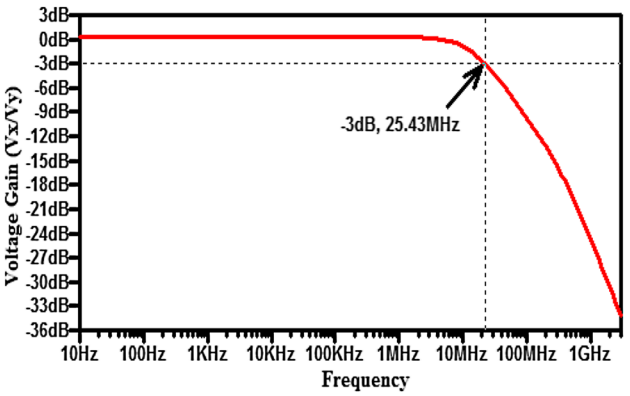

Figure 14. Frequency response showing variations in voltage gain for proposed class-A SC-CCII.

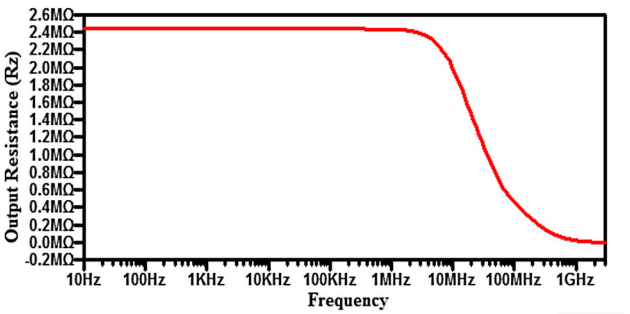

Figure 15. Output resistance (Rz) for proposed class-A SC-CCII.

shown in the figure. Similarly, negative slew rate (SR−) is calculated by observing the slope of falling edge of the waveform. Slew rates for other CCII configurations have also been calculated with the help of simulations and all these resultant parameters are listed in table 2. These values show that the slew rate of all the CCII configurations discussed in the paper are approximately similar with DCCII having the lowest slew rate.

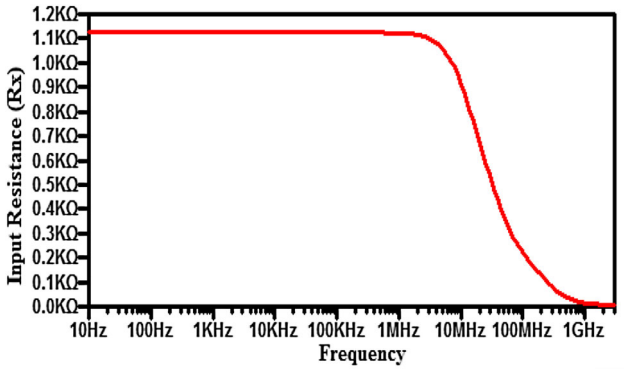

Figure 16. Input resistance (Rx) for proposed class-A SC-CCII.

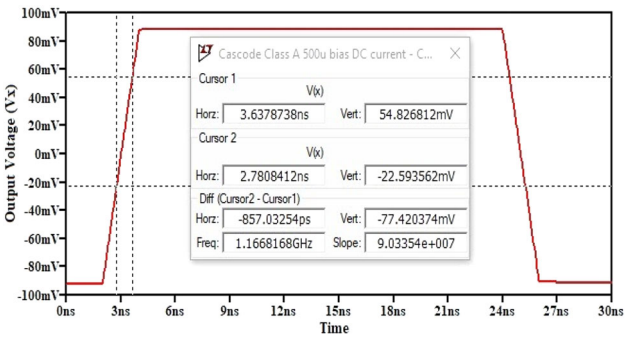

Figure 17. Transient response showing slew rate for FVF based Class-A SC-CCII.

6. Conclusion

Various high performance CCII topologies have been analysed and implemented in this paper. It has been observed that output resistance of these topologies is not sufficient for CCII to be used as a versatile block for implementing different circuits. FVF based class-A SC-CCII configuration has been designed and proposed in this paper. This proposed circuit utilizes super cascode configuration at output terminal (Z) to increase resistance seen through this node. Moreover, to achieve the required goal in the proposed CCII, biasing circuit is replaced with low voltage cascode current mirror. Small signal analysis mathematically justifies the improvement in output resistance. Simulations for the proposed CCII have been carried out in LtSpice using 0.18 μm technology. Moreover, the proposed CCII is compared with the existing high performance CCIIs. It has been observed that the proposed CCII offers maximum output resistance of 2.44 MΩ. Further, the proposed CCII operates for ±500 μA current range and ±500 mV voltage range. It offers 20 MHz current-gain bandwidth 25.43 MHz voltage-gain bandwidth and 89.83 V/μs slew rate with C_L of 1 pF. This proposed SC-CCII will prove to be an important block for designers working in the area of high performance integrated circuits.

Abbreviations

CCII	Second generation current conveyor
FVF	Flipped voltage follower
SC	Super-cascode
Opamp	Operational amplifier
VM	Voltage mode
GBP	Gain bandwidth product
CM	Current mode
CC	Current conveyor
DCCII	Differential second generation current conveyor
CCCII	Controlled current conveyor II

Declarations

Conflict of interest The authors declare that they have no conflict of interest.

References

[1] Franco S 2015 Design with operational amplifiers and analog integrated circuits. 4th edn. Mc Graw Hill Education, India, pp. 1–66

[2] Salem S B, Fakhfakh M, Sellami D, Loulou M, Loumeau P and Masmoudi N 2006 A high performance CMOS CCII and high frequency applications. *Analog Integr. Circuits Signal Process.* 49: 71–78

[3] Sedra A S and Smith K C 1970 A Second generation current conveyor and its application. *IEEE Trans. Circuit Theory* 17: 132–134

[4] Senani R, Bhaskar D R and Singh A K 2015 Current conveyors: variants applications and hardware implementations. Springer, Switzerland, pp. 3-16, 255-313

[5] Hassen N, Ettaghzouti T and Besbes K 2011 High performance second generation controlled current conveyor CCCII and high frequency applications. *WASET Int. J. Electron. Commun. Eng.* 5: 1764–1773

[6] Cha H W and Watanabe K 1996 Wideband CMOS current conveyor. *Electron. Lett.* 32: 1245–1246

[7] Fabre A, Saaid O, Wiest F and Boucheron C 1995 Current controlled bandpass filter based on translinear conveyor. *Electron. Lett.* 31: 1727–1728

[8] Pal K 1989 Modified current conveyors and their applications. *Microelectron. J.* 20: 37–40

[9] Awad I A 1999 Inverting second generation current conveyors: the missing building blocks, CMOS realizations and applications. *Int. J. Electron.* 86: 413–432

[10] El-Adawy A A, Soliman A M and Elwan H O 2000 A novel fully differential current conveyor and applications for analog VLSI. *IEEE Trans. Circuits Syst. II* 47: 306–313

[11] Zeki A and Toker A 2003 The dual-X current conveyor (DXCCII): a new active device for tunable continuous-time filters. *Int. J. Electron.* 89: 913–923

[12] Naik A P and Devashrayee N M 2010 A compact second generation current conveyor (CCII). In: *International conference on advances in recent technologies in communication and computing*, pp. 20–24

[13] Alzaher H A, Elwan H and Ismail M 2003 A CMOS fully balanced second-generation current conveyors. *IEEE Trans. Circuits Syst. II* 50: 278–287

[14] De Marcellis A, Ferri G, Guerrini N C, Scotti G, Stornelli V and Trifiletti A 2009 The VCG-CCII: a novel building block and its application to capacitance multiplication. *Analog Integr. Circuits Signal Process.* 58: 55–59

[15] Masmoudi D S, Salem S B, Loulou M and Kamoun L 2004 A radio frequency CMOS current controlled oscillator based on a new low parasitic resistance CCII. In: *International conference on electrical, electronic and computer engineering, ICEEC '04,* pp. 563–566

[16] Chunhua W, Yang L, Qiujing Z and Yu F 2010 Systematic design of fully balanced differential current-mode multiple-loop feedback filters using CFBCCII. *Radioengineering* 19: 185–193

[17] Metin B, Herencsar N and Vrba K 2012 A CMOS DCCII with grounded capacitor based cascadable all-pass filter application. *Radioengineering* 21: 718–724

[18] Ismail A M and Soliman A M 1998 Wideband CMOS current conveyor. *Electron. Lett.* 34: 1245–1246

[19] Surakampontorn W, Riewruja V and Cheevasuvit F 1991 Integrable CMOS-base realization of current conveyors. *Int. J. Electron.* 71: 793–798

[20] Torralba A, Carvajal R G, Ramirez-Angulo J and Munoz E 2002 Output stage for low supply voltage, high-performance CMOS current mirrors. *Electron. Lett.* 38: 1528–1529

[21] Aggarwal B, Gupta M, Gupta A K and Bansal S 2013 A novel very high performance current mirror for CMOS technology. *Analog Integr. Circuits Signal Process.* 75: 67–74

[22] Razavi B 2008 Design of analog CMOS integrated circuits. 2nd edn. Tata Mc-Graw Hill, New Delhi, pp. 134-172

[23] Gregorian R and Temes G C 2008 Analog MOS integrated circuits for signal processing. Wiley, New Delhi, pp. 64-120

[24] Aggarwal B, Gupta M and Gupta A K 2016 A comparative study of various current mirror configurations: topologies and characteristics. *Microelectron. J.* 53: 134–155