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# Design, real-time modelling, simulation and digital implementation of phase-locked loop-based auto-synchronising current-sourced converter for an induction heating prototype

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**Abstract.** Induction heating (IH) converters operate just above resonant frequency, at near unity power factor (UPF), to supply power to the targeted work-piece. Some power electronic converter-fed IH systems use power control strategies based on dynamic tracking of the changing resonant frequency as the work-piece gets heated up (since inductance changes). Therefore, the correct in-process determination of the resonant frequency is essential. A method of dynamically detecting the resonant frequency is by calculating the phase-shift between current and voltage continuously during the process. In case of CSI- (and VSI-) fed IH, the phase-shift between voltage and current is zero at resonant frequency. Hence one way of identifying the resonant frequency is by varying the frequency until the phase-shift is zero. For controlling this phase-shift between current and voltage waveforms, most of the controllers use a phase-locked loop (PLL) IC. In this paper, a novel method for the dynamic tracking of resonant frequency is proposed and the practical implementation of the same, using a field-programmable gate array (FPGA) based digital-PLL, is presented. The scheme is first simulated with generated off-line signal samples and then implemented on a real-time model of a CSI-fed IH application. Finally, the digital-PLL logic is implemented on controller hardware and practically tested in a laboratory-made experimental set-up of 2 kW at a nominal frequency of 10 kHz. The switching frequency is auto-synchronising. This fact is practically verified both by varying (i) the geometric dimensions as also (ii) the initial temperature of the work-piece. It is practically observed in the oscillograms that the phase gets locked in few cycles (and hence ensures quick tracking of the dynamically changing resonant frequency for this set-up).

**Keywords.** Induction heating; current source inverter (CSI); phase-locked loop; FPGA; real-time simulation.

## 1. Introduction

Induction heating converters operate just above resonance to supply power to the work-piece at almost unity power factor (UPF). The electrical equivalent of an indication heating (IH) system is a passive series (or parallel) *RL*-circuit. But the equivalent inductance of the coil puls work-piece combination has different values at different temperatures of the heated sample. For example, initially at room temperature of the work-piece, the inductor has some (maximum) value. It is well known that the magnetic permeability $\mu$ ($\mu = \mu_0\mu_r$, $\mu_r$ being the relative magnetic permeability of the material) of the work-piece is an inverse function of temperature. As the temperature increases inside the furnace, the permeability (and hence the inductance) gradually reduces. At Curie temperature, the magnetic permeability becomes exactly equal to the air (free-space) permeability and the inductance comes back to the initial value that would have been obtained without the work-piece. Thus, the inductor, as well as the equivalent resistor, depends on a number of parameters and its analytical determination is extremely involved. The resonant frequency also gets changed accordingly for a fixed value of the (resonant) capacitor. This compensating capacitor can be connected in series or in parallel with the induction coil. In case the induction coil is in series with the capacitor, then it has to be fed from voltage-fed inverter (VSI) [1]. For a parallel configuration the set-up has to be fed from a current-fed inverter (CSI) [1–5]. In both cases, the converter operates slightly above resonance. IH systems using power control strategies based on shifting out of resonance need to detect what then is the operating resonant frequency (dynamically changing with heating). Therefore, the correct in-process determination of the load circuit resonant frequency is a matter of vital importance in such IH converters. A method of detecting the resonant

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frequency is by dynamically computing the phase-shift between current and voltage waveforms. In case of CSI-(and VSI-) fed IH, the phase-shift between voltage and current is zero at resonant frequency. Hence, one method of determining the resonant frequency is by varying the frequency until the phase-shift is zero. For controlling this phase-shift, most of controller use a phase-locked loop (PLL) system. In this paper, a digital PLL for control of a power electronic converter for IH applications is presented. First, the nuances of control principles for PLL systems applied to IH power converters (IHPC) are introduced. Thereafter its real-time simulation is discussed, in section 3, followed by implementation of the logic in real time (section 4). Finally, in section 5, the hardware implementation on a practical experimental set-up of 2kW at a nominal frequency of 10 kHz is presented.

## 2. Phase-locked loop principles and description

It is known that a PLL is a circuit (system) that synchronises a periodic input signal with a periodic output signal. It is composed of three basic elements: a phase detector, a low-pass filter and a voltage-controlled oscillator (VCO). The scheme of a basic PLL is shown in figure 1 [6].

Figure 1 shows the block diagram of a typical PLL system. There are different types of PLLs, depending on the principles involved in implementing the phase detector, the filter and the VCO [6]. The output of the VCO will stabilise only when the phase difference between $v_i$ and $v_o$ is zero (and of course frequency is the same). Since the first analog PLL integrated circuits appeared in the 1960s, PLLs have incorporated more and more digital components. First the digital PLL appeared, which included digital phase detectors with exclusive OR(XOR) gates or flip-flops, and after that the all-digital PLL was made, in which all the components were digital. Over the last few decades, with the development of high-performance microcontrollers and DSPs, PLLs have become all-digital and software based. Although digital and all-digital PLLs are still widely used,

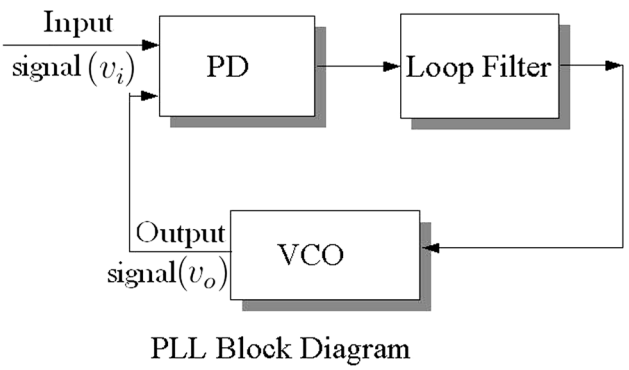



**Figure 1.** Basic scheme of a PLL circuit.

high-performance microcontrollers or DSP based-PLLs have advantages regarding the integration, flexibility and control complexity that can be difficult to realise with classical PLL systems.

Considering the use of PLLs and IH applications, PLL systems are used to control the phase-shift between the CSI output current and voltage till they reach the resonant frequency. Some examples of use of PLL schemes in IH may be found in [3].

## 3. Implementation of PLL logic in FPGA platform

Phase-locked loop (PLL) locks the phase of the output to the input. An unlocked phase and phase error ($\Delta\phi$) are shown in figure 2 and the locked phase condition is shown in figure 3. A simple yet novel method, not mentioned elsewhere in the published literature, has been proposed here.

If the frequency $\omega_o$ (output frequency) and $\omega_i$ (input frequency) are out of phase (unlocked) in a transient sense, then the phase error detector (PED) module detects the phase error and the phase conversion module smoothens the error signal ($v_{\Delta\phi}$). After an appropriate comparison stage a control signal is generated, which slows down or speeds up the frequency $\omega_o$ of the output ($v_o(t)$) till the phase difference is corrected to zero (locked) and hence frequencies are equalised. The PLL logic proposed and implementation in the present work has been shown in figure 4 in the form of a flowchart. The implementation of each module (part) is described in following paragraphs.

### 3.1 *Phase error detector (PED)*

If output signal ($v_o(t)$) and input signal ($v_i(t)$) are out of phase (unlocked), then the phase error detector (PED) module detects the error between the input and the output signal (figure 2). This will continuously (dynamically) go on happening since the resonant frequency of the load circuit changes with temperature.

The phase error can be easily found by logical XOR-ing the two signals (digitally). The logical symbol and truth table of XOR gate are shown in figure 5.

### 3.2 *Phase error conversion module*

The phase conversion module converts the phase error to a corresponding numerical (digital) value and thereby smoothens the error signal (as shows in figure 6). The phase conversion has been done using an up/down counter, where it 'up-count's during the high duration of the error signal starting at the high going edge. The counting is enabled at the low going edge of the error signal as shows in figure 7. The final count at the end of the high duration (peak of the

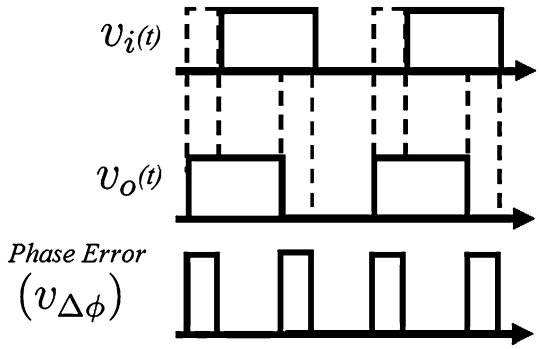



**Figure 2.** Unlocked phase and phase error ($\Delta\phi$).

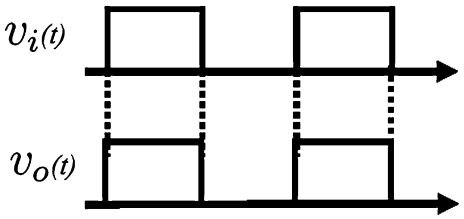



**Figure 3.** Locked phase.

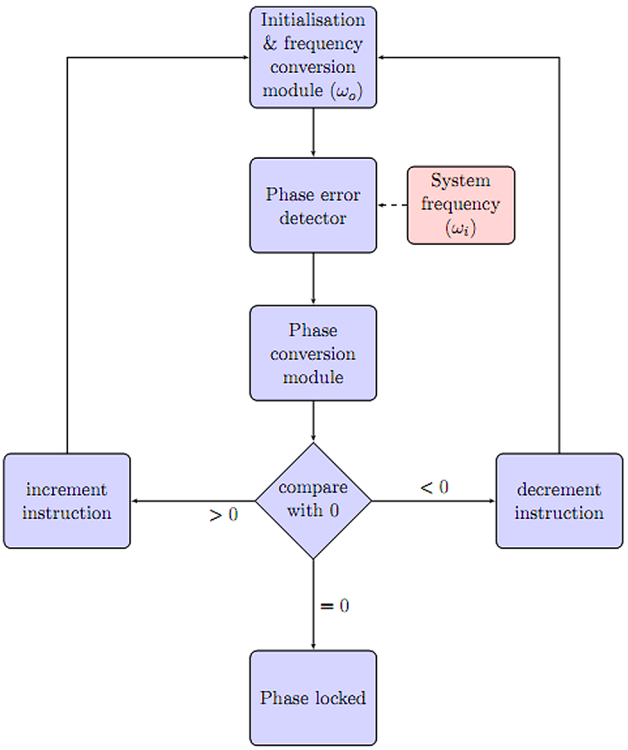



**Figure 4.** Flowchart of phase-locked loop implementation logic.

ramp) is sampled using a D-flip-flop as shown in figure 8. It is evident that the final count (and hence the output from D-flip-flop) changes with change of the width of high duration ($\Delta\phi$). This explanation holds for the case of a leading input signal. If the input signal lags the output signal, there will not be any change in the waveform of the PED output signal. Still another D-flip-flop is used to detect the peak value (final count). Only, in this case the value is inverted to (get a negative value and) imply lagging sense.

Thus, the value (final count) is positive if input signal ($v_i(t)$) leads the output ($v_o(t)$), and negative if input signal lags the output signal.

### 3.3 *Phase error comparator module*

Comparisons module is used to compare the phase-converted numerical (digital) value from the preceding stage with 'zero'. When value is compared with the 'zero', if the numerical value is greater then zero then frequency reduction instruction is passed on to the next stage. If on the other hand this value is less then 'zero' then frequency increment instruction is passed on. Thus finally frequency gets locked, as the phase error goes to zero after a few cycles of incrementing (or decrementing) the frequency. The phase-locked signal shown in figure 9.

### 3.4 *Frequency conversion module*

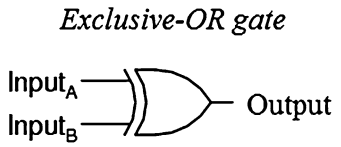
As mentioned, a frequency conversion module is used to convert a digital value to a logic pulse at fixed frequency. The pulse frequency can be changed by increasing or decreasing the digital value. A simple logic has been implemented to obtain the pulse and implemented first in real-time simulation. The implementation of the same is explained in the next section.

## 4. Implementation of PLL control on real-time model of induction heating system

Before practical implementation is carried out, it is preferable to have a real-time simulation of the system in question. In the present case we have to therefore represent the power converter plus coil assembly by its mathematical model. Here, the model, whose derivation is detailed below, is implemented on an field-programmable gate array (FPGA) platform in real time. The FPGA platform is built around an Altera-make Cyclone EPIC12Q240C processor.

### 4.1 *Simulation model*

The system simulated is a CSI fed IH coil with an H-bridge power converter consisting of 4 IGBTs with series diodes (for reasons already discussed in [7]) and is shown in figure 12. The system parameters are given in table 1. The parameters (resonant frequency, inductance, etc.) were evaluated through an FEM analysis of the electromagnetic model of the IH coil [8]. Figure 10a and b shows the plots




| A | B | Output |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

**Figure 5.** Logical symbol and truth table of XOR gate.

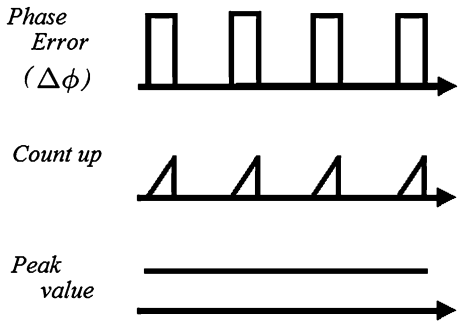



**Figure 6.** Count of up in the phase error duration and detection of the peak value.

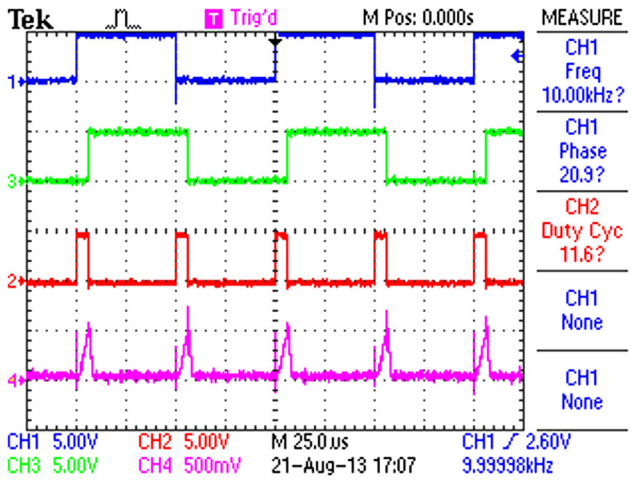



**Figure 7.** The phase error detection and the phase conversion.

of the generated mesh (obtained after meshing operation) and flux density (obtained after running the solver) under the rated operating conditions. The exercise was repeated at different frequencies to obtain the parameter values over a large range of frequencies. Figure. 11 shows the resistance and inductance varying with change of frequency [9]. The values in table 1 below correspond to a frequency of 7.88 kHz as can be seen from the graphs. The value of the capacitance can be worked out using a simple formula [9].

It may be mentioned here that the values of the circuit parameters were experimentally verified and were found to be in fair agreement with the FEM model values, as has been detailed in table 1.

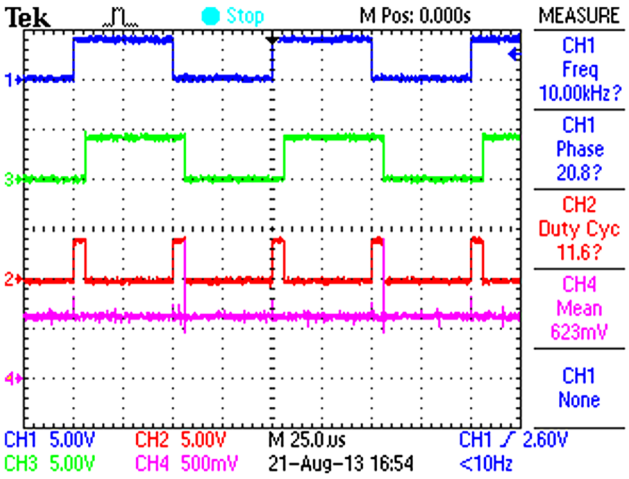



**Figure 8.** Phase-converted smooth error signal.

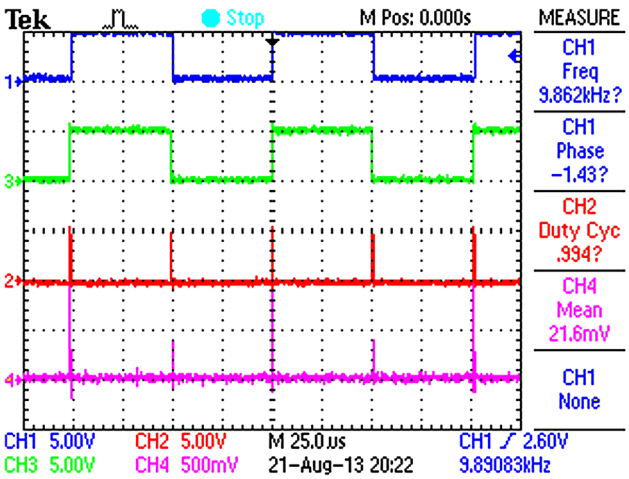



**Figure 9.** Frequency has been locked and phase-converted smooth error signal is equel to 'zero'.

**Table 1.** Important parameters of the simulated system.

| Parameters | Analytical value | Experimental value |
|---|---|---|
| Load resonant circuit | | |
| Inductance | 16.8 µH | 19.6 µH |
| Resistance | 0.139 Ω | 0.14 Ω |
| Capacitance | 21 µF | 21 µF |
| Resonant frequency | 8.47 kHz | 7.88 kHz |
| DC-link current | 8 A | 8 A |

## 4.2 *Model equation*

An electrical parallel LC resonant circuit is shown in figure 12 where the series 'RL' element represents the coil in the presence of the sample to be heated and the 'C' represents the actual capacitor connected across the experimental coil. Transient current and voltages are established

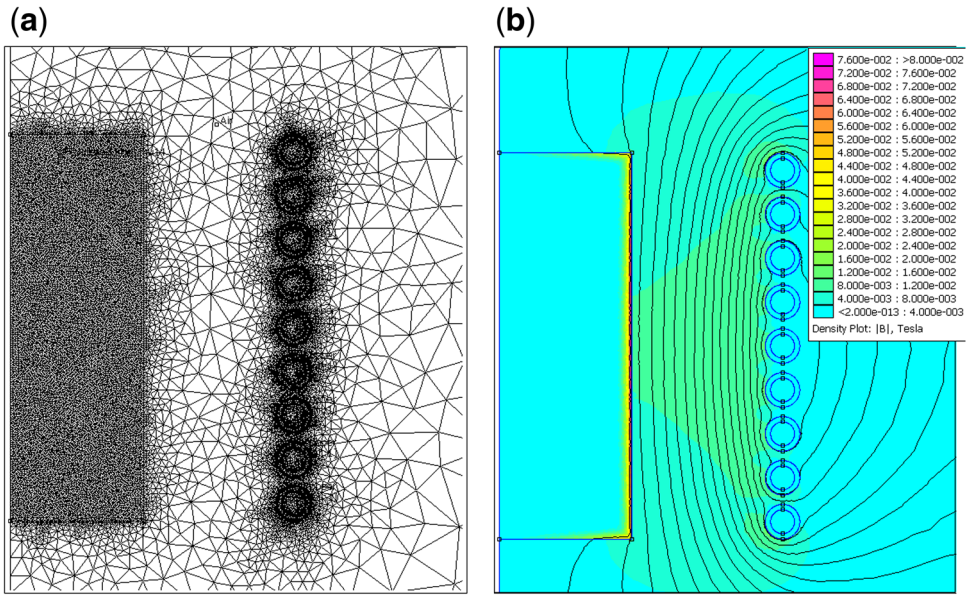



**Figure 10.** (**a**) Manually generated mesh output plot for the FEM and (**b**) flux density plot for the same.

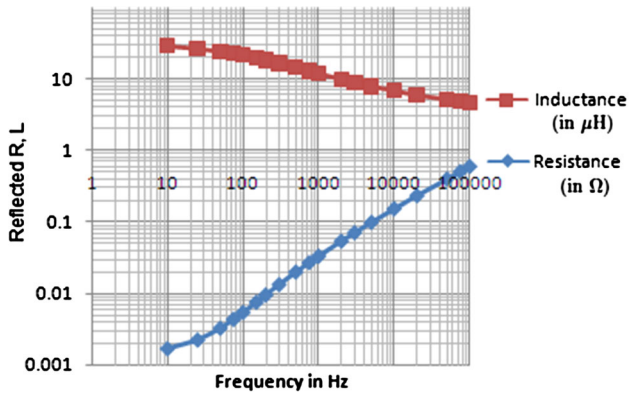



**Figure 11.** Frequency versus coil-reflected resistance (in Ω) and inductance (in μH).

in the circuit when the switches are operated. The assumed positive sense of the variables are as indicated in figure 12. Equations that describe the transient behaviour of the circuit (figure 12) are given by

$$i'_L = i_L + i_C \tag{1}$$

$$i_C = C\frac{dv_C}{dt} \tag{2}$$

$$v_C = Ri_L + L\frac{di_L}{dt} \tag{3}$$

arising out of KCL and KVL.

These equations are first-order linear differential equations that can be solved using standard numerical methods (one of which is mentioned in the appendix). The equations

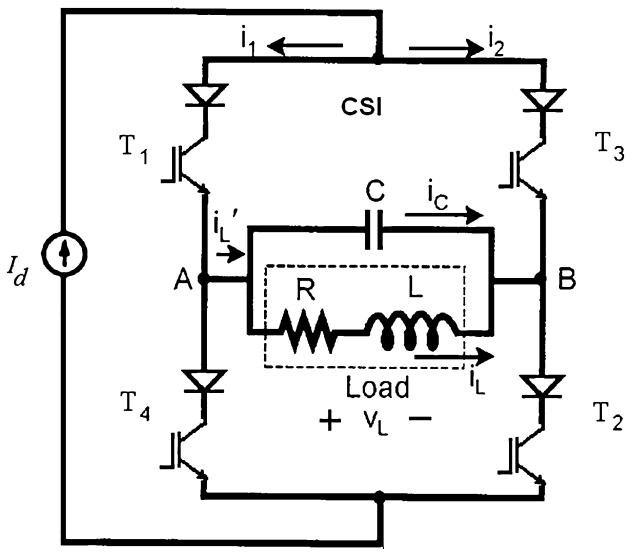



**Figure 12.** Current source inverter fed parallel resonance circuit.

are first normalised with the help of base values $V_b$, $R_b$ and $I_b$. The base values were chosen with the following justification. The $Q$-factor of the present IH coil is 7. This, in other words, implies that the reactive current component is 7 times the active current. Keeping a factor of safety of 2, the largest number for the allowable maximum bits should represent 14 of the $I_d$. Accordingly, $I_b = 25$ A, and $R = 10$ Ω. Thus, we get,

$$\frac{i'_L}{I_b} = \frac{i_L}{I_b} + \frac{i_C}{I_b} \tag{4}$$

**Table 2.** Parameters.

| Parameters | | PU value | Equivalent decimal value |
|---|---|---|---|
| $V_b$ | 250 V | 1 | $16383_d$ |
| $R_b$ | 10Ω | 1 | $16383_d$ |
| Step time $\Delta t$ | $0.2 \times 10^{-6}$ s | – | – |
| $\tau_{CR}$ | $210 \times 10^{-6}$ s | – | – |
| $\tau_{LR}$ | $1.96 \times 10^{-6}$ s | – | – |
| $\frac{\Delta t}{\tau_{CR}}$ | $\frac{0.2\times10^{-6}\text{ s}}{210\times10^{-6}\text{ S}}$ | $9.766 \times 10^{-4}$ | $16_d$ |
| $\frac{\Delta t}{\tau_{LR}}$ | $\frac{0.2\times10^{-6}\text{ s}}{1.96\times10^{-6}\text{ S}}$ | 0.101 | $1655_d$ |
| $R^*$ | $\frac{0.14}{10}$ | 0.014 | $228_d$ |

**Table 3.** PU values.

| PU value | Equivalent digital value | Equivalent decimal value |
|---|---|---|
| 2 | $7FFF_h$ | $32767_d$ |
| 1 | $3FFF_h$ | $16383_d$ |
| 0 | 0 | 0 |
| −1 | $C000_h$ | $49152_d$ |
| −2 | $8000_h$ | $32768_d$ |

$$\frac{i_C}{I_b} = CR_b \frac{d\frac{v_C}{V_b}}{dt} \tag{5}$$

$$\frac{v_C}{V_b} = \frac{Ri_L}{R_b i_b} + \frac{L}{R_b}\frac{d\frac{i_L}{I_b}}{dt} \tag{6}$$

where $I_b = \frac{V_b}{R_b}$.
With the replacements

$$\frac{i'_L}{I_b} = i^*, \frac{i_L}{I_b} = i_L^*, \frac{i_C}{I_b} = i_C^*, \frac{v_C}{V_b} = v_C^*, \frac{R}{R_b} = R^*, CR_b = \tau_{CR}, \frac{L}{R_b} = \tau_{LR}$$

a set of non-dimensional equation results:

$$i^* = i_L^* + i_C^* \tag{7}$$

$$i_C^* = \tau_{CR}\frac{dv_C^*}{dt} \tag{8}$$

$$v_C^* = R^* i_L^* + \tau_{LR}\frac{di_L^*}{dt}. \tag{9}$$

These first-order linear differential equations can be solved using Euler's method as mentioned in the appendix.

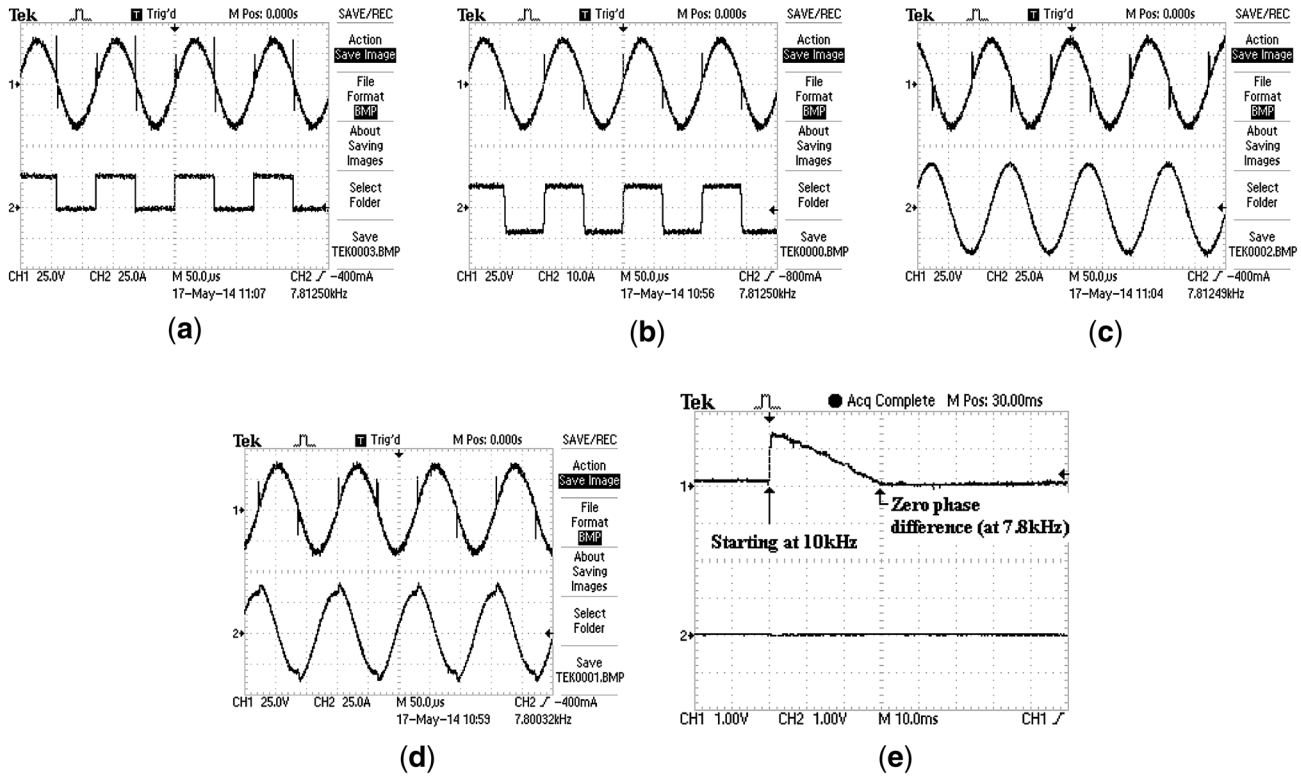



**Figure 13.** (**a**) Waveforms of load voltage ($v_L$) and gate pulse of the device $T_1$. (**b**) Waveforms of load voltage ($v_L$) and inverter terminal current ($i'_L$). (**c**) Waveforms of load voltage ($v_L$) and coil current ($i_L$). (**d**) Waveforms of load voltage ($v_L$) and capacitor current ($i_C$). (**e**) Waveforms of phase-error-converted numerical (digital) value as discussed in 3.2. Waveforms of real-time simulation.

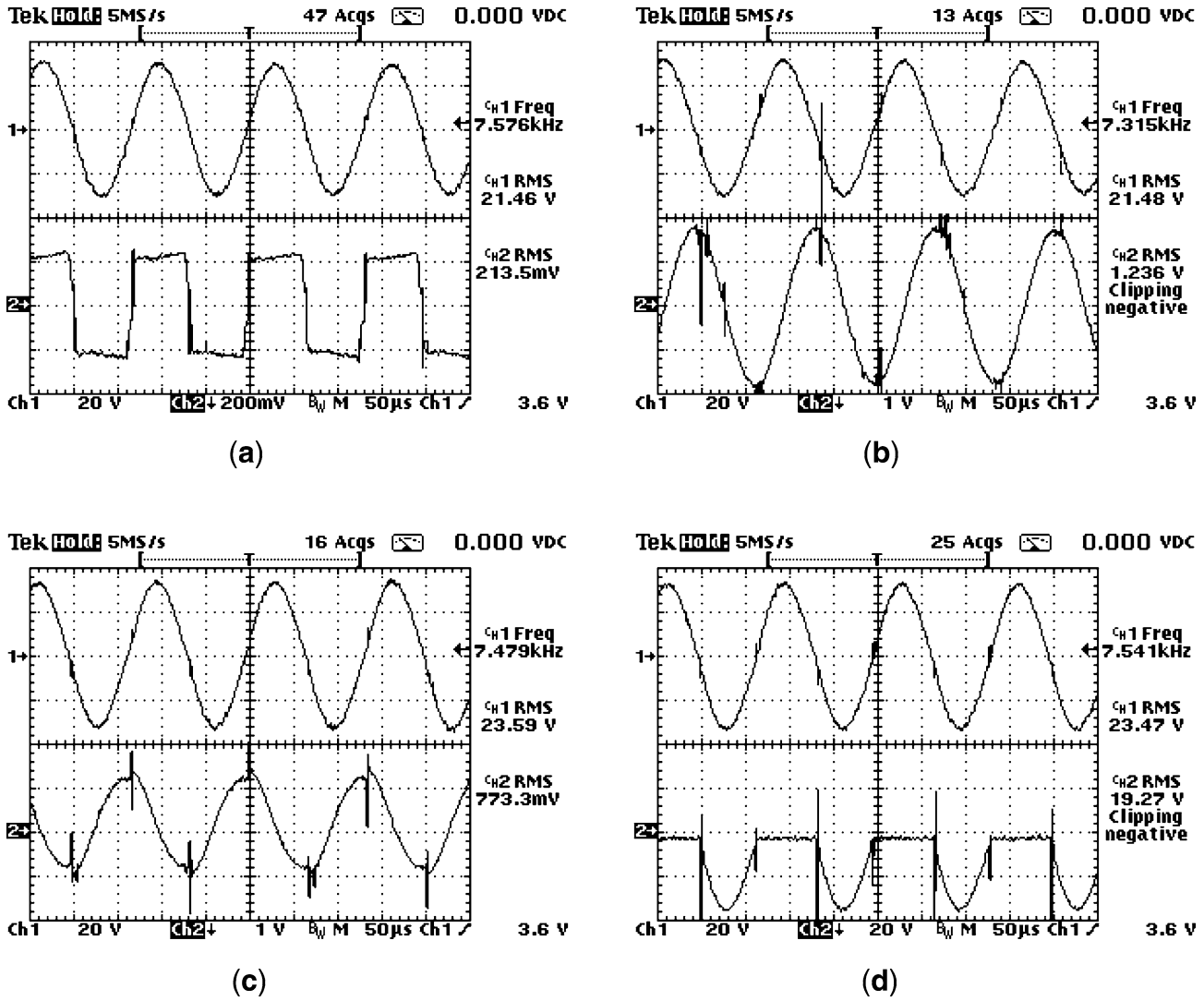



**Figure 14.** (**a**) Waveforms of CH1: coil voltage (20 V/div) and CH2: inverter terminal current (8 A/div). (**b**) Waveforms of CH1: coil voltage (20 V/div) and CH2: coil current (20 A/div). (**c**) Waveforms of CH1: coil voltage (20 V/div) and CH2: capacitor current (40 A/div). (**d**) Waveforms of CH1: coil voltage (20 V/div) and CH2: device voltage (20 V/div). Experimental waveform of laboratory-made induction heating converter applying FPGA-based PLL logic.

### 4.3 *Implementation*

4.3a *Parameters:* Table 2 gives the chosen base values for voltage, current and the values of other quantities.

4.3b *PU system followed:* Table 3 shows the digital equivalent for the PU (per-unit) values [10, p. 9]. The bit length of the digital word is not limited in an FPGA. In order to incorporate the signed arithmetic, the digital equivalent for a negative PU value is chosen as 1's complement of digital equivalent of its corresponding positive PU value.

### 4.4 *Results*

The output waveforms are shown in figure 13. Figure 13e shows waveform of phase-error-converted numerical (digital) value. The real-time simulation was started with a converter switching frequency of 10 kHz. However, as seen earlier, the coil resonant frequency is 7.8 kHz. The waveform demonstrates how smoothly the switching frequency adjusts itself to 7.8 kHz (though initially set at 10 kHz), in the process adjusting the phase error to zero (ramp falls to zero) through PLL mechanism in only 30 ms. The waveform thus establishes the success of the developed PLL strategy.

Figure 13a shows the simulated waveforms of the logic pulse (for device $T_1$) in channel 2 and load voltage ($v_L$) in channel 1, and they are clearly in phase with each other. Similarly, figure 13b shows the load voltage ($v_L$) in channel 1 and inverter output current ($i'_L$) in channel 2. Figure 13c shows the simulated waveform of the load voltage ($v_L$) in channel 1 and coil current ($i_L$) in channel 2. Figure 13d

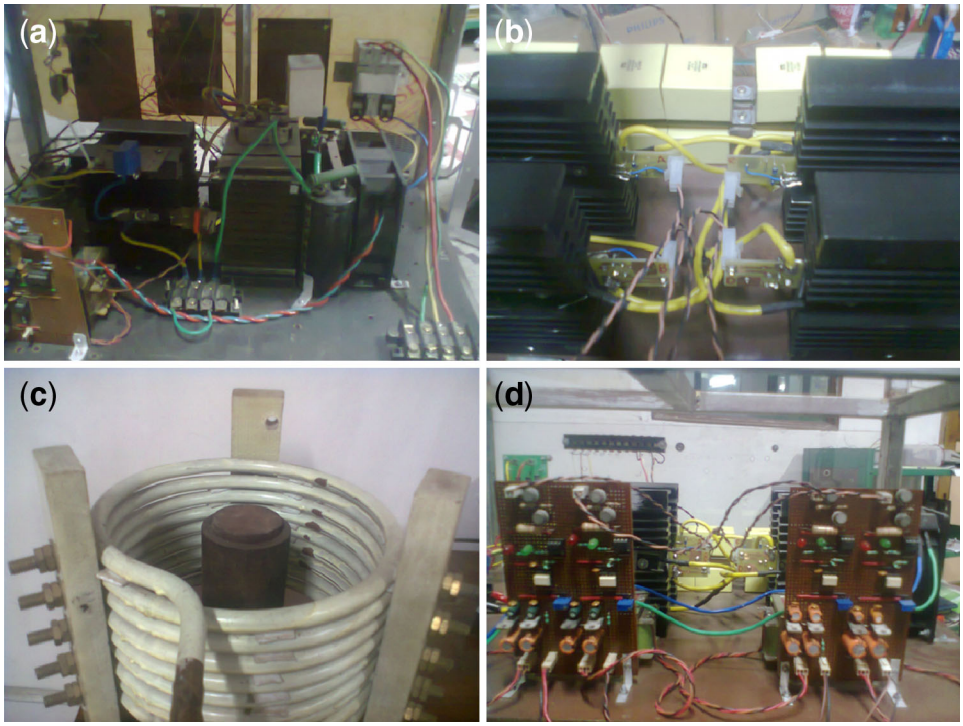



**Figure 15.** Photograph of laboratory prototypes of (**a**) rectifier module and buck chopper, (**b**) IGBTs with series diode are placed on the heat sink and capacitor bank, (**c**) induction coil and work-piece and (**d**) IGBT-based converter and its driver circuit.

**Table 4.** Set-up details.

| Sl. no. | Quantity | Value or rating |
|---|---|---|
| 1 | DC link inductor ($L_d$) | 20 mH |
| 2 | Coil inductance ($L_{coil}$) | 19.8 μH |
| 3 | Coil resistance ($R_{coil}$) | 0.14 mΩ |
| 4 | Capacitor across coil ($C$) | 21μF |
| 5 | IGBT | IRG4PC40U |
| 6 | Diode | DSEI60-12A |

**Table 5.** Key experimental results for IGBT-based CSI fed IHU.

| Sl. no. | Quantity | Meter reading |
|---|---|---|
| 1 | Resonant frequency ($f_r$) | 7.8 kHz |
| 2 | CSI operating frequency ($f_s$) | 7.8 kHz |
| 3 | Coil current ($I_L$) | 30 A |
| 4 | Load voltage across coil ($V_L$) | 27 V |
| 5 | Peak inverse voltage across device ($T_1$) | 38 V |
| 6 | Current through DC-link inductor ($I_d$) | 8 A |

shows the simulated waveform of the load voltage ($v_L$) in channel 1 and capacitor current ($i_C$) in channel 2 (figure 14).

## 5. Hardware implementation

The circuit diagram for the induction heating converter has been shown in figure 12 and a photograph of the laboratory prototype is shown in figure 15. Figure 15a shows a photo of the rectifier module (TSPR40PB), DC-link capacitor and the buck chopper portion of the converter. In figure 15b IGBTs with series diode are seen to be placed on the heat sink along with the compensating capacitor bank of 21μF. Figure 15c shows the photo of the induction heating coil and the work-piece (job), which is placed inside the coil. Figure 15d shows the IGBT-based converter and its driver circuit. The details of design, fabrication and operation of the entire set-up may be found in [11]. The developed PLL logic has been applied in the afore-mentioned experimental set-up developed in the laboratory, whose details are given in table 4.

It has been observed that the load voltage phase gets locked with the converter current within a few cycles. The switching frequency is shown to be auto-synchronising. This fact is also practically verified both by (i) varying the geometric dimensions as also (ii) the initial temperature of the work-piece. It is practically observed in the oscillograms that the phase gets locked in a few cycles (and hence the operating resonant frequency) for this set-up. This is an important feature of this experimental work and has application potential in the industry. The experimental waveforms of the load voltage and inverter terminal current have been shown in figure 14a and it is seen that the waveforms are precisely in phase with each other. It is clearly seen that the voltage and current are in the same phase. The set-up operates at around 7.8 kHz for the present billet samples. Also the experimental results are in excellent correlation with those predicted using the real-time model as shown in figure 13b.

Figure 14c shows the experimental waveforms of the load voltage ($v_L$) and capacitor current ($i_C$). Once again the waveforms are found to match excellently with the predicted waveforms in figure 13d. Figure 14b shows the experimental waveforms of the load voltage ($v_L$) and current ($i_L$) of the induction coil. These waveforms are also found to agree very well with the predicted waveforms in figure 13c. A hall current sensor (ratio 20:1) is used for sensing the current. Figure 14d shows the experimental waveform of the load voltage ($v_L$) and voltage across the device ($T_1$). Table 5 summarises the meter readings and other practical values obtained during this test.

## 6. Conclusions

In this paper, real-time simulation and hardware implementation of a digital PLL for self-adjusting resonant CSI-fed IH application is thoroughly presented. As mentioned elsewhere, the nominal ratings of the set-up are 2 kW at the nominal frequency of 10 kHz. The digital PLL is first simulated and implemented in (FPGA-based controller) real-time simulation of the afore-mentioned system. Modelling of the power electronic converter-fed parallel RLC circuit (equivalent to IH system) for real-time simulation has also been done. Then the digital PLL logic is practically implemented in laboratory-made small-scale prototype circuit of CSI-fed IH application and the results have been compared. It has been observed that switching frequency is auto-synchronising under all conditions of loading and temperature variation. The results and waveforms from simulation and experiments are found to be in excellent agreement.

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## Appendix

Dynamic systems may be represented generally in the form of ordinary differential equation (ODE)

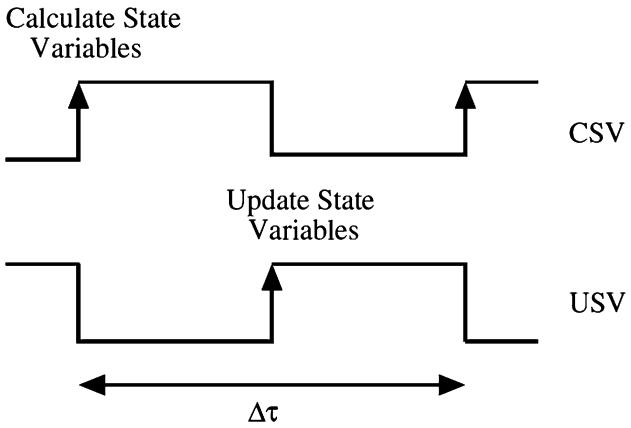


**Figure 16.** Triggering timing.

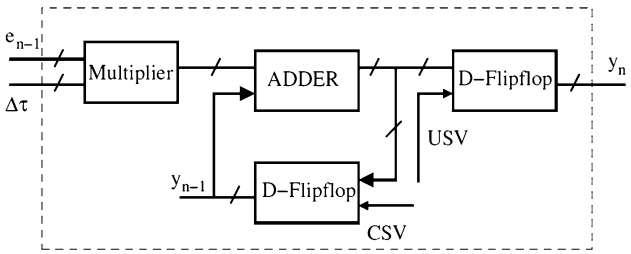


**Figure 17.** Zero-order integrator (Euler's method).

$$\frac{dy_i}{dt} = e_i(x_j, y_k, t), \quad i, j, k = 1, 2, 3, \ldots, n \tag{10}$$

where $x_j(t)$ are the independent forcing functions, $y_k(t)$ are the state variables and $t$ the time.

The procedure for solving a system of equations simply involves applying the one-step technique for every equation at each step before proceeding to the next step. A clock signal drives the digital circuit. During each clock cycle, the present states of the system are calculated. These calculations are split into two stages as shown in figure 16. In the first stage the present states of the system are calculated using the previous states of the system. In the second stage the values are updated. There are several integration methods [12] to solve the differential equations (10). These methods differ in complexity. Each integration method can be implemented by digital logic elements in FPGA [13, pp. 81–90]. Because of its simplicity, Euler's algorithm is widely used.

### *Backwards Euler's method*

In this method, the time axis is subdivided into several intervals. In each interval, $e_i$ is approximated by a constant representing the average of $e_i$ in that interval. A new value of $y_i$ is predicted using the slope (equal to the first

derivative at the previous value) to extrapolate linearly over the step size $\Delta t$:

$$y_i(n) = y_i(n-1) + e_i(n-1)\Delta t. \tag{11}$$

In digital logic circuit, Euler's method is represented as shown in figure 17.

D-flip-flop is used for delaying the input until the next clock pulse is given. With the rising edge of the clock pulse CSV, $y_i(n-1)$ is latched. Error function $e_i(n-1)$, which is dependent on the previous state variables $y_i(n-1)$, is calculated and given as input to the integration block. Inputs to the ADDER block are $y_i(n-1)$ and $e_i(n-1)\Delta t$ as in Eq. (11). State variables are updated with the rising edge of the clock USV.

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