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An X band RF MEMS switch based on silicon-on-glass architecture

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Abstract. Communication systems such as those used on satellite platforms demand high performance from individual components that make up the various systems and sub-systems. Switching and routing of RF signals between various modules is a routine and critical operation that determines the overall efficiency of the entire system. In this paper, we present the design and fabrication aspects of a direct contact RF MEMS switch designed to operate in the X band (8–12 GHz) with a target insertion of about 0·5 dB and isolation better than 30 dB. The actuation voltage is expected to be around 50 V. The die size is designed to be 3 mm (H) × 3 mm(W) × 2 mm(H). The switch is built from a low residual stress device layer of a highly conducting (0·005 Ohms-cm) silicon on insulator (SOI) wafer. After subsequent lithographic steps, the wafer is bonded to a Pyrex glass wafer which has been previously patterned with gold transmission lines and pull in electrodes. Being built from a single crystal silicon structure, the mechanical robustness of the actuator is much greater than the those in similar membrane-based devices. A 6 mask fabrication process utilizing Deep Reactive Ion Etching to achieve high aspect ratio stiction free structures was developed and implemented. Devices from the first fabrication run are being analysed in our laboratory.

Keywords. RF MEMS; deep reactive ion etching; silicon-on-insulator.

1. Introduction

Switching and routing of high frequency RF signals (10–60 GHz) is a routine and important process in satellite communication modules. The overall efficiency of the host system is critically dependent on the performance of the switching elements that appear in the signal path. Conventional switches based on PIN diodes and mechanical coaxial switches have been extensively used till date. Solid state switches such as PIN diodes exhibit poor isolation at frequencies and are known to introduce distortions in the input signal at high frequencies. On the other hand, mechanical switches perform well at high frequencies but are

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Table 1. Target specifications of the RF MEMS switch.

Operating frequency	8–12 GHz (X band)
Insertion loss	$< 0{\cdot}5$ dB
Isolation	> 30 dB
Actuation voltage	< 50
RF power handling capacity	< 500 mW

heavy and power hungry. In satellite systems with tight weight and power budgets these features are undesirable. An elegant solution to this problem is offered by Micro Electromechanical Systems (MEMS) technology. RF switches based on MEMS processes combine the advantages of small size of solid state switches and the linearity and high isolation of mechanical switches (Rebeiz 2003). Also, the current trend of development of miniaturized space system such as planetary probes and micro satellites demand miniaturized high performance RF components such as filters, phased array antennae which are based on RF MEMS switches of various types. In this paper, we present the design and fabrication details of a direct contact series RF MEMS switch currently underway in our laboratory. The target specifications for the device are given in table 1. These specifications are intend to be a broad guideline for the initial fabrication attempts. The following sections focus mainly on the fabrication efforts. RF simulations and optimization will be presented elsewhere.

2. Structure and design

The device under fabrication is a direct contact RF MEMS switch. We employ a commonly used substrate transfer technique that has been used by several groups to fabricate MEMS devices such as RF switches and variable capacitors (Sakata *et al* 1999, Kim *et al* 2004, 2005). The actuator part of the switch fabricated from the device layer of a high conductivity silicon on insulator (SOI) wafer. The actuator is suspended by fine beams over a gap on CPW transmission line patterned in gold on a low loss Pyrex 7740 glass substrate. A contact dimple made from a gold–platinum alloy $0{\cdot}2\,\mu$m thick and isolated by a thermally grown silicon dioxide layer of thickness $1{\cdot}0\,\mu$m) micromachined on the lower part of the actuator facing the transmission lines. On either side of the contact region are drive capacitors $250 \times 300\,\mu$m (each) are fabricated on the same silicon structure to provide the electrostatic drive mechanism required to 'close' the switch. A three-dimensional model of the switch is shown in figure 1(a). An expanded view of the actuator structure is shown in figure 1(b). The ground lines of the CPW waveguides also act as the bottom pull in electrodes. A thin silicon dioxide insulating layer is deposited on the CPW ground lines in the area directly beneath upper electrodes on the actuator to prevent shorting and stiction in the ON state. The entire actuator structure acts like upper electrode since it is highly conducting. This has the advantage of not having to pattern separate upper electrodes on the actuator structure. Electrical contacts to the upper electrodes are taken via aluminum pads that are sputtered and annealed to produce low resistance ohmic contacts. Detailed electromemcanical and RF simulations of the switch are being carried out alongside the fabrication runs. The important structural dimensions used in these simulations are described in figure 2. The fabricated device has the same dimensions of the suspension beams as used in the simulations.

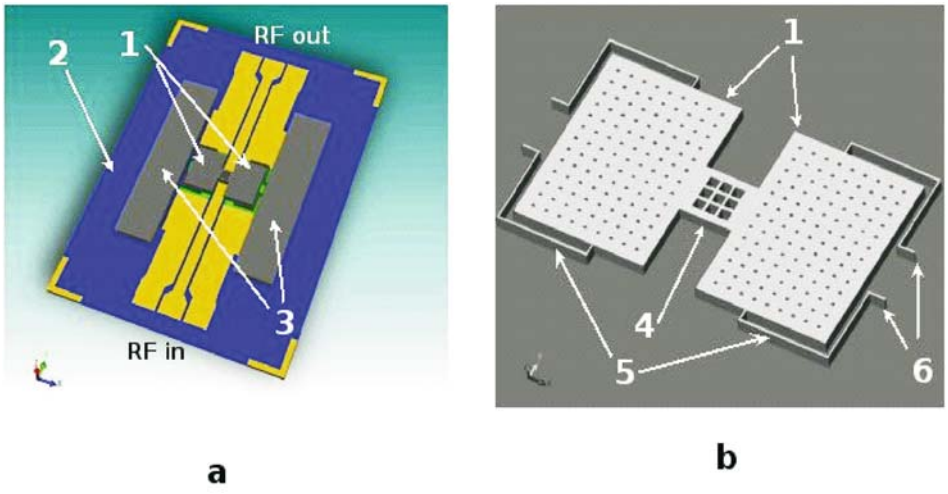

Figure 1. **(a)** Showing a three-dimensional model of the device 1-drive capacitors on the actuating structure, 2-the glass substrate on which the transmission lines are patterned, 3-contact pads for the upper electrodes, the CPW input and output ports of the device are indicated. **(b)** Showing the details of the actuator, 4-the contact region that bridges the gap in the transmission lines, 5-suspension beams, 6-anchor points of the suspension beam (anchor post and transmission lines not shown in the illustration).

Figure 3 shows a typical result of such a simulation. The FEM calculations were performed using a MEMS simulation package. The results obtained will be compared with measurements made on actual devices in the laboratory and parameters in the computer models will be adjusted so that they mimic the actual devices as best as possible. Such validated models will be used to refine the current design in subsequent fabrication runs. The consolidated simulation results will be presented elsewhere.

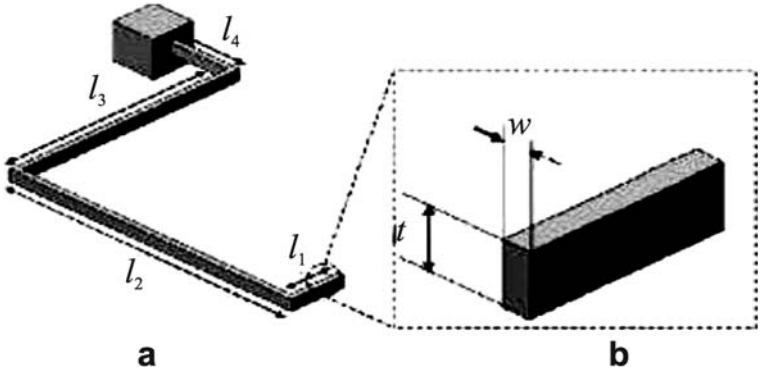

Figure 2. A close-up view of the suspension beams of the actuator structure. The length of the beam segments shown in **(a)** are $l_1 = 20$ um, $l_2 = 175$ um, $l_3 = 145$ um, $l_4 = 30$ by design. The thickness and the width illustrated in **(b)** are $t = 25$ um and $w = 4$ um. The gap between the capacitor plates is taken to be 2·8 um. These values are used to estimate the pullin voltages from FEM simulations.

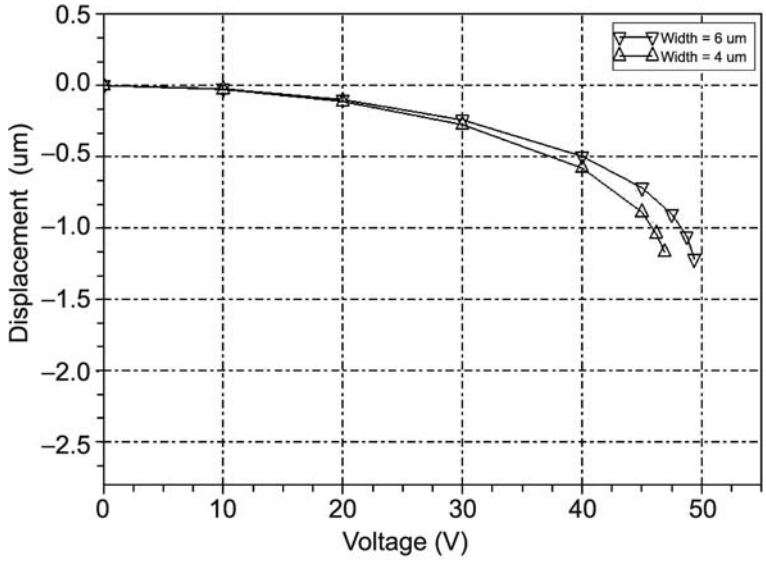

Figure 3. Simulation of the pull in behaviour of the switch using FEM model. The two curves correspond to two different widths of the suspension beams. The parameters used in these simulations are the ones described in figure 2.

3. Fabrication process

Important steps in the fabrication process flow are indicated in figure 4. Fabrication starts with a ⟨100⟩ SOI wafer with a 30 μm device layer a 4 μm thick buried oxide layer and a 380 μm thick handle layer. The resistivity of the device and handle layers are 0·001–0·005 Ohm-cm. The first step involves the etching of 5 μm cavities surrounded by supporting pillars that act anchors for the actuator when fabricated at a later stage. Etching the cavities to the correct depth is important from the RF point of view since this defines the transmission line to contact dimple gap, which in turn determines the isolation in the off state. A timed 3 minute Bosch process was used to etch the cavities with uniformity of $\pm$0·5 μm across the 100 μm wafer. An insulating thermal oxide layer is grown using wet oxidation at 995°C. The oxide is patterned to form a dimple on which a specialized gold pad (of 2000 A thickness) for electrical contact is patterned. The cross section through the contact dimple is illustrated in figure 4a. A 1 mm thick pyerx glass wafer is patterned with transmission lines and pull in electrodes formed from gold film 0·2 μm thick with an underlying chromium seed layer 0·07 μm thick. Silicon dioxide is then sputtered and patterned by lift-off to form the insulating layer between the drive electrodes. The glass substrate is 'trenched' to half its thickness using a wafer dicing system as shown in figure 2b. The trenches will facilitate device singulation after the fabrication is completed. The glass and silicon wafers are anodically bonded as shown in figure 4c. The bonding was carried at 375°C with 600 V applied across the wafers under high vacuum. Removal of the handle layer and buried oxide is carried out using wet chemical etchants, 30% KOH at 80 deg C and buffered HF solution respectively as illustrated in figure 4d. The 4 μm thick buried oxide acts as very reliable etch stop for the KOH etchant. The subsequent removal of the buried oxide leaves behind a 25 μm free hanging single crystal silicon. This is the main advantage of using SOI wafers in this process. Most other

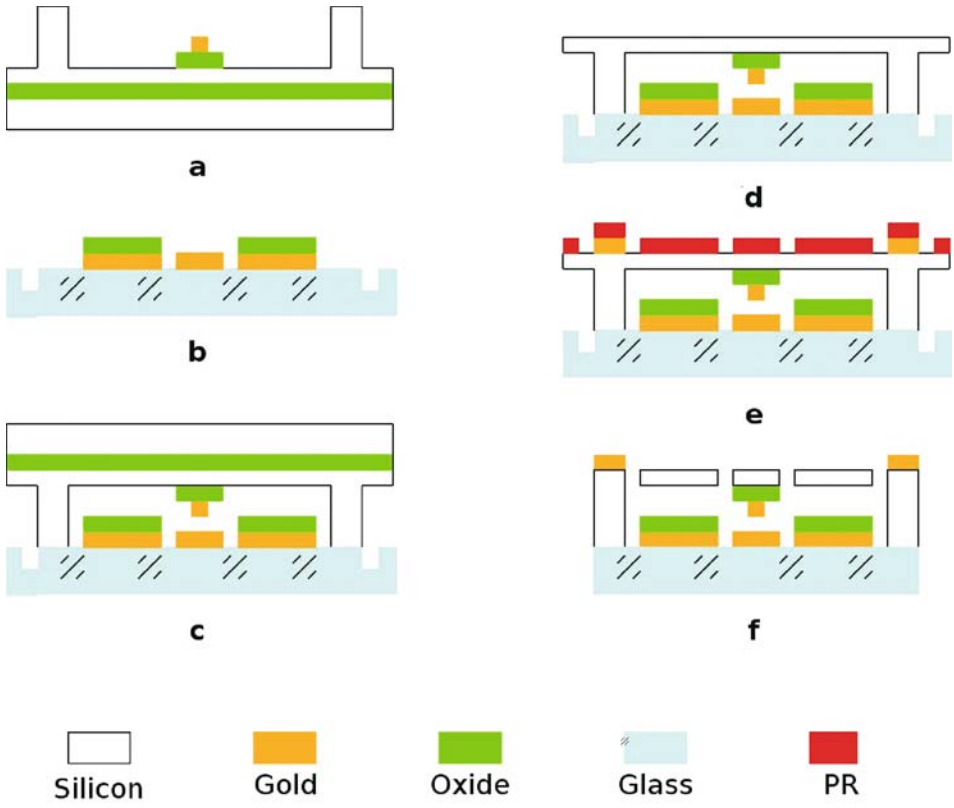

Figure 4. Process flow showing the key steps in the fabrication of the RF MEMS switch. **(a)** Etching the device layer to form a cavity and fabrication of contact dimple. **(b)** Patterning of glass wafer with transmission lines and trenching to half its thickness. **(c)** Anodic bonding of glass and SOI wafers. **(d)** Removal of handle layer and buried oxide. **(e)** Patterning of upper electrode contact pads and actuator structure on device layer. **(f)** DRIE etching to form the actuator, ashing of photoresist and device singulation.

techniques of back side silicon removal would produce non uniformities in the suspension beam thicknesses which would result in deviations from the designed device performance. Metal contact pads for the upper electrodes are patterned after which the photoresist patterning for the actuator structure is carried out, figure 4e. Using DRIE, the 25 μm thick device layer is etched to form the actuator. The resist ashed in an oxygen plasma at 100 W. Wet stripping of resist is avoided to prevent stiction of the actuator structure. The wafer is manually broken along the trench lines on the glass wafer to obtain individual devices as illustrated in figure 4f.

Scanning electron microscope (SEM) images of a typical actuator fabricated by this process is are shown in figure 5. A magnified image of the right hand side drive capacitor is shown in figure 5a. The perforations on the plate are $20 \times 20\,\mu$m in size by design. These are to reduce the 'squeeze film effects' of the surrounding gasses during switch operation. Figure 5b shows the magnified image of the suspension beam taken with sample tilted 10 degrees away from the normal. The image shows the beams to have uniform side walls indicating negligible side effects of DRIE processing such as notching and scalloping. The magnified view of a

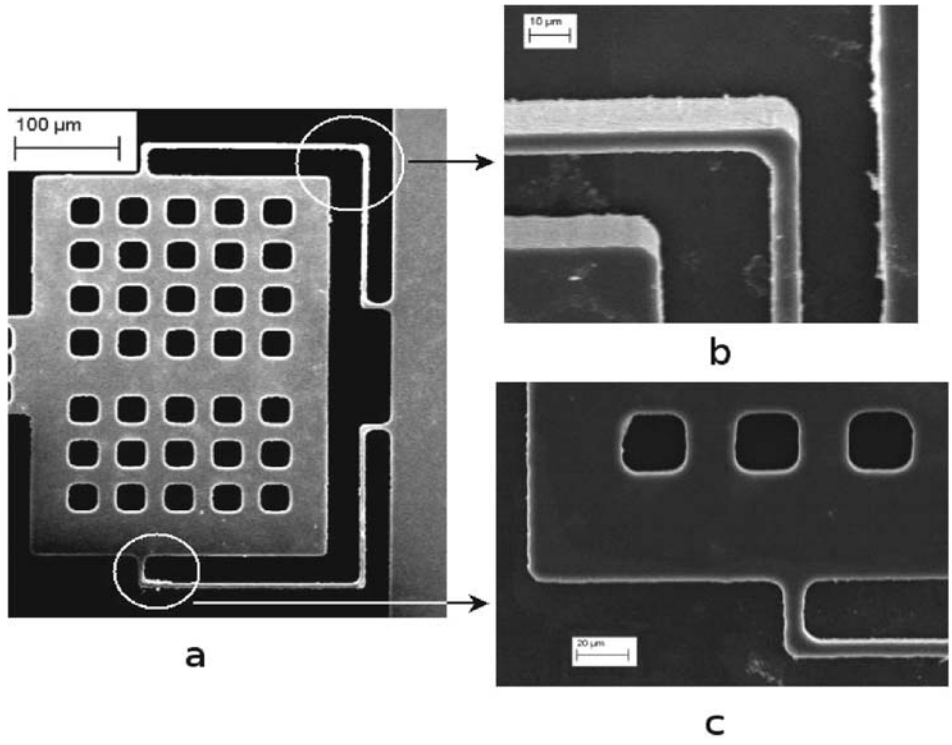

Figure 5. SEM images showing structural details of a typical actuator. **(a)** Magnified view of a drive capacitor illustrating the suspension beams and anchor regions. **(b)** The suspension beams imaged with the sample tilted 10 degrees from the normal, showing smooth taper free sidewalls. **(c)** Detailed view of the suspension beam having a designed width of 10 μm.

suspension beam 10 μm wide by design is shown in figure 5c. The width of the fabricated beam is close to its designed value.

As mentioned before, one of the critical parameters for the operation of the switch is the vertical separation between the transmission line and the contact region. In finished devices this separation can be ascertained by measuring the 'up-state' capacitance and comparing it with the simulated values. On wafer measurements on several devices were made using a probe station connected to a calibrated highly sensitive LCR meter (Agilent 4284A) and was found to be on an average 0·32 pf. This compares well with the simulated value of 0·38 pf indicating the expected separation between the top and bottom electrodes has been achieved.

4. Summary

The work presented in this paper is an account of the on going RF MEMS development which is underway in our laboratory. Initial fabrication runs have been carried out resulting the successful realization of the basic silicon on glass devices. These devices being analysed at the wafer level in terms of their electromechanical and RF characteristics. In addition, a few process and materials modifications are being considered to improve the yield.

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