




Development of indigenous silicon detector and readout electronics for forward electromagnetic calorimeter prototypes

SOURAV MUKHOPADHYAY^{1,3} ^{*}, V B CHANDRATRE^{1,3}, MENKA SUKHWANI^{1,3}, RAMA N SINGARAJU², SANJIB MUHURI^{2,3}, JOGENDER SAINI², SHUAIB A KHAN² and TAPAN NAYAK^{2,4,5}

¹Bhabha Atomic Research Centre, Mumbai 400 085, India

²Variable Energy Cyclotron Centre, Kolkata 700 064, India

³Homi Bhabha National Institute, Mumbai 400 094, India

⁴National Institute of Science Education and Research, Jatni 752 050, India

⁵CERN, Geneva 23, Switzerland

*Corresponding author. E-mail: souravm@barc.gov.in

MS received 25 February 2022; accepted 7 April 2022

Abstract. ALICE is a high-energy physics experiment at the CERN Large Hadron Collider (LHC) in Geneva, to study the properties of quark-gluon plasma, formed in heavy-ion collisions. In the upgrade program, a new electromagnetic forward calorimeter (FOCAL) based on silicon and tungsten (Si+W) sampling configuration, has been proposed to address new physics objectives of ALICE experiment. The high luminosity environment of the LHC and the requirement of compact design for the FOCAL, put stringent requirements for the development of silicon detector and front-end electronics (FEE). The ALICE-India collaboration made the first proposal for the FOCAL in the year 2008, and initiated indigenous R&D activities for silicon detectors, FEE and instrumentation. As a result, large area (40 cm²), segmented silicon pad sensors (6.3 cm × 6.3 cm with 36 pads) and two different FEE application-specific integrated circuits (ASICs), ANUSANSKAR and ANUINDRA respectively, were developed. Progressive FOCAL prototypes were built using these sensors and ASICs, which have undergone test beam validation in a phased manner achieving the desired calorimetric performances, in line with the GEANT-based performance simulations. Further, the results of the test beam experiments provided crucial inputs for achieving the technical specifications of the silicon detector and readout electronics for the final calorimeter. This manuscript presents, in a chronological order, India's indigenous FEE ASICs, sensor and instrumentation development and reports the subsequently improved readout methodology for the prototype FOCAL detector.

Keywords. Forward calorimeter; front-end electronics ASIC; ANUSANSKAR, ANUINDRA; large area silicon detector; small- x physics.

PACS Nos 85.40.Bh; 29.90.+r; 29.40.Wk; 29.40.Vj

1. Introduction

ALICE is one of the largest experiments specialising in measuring the aftermaths of lead ion collisions at ultrarelativistic energies (colliding at a maximum centre-of-mass energy of 5.02 TeV). The heavy-ion collisions are used to probe the properties of quark-gluon plasma generated from such collisions. This quark-gluon plasma matter presumably existed within a few microseconds after the birth of our Universe. The ALICE experiment in the present configuration has optimal coverage in the central rapidity region with the

central barrel but limited detector set-up in the forward directions. To equip the ALICE to address some of the physics topics of interest accessible at forward rapidity, a silicon and tungsten-based sampling type electromagnetic calorimeter, FOCAL, has been proposed [1]. The FOCAL is expected to address the new physics goals, specifically in the small Bjorken- x region. The major physics objectives of the FOCAL during proton-proton, proton-lead and lead-lead collisions can be summarised as

- study of parton distribution functions at low Bjorken- x both in hadron and heavy ions,

- study of the cold nuclear matter effect,
- the energy loss of partons in strongly interacting matter and thus the opacity of the medium formed.

Bjorken- x is expressed as $(p_T/\sqrt{s})e^{-y}$, where p_T is the transverse momentum and y is the rapidity. This scaling variable gives the fraction of proton momentum carried by the parton. At high energies, one probe low Bjorken- x which let the number of quark–antiquark pairs to increase. At small values of Bjorken- x [2], gluons are the dominating partons, resulting in a condensation-like state in the QCD theory of strongly interacting matter. The main observables are photons arising from different stages of evolution of the matter after the collision to probe the new physics. The purpose of the FOCAL detector is to provide optimum position and energy resolution of the photons and differentiate γ from π^0 up to 200 GeV of the incoming particle's energy. The ALICE-India collaboration had made the first proposal for FOCAL, way back in 2008, relying on simulation studies for possible detector geometry and the required performance matrix [1].

A compact design of FOCAL as evolved from the GEANT4 simulation studies [3] consists of tungsten, a highly dense material, used as an absorber/converter material and silicon as an active detection medium. The main aim is to optimise the energy leakage in both the transverse and longitudinal directions to the path of the incident particle and restrict the shower diffusion for possible overlaps under large particle fluence. The EM-shower spread need to be compact (to minimise cluster overlapping) to cope with high particle fluence environments and on the other hand the requirement for detector, front-end electronics (FEE) and their interconnections were kept in mind during the optimisation of the interlayer spacing in the calorimeter using GEANT simulation. Also the space constraints in the experimental cavern warrant compactness, and thus pose challenges in detector design and readout methodology. To optimise the physics requirement and the cost of building the detector, a hybrid silicon detector configuration consisting of high granularity layers (HGL) and low granularity layers (LGL) has been proposed. The objective of HGLs, placed at an optimal position inside the calorimeter with a pixel size of $\sim 1 \text{ mm}^2$, is to provide enhanced tracking resolution. On the other hand, active silicon sensors in the LGLs furnish the energy information when summed up layer-wise, thereby constructing the complete EM shower. A large-area silicon pad sensor, segmented with individual pad size of 1 cm^2 [3], has been finalised for the LGLs of the calorimeter with the requirement of high breakdown voltage and low leakage current. The GEANT4 simulation studies further indicate that for 200 GeV energy incident photons, an individual detector

element in the LGL of the calorimeter will experience a maximum, ~ 1000 MIP (minimum ionising particle) energy deposition, at a depth of shower maximum layer. In addition, the detector is also required to measure a single MIP, well separated from the background. So, a wide dynamic range (ratio of maximum detectable signal to noise floor) is the primary requirement for the FEE to measure MIP and significant energy deposition in and around the shower max layers. Besides, low-power, high-density FEE for a compact calorimeter is essential for a lower thermal budget. Therefore, the simultaneous requirement of low-power, low-noise and wide dynamic range FEE makes the design challenging.

R&D efforts were initiated in India by Variable Energy Cyclotron Centre (VECC) and Bhabha Atomic Research Centre (BARC) collaboration for building the FOCAL prototypes with the development of silicon pad sensors for low granularity layers and associated FEE. Customary to mention that R&D activities simultaneously began at different collaborating institutes for different parts of the calorimeter, e.g., silicon pad development for the LGL layers and FEE, instrumentation in Japan [4], silicon MAPS (monolithic active pixel sensor) prototypes with FEE for HGL in the Netherlands [5].

This paper presents the chronological development of the FOCAL prototype detectors in India and their beamline tests at CERN towards prototype FOCAL development. In §2, the design of the proposed FOCAL is discussed in brief. Development of the large-area silicon pad sensors is reported in §3, and in §4, the design of the FEE ASICs and their salient features are presented. Three beam tests with prototype FOCAL using different readout methodologies and FEE ASICs are highlighted in §5. Section 6 presents the test beam results and §7 concludes the paper.

2. Design of FOCAL

FOCAL is a sampling-type electromagnetic calorimeter with a silicon detector (Si-det) as the active detection medium and high-purity (99.98%) tungsten (W) as an absorber/converter [6]. The target is to achieve adequate energy and position resolutions to handle extremely high particle fluence environments. So, the proposed design consists of 20 alternating layers of silicon and tungsten. Each layer consists of a 3.5 mm thick (one radiation length) tungsten plate followed by a 0.3 mm thick Si-det. The calorimeter, shown in figure 1, consists of three high granular (HGLs) silicon planes placed in the region of the expected shower maxima for accurate position measurements and tracking. These three layers (4, 8 and 12) out of the 20 layers are made of highly granular

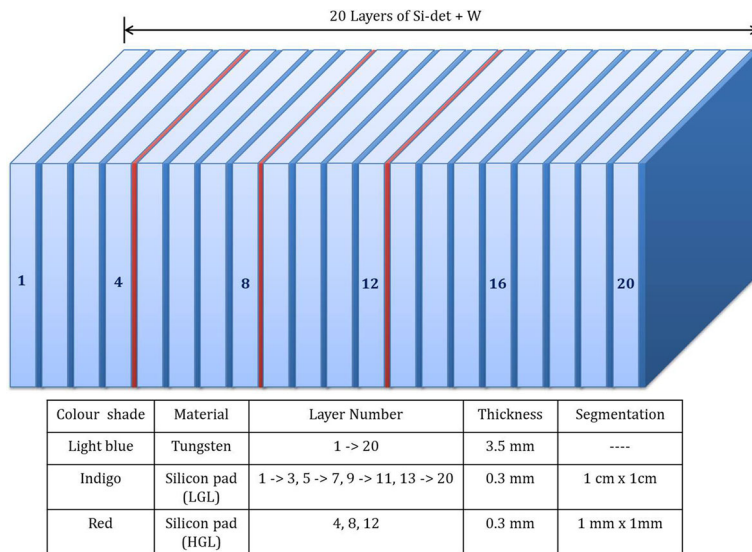


Figure 1. The components of a silicon–tungsten sampling calorimeter consisting of 20 layers of detectors.

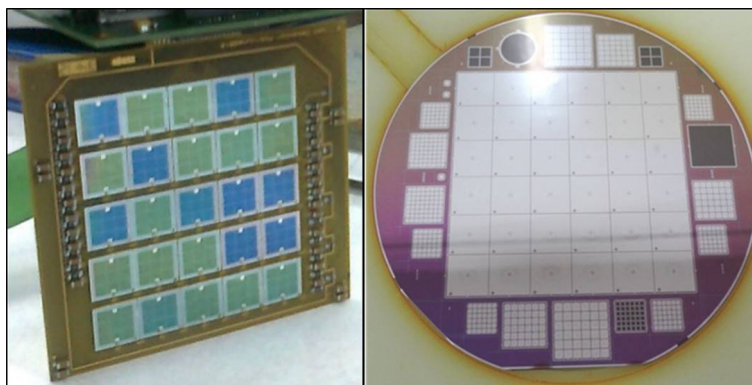


Figure 2. (Left) 5×5 array of individual discrete 1 cm² silicon pad mounted on a single PCB as the first prototype and (Right) fabricated 4-inch high resistivity wafer containing the 6×6 silicon pad in the centre along with the other test structures in the periphery [6,7].

silicon pads, each with a dimension of ~ 1 mm². The rest of the layers (LGLs) are made up of lower granular ~ 1 cm² silicon pad detectors.

For the LGLs of the FOCAL, large-area silicon pad sensors and the two different readout FEE ASICs, namely ANUSANSKAR and ANUINDRA, have been developed in India. The indigenous silicon sensors and readout electronics were used to build the prototype FOCAL detectors, characterised and validated in the laboratory (BARC and VECC) and during the series of test beams (TB1, TB2, TB3) using the CERN beamline facilities. The details of the configuration and test results can be found in [6,7].

3. Development of large-area silicon pad sensors

The activity of building a prototype calorimeter started in the year 2010–2011, involving the development of a

5×5 array silicon pad sensor with individual discrete silicon pad (each pad area = 1 cm²) mounted on a printed circuit board (PCB). The left panel of figure 2 shows the photograph of the first prototype sensor. This was followed up in 2013 with the design of a large-area (~ 6.3 cm × 6.3 cm, 36 pads) silicon pad sensor on a single wafer with high breakdown voltage (>500 V) and low leakage current (<10 nA/cm²) per pixel.

The 6×6 arrays of silicon pad sensors with an optimised individual pad size of 1 cm² were developed on a 4-inch N-type high resistivity wafer (4–5 kΩ-cm) with 300 ± 20 μm thickness [8]. To attain higher breakdown voltage, the pad sensor was designed with three floating guard rings (FGR) along the periphery surrounding the 6×6 pad, 10 μm of metal overhang (MO) over the individual P+ pads and a junction depth of 3 μm. Besides, specific processing steps like intrinsic and extrinsic gettering and backplane ohmic side

processing by the double implantation method were incorporated to realise low leakage current. The detector had been fabricated and packaged at Bharat Electronics Limited (BEL), Bengaluru, India. TCAD studies were done by BARC to optimise the design and process at BEL. The packaged detectors were used to build a series of FOCAL prototypes and characterised extensively in the beamlines [7]. The right panel of figure 2 shows the photograph of a processed 4-inch high resistivity silicon wafer with the 6×6 silicon pad sensor in the centre.

4. Development of FEE ASICs

Indigenous efforts of the ALICE-India collaboration for the development of FEE ASIC had started in parallel to address large dynamic range, low noise readout electronics requirements. The design of the first FEE ASIC, named ANUSANSKAR [6], was started in 2010 and fabricated using $0.7 \mu\text{m}$ CMOS technology. It was a low-power, low-noise FEE ASIC with a dynamic range of $\pm 600 \text{ fC}$. This ASIC achieved better performance in terms of dynamic range than the existing MANAS ASIC [9], which was initially developed for the PMD & Muon Chambers detector in the ALICE experiment and used as one of the FEEs during the FOCAL prototype test. The ANUSANSKAR ASIC was used in the first two test beams (TB1, TB2) [6,7] with MANAS ASIC in 2012 and 2015. However, the test beam data indicate the need for an even wider dynamic range for the FEE. Thus, later in 2016, to cater to the still higher dynamic range requirement, a new ASIC, called ANUINDRA with a dynamic range of $\sim 2.6 \text{ pC}$, was developed using $0.35 \mu\text{m}$ CMOS technology. This ASIC was used in the third test beam (TB3) in 2017 around the expected shower max region for the incident particle energy range, and a significant improvement was achieved. All these ASIC's interfaces are designed to be compatible with the MARC IC [10] used as the controller and CROCUS [10,11] used as DAQ (discussed in the next section) in all the test beams. Salient design features of the ASICs, in brief, are described below.

4.1 MANAS ASIC

MANAS ASIC [9], developed in SCL $1.2 \mu\text{m}$ C1D twin tub process, comprises 16 pulse processing channels with an analogue multiplexed output. Each channel consists of a charge-sensitive amplifier (CSA), pulse shaper, track and hold (T/H) stage. The semi-Gaussian shapers inside MANAS have been implemented through Gm-C filter [12] topology. MANAS ASIC is a modified version of the Gassiplex ASIC [13,14] with a dynamic range from $+500 \text{ fC}$ to -300 fC . Designed with a die area of

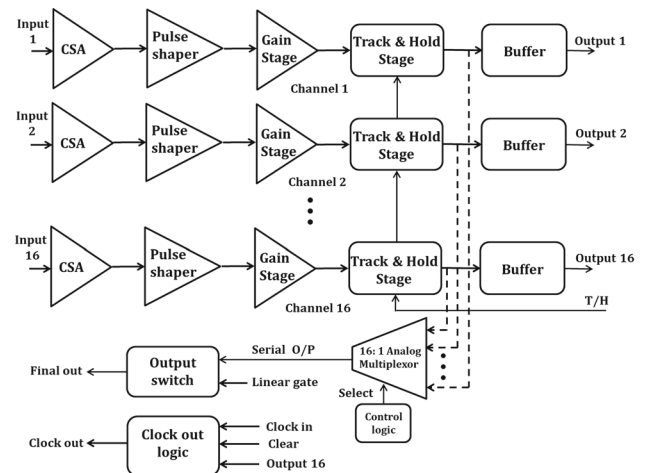


Figure 3. Block diagram of the ANUSANSKAR ASIC.

$2.4 \text{ mm} \times 4.6 \text{ mm}$, the ASIC has been packaged using TQFP 48.

4.2 ANUSANSKAR ASIC

The ANUSANSKAR ASIC [6], developed using standard $0.7 \mu\text{m}$ CMOS technology, incorporates 16 pulse processing channels with individual output along with an analogue multiplexed output, as shown in figure 3. Each channel consists of CSA, semi-Gaussian pulse shapers, T/H stage and output buffer. Inside ANUSANSKAR, the design of CSA is based on the folded cascode architecture, while the feedback resistor was designed using the current conveyor [15] architecture. The CR-RC² like second-order semi-Gaussian pulse shaper using the low noise sallen-key [16] filter architecture and operational transconductance amplifier (OTA), has been implemented inside ANUSANSKAR with a peaking time of $1.2 \mu\text{s}$ (in accordance with CROCUS). The outputs of ANUSANSKAR ASICs can be serially read out through the analogue multiplexer with a clock rate of 1 MHz. The clock out signal can be used for daisy-chaining among the multiple ASICs. All the required control signals, i.e., Clock in, T/H, Clear, for the FEE ASIC, need to be provided externally. The output of the analogue mux (Final out) can be coupled with an ADC for digital conversion. The linear gate signal for the output switch and the control logic for the analogue mux is generated inside the ANUSANSKAR ASIC.

The ASIC has a die area of $5.6 \text{ mm} \times 5.6 \text{ mm}$ as shown in the left panel of figure 4, and has been packaged in CLCC 64. ANUSANSKAR has an enhanced dynamic range of $\pm 600 \text{ fC}$ with respect to the MANAS ASIC.

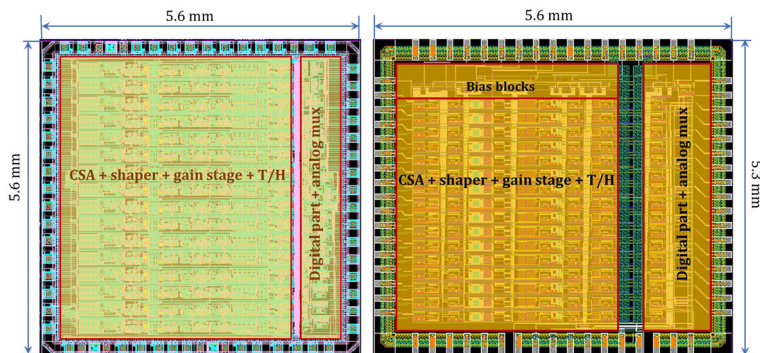


Figure 4. Layout view of the 16 channel pulse processing ASICs. (Left) ANUSANSKAR and (Right) ANUINDRA (dimensions are not to scale).

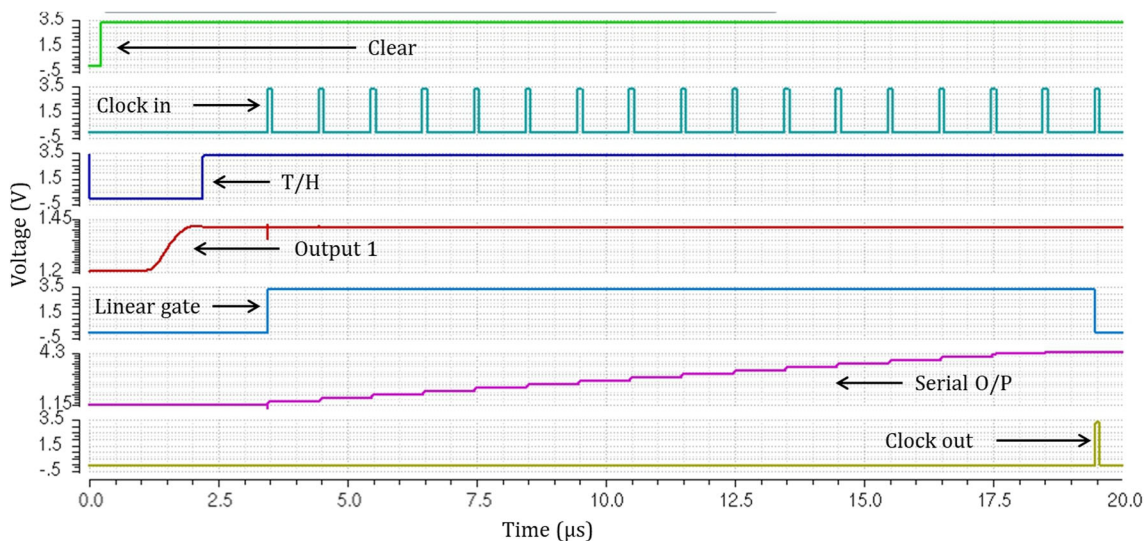


Figure 5. Control signals and simulated final output of the ANUINDRA ASIC.

4.3 ANUINDRA ASIC

The ANUINDRA ASIC was designed using $0.35\ \mu\text{m}$ CMOS technology to cater to higher dynamic range requirements. The ASIC, based on a similar architecture as ANUSANSKAR (as shown in figure 3), comprises 16 pulse processing channels with analogue multiplexed output. All the functionalities and timing performance of the ANUSANSKAR ASIC has been kept intact in ANUINDRA, except with the introduction of wide swing building blocks, as it has to be interfaced with the same DAQ (CROCUS) set-up. A novel charge-sensitive amplifier [17] was designed using a folded cascode architecture and a wide swing current mirror as the load. The value of the feedback capacitor of the CSA was optimised to be $0.8\ \text{pF}$ providing a sensitivity of $1.25\ \text{mV/fC}$. Wide swing current mirror

architecture is chosen as the active load to satisfy the wider dynamic range requirement of the CSA, which reduces the requirement of voltage headroom from $2V_{\text{dsat}} + V_{\text{th}}$ to $2V_{\text{dsat}}$. All subsequent stages like the pulse shaper, T&H stage and the buffers were designed with wide swing architectures. ANUINDRA ASIC is packaged in CLCC 64 with a die area of $5.3\ \text{mm} \times 5.6\ \text{mm}$ (figure 4, right panel). The simulated serial output of ANUINDRA ASIC is shown in figure 5 with all the external control signals. The wide output swing of ANUINDRA ASIC is shown in figure 6. The ASIC has shown a linear response up to $\sim 2.6\ \text{pC}$ of input charge with a $1.25\ \text{mV/fC}$ charge gain (sensitivity). The noise level of 820 electrons has been achieved with a detector capacitance of $0\ \text{pF}$, ensuring an SNR (signal-to-noise ratio) of $\sim 79\ \text{dB}$. Table 1 highlights the salient design features and performance parameters of the indigenously developed FEE ASICs.

Table 1. Comparative analysis of ANUSANSKAR and ANUINDRA from design approach and key performance parameters.

Design aspects/parameters	ANUSANSKAR	ANUINDRA	Remarks
CSA architecture	Folded cascode input stage with self-cascode [18] composite current mirror load	Folded cascode input stage with wide swing current mirror [19] load	Folded cascode architecture is chosen for its high gain and wide bandwidth with minimum no. of active components
I/P transistor type and aspect ratio	P-type and (8000 $\mu\text{m}/1.5 \mu\text{m}$)	P-type and (5000 $\mu\text{m}/0.5 \mu\text{m}$)	Input device plays a vital role in determining the noise performance of the whole amplifier; large area p-type transistor is used as the input device to reduce the flicker noise
I/P transistor properties (g_m and i_{dc})	$\sim 6 \text{ mA/V}$ and $500 \mu\text{A}$	$\sim 7 \text{ mA/V}$ and $350 \mu\text{A}$	The input device biased in the subthreshold region with high current, ensures appropriate transconductance (g_m) to take care of the thermal noise
Feedback resistor	Current conveyor method	Active transistor method	Active transistor-based method provides an additional external control to vary the feedback resistance
Pulse shaper	Sallen-key architecture (Okhawa [20] method)	Sallen-key architecture (Mosher [21] method)	For superlative baseline recovery Mosher method is implemented in ANUINDRA
Overall channel gain	$\sim 3.3 \text{ mV/fC}$	$\sim 1.25 \text{ mV/fC}$	To ensure wide dynamic range, the overall channel gain is kept low in ANUINDRA
Supply voltage	$\pm 2.5 \text{ V}$	+5 V, GND	To have higher dynamic range, high voltage transistors of $0.35 \mu\text{m}$ technology were used in ANUINDRA
Output DC potential (pedestal value)	$\sim 200 \text{ mV}$	$\sim 1.2 \text{ V}$	Due to single polarity supply and to ensure larger positive output swing, the o/p DC potential is optimised towards lower supply voltage in ANUINDRA
Power	$\sim 15 \text{ mW/Ch}$	$\sim 25 \text{ mW/Ch}$	Larger output swing requires larger power dissipation in ANUINDRA
Noise at 0 pF	~ 390 electron	~ 820 electron	Lower overall channel gain in ANUINDRA results in a little bit higher noise but which is low enough for MIP detection
Dynamic range	$\sim \pm 600 \text{ fC}$	$\sim 2.6 \text{ pC}$	Four-fold increase in positive dynamic range
Technology	$0.7 \mu\text{m}$ CMOS	$0.35 \mu\text{m}$ CMOS	

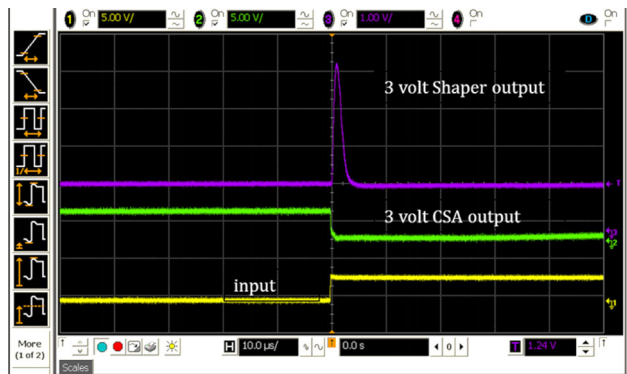
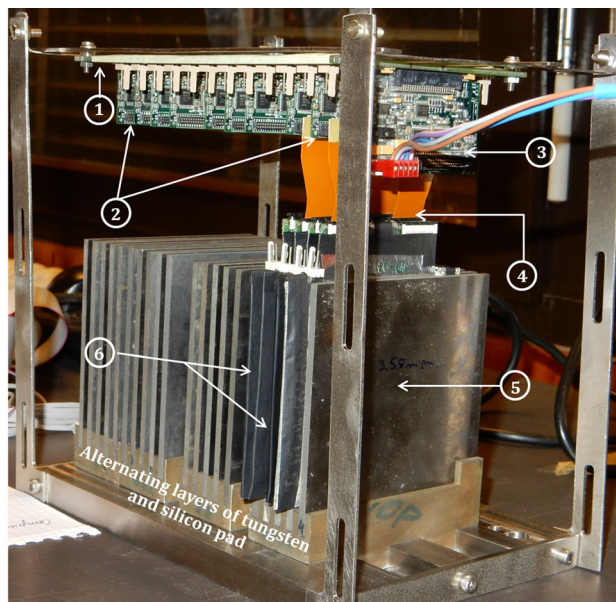


Figure 6. Wide swing output of ANUINDRA ASIC on the oscilloscope (Channel 1 –yellow: 5 V/div, Channel 2–green: 5 V/div, Channel 3–purple: 1 V/div, time-scale: 10 μs/div).

5. FOCAL prototypes and readout methodology

A series of prototypes were developed using the silicon pad sensors, custom-designed FEE ASICs and tungsten plates as the major components. Figure 7 shows a mechanical set-up for the prototype, populated partially with detector layers for visual clarity. Different interfacing boards/cards were designed and utilised in the prototypes, such as detector PCB, readout FEE cards, translator board and backplane PCB. Each card was developed with a specific job: detector PCB to mount the silicon pad sensors, FEE boards to read out the detector signal, translator board to convert the LVTTTL signals to LVDS signals and vice versa, and backplane PCB to mount the FEE boards, the translator board and to distribute the HV signals to the silicon PAD detectors.

The general schematic of the readout methodology, adopted during all the test beams, is illustrated in figure 8. It represents the signal flow chains used during tests at the laboratory and CERN SPS beamlines. The FEE readout cards are mounted on the backplane PCB from the top and connected with the silicon PAD through flexible Kapton cable not to compromise the interlayer gaps and the compactness of the calorimeter. A dedicated trigger set-up, using two pairs of scintillator paddles defining the incoming beam’s X–Y position within the 1 cm² area, and the small finger scintillator (3 mm×3 mm) helps to focus the beam within a single silicon pad. The coincidence signal from the scintillator paddles and the finger scintillator was used to select the beam. Electrons were discriminated using the Cherenkov detector trigger in coincidence with the scintillator paddles. The final trigger signal corresponding to the valid physical event is provided to the cluster read out concentrator unit system (CROCUS DAQ). The Orsay group has developed the CROCUS for the readout of tracking chambers of dimuon spectrometer



1->Back plane PCB, 2->FEE cards, 3->Translator board, 4->Kapton cable coupling FEE with sensor, 5-> Tungsten layers of one radiation length, 6->Silicon sensors packaged in detector PCB and wrapped in black paper.

Figure 7. Photograph of the FOCAL prototype, partially filled with tungsten layers and detector array. Each component is highlighted with a description below the picture.

[10,11] and PMD. It is a crate arrangement that consists of one backplane for the interconnection, which can accommodate 5-FRT (frontal boards) and one CRT (concentrator board). The FRT acts as the interface of the readout electronics via protocol for ALICE tracking chamber (PATCH) bus cable. The main job of the FRT is to load the configuration data to the front-end boards, receive the data from the front-end boards, and, if required, do zero suppression of the data. These data from all the 5-FRTs are sent to CRT for data concentration, where a standard data stream is made and sent to DAQ for storage. The CRT has a provision for trigger input to operate the whole crate in triggered mode. This trigger is then distributed to FRTs and from FRTs to readout boards.

The silicon pad signals are first processed in the FEE board, comprising the FEE ASICs, MARC IC, AD7476 [22]. FEE ASICs provide the multiplexed output of 16 channels after due amplification and shaping. The multiplexed serial output data are then sent to onboard ADC (AD7476) for digitisation. Finally, the data is sent to the onboard IC MARC (developed by INFN Cagliari using 0.6 μm CMOS technology), which performs further processing like zero suppression. MARC IC provides all the necessary control signals for the FEE boards (reset, multiplexor clock, T/H signal) and the ADC (chip select and serial clock). Sets of FEE boards are connected to the translator board via PATCH Bus. The data are sent

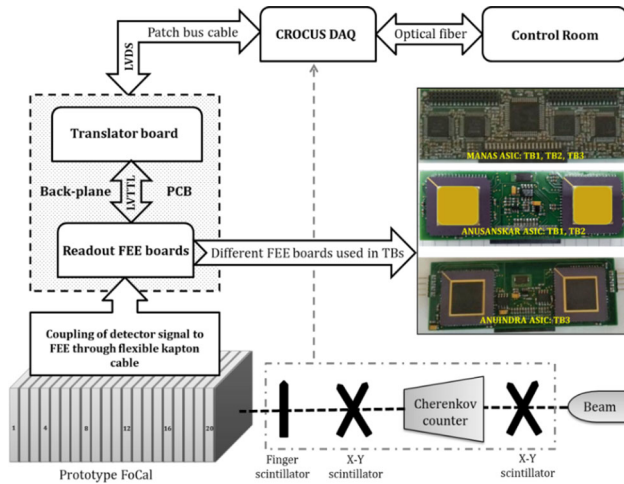


Figure 8. The block chart shows the signal processing from the detector to the DAQ. All the interfacing components are schematically represented in this chart.

in LVTTTL (low voltage transistor–transistor logic) level from the FEE boards to the translator board, where it gets translated to LVDS (low voltage differential signaling) level. The LVDS level signals then reach the CROCUS crate. This CROCUS crate is directly connected to ALICE DAQ situated at the control room with an optical link. The data are then stored and archived for analysis in the final steps.

Three consecutive beamline experiments (TB1, TB2, TB3) have validated the indigenously developed FOCAL prototypes. Depending on their chronological development schedule, three different readout ASICs, MANAS, ANUSANSKAR and ANUINDRA, respectively have been used in these test beams progressively.

5.1 Test beam 1 (TB1): Mini-prototype for FOCAL

A mini-prototype, with four alternately placed layers of detectors and absorbers, was built in 2012 as the first proof-of-concept for the FOCAL prototype [6]. The 5×5 silicon pad detectors were read out using ASIC MANAS and the indigenously developed ASIC ANUSANSKAR. The mini-prototype was tested in the CERN proton synchrotron (PS) beamline during 2012, where the detector's response to pions and electrons of incident energy range from 1 to 6 GeV was studied. The electromagnetic shower, initiated by the incident electrons, was reconstructed and compared with simulated results and found to be in agreement with the predicted data well within the expected errors. The mini-prototype results were encouraging, and validate the experimental set-up, detector architecture, readout methodology, reliability of data acquisition and analysis method. This led

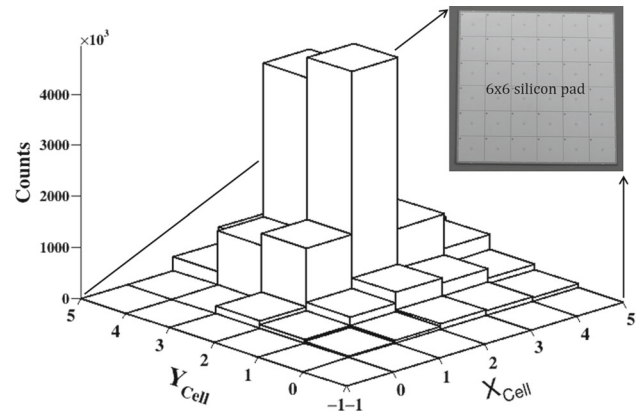


Figure 9. Distribution of energy deposition in a silicon pad layer (10th layer) around the shower max layer with 20 GeV of electron beam.

to the scope for further development towards a full-size prototype with advanced detector and electronics.

5.2 Test beam 2 (TB2): First full-length prototype for FOCAL

Motivated by the successful mini-prototype test results, a 19-layer prototype [7] was built in 2015 using a 6×6 array of 1 cm^2 silicon detectors. Both ANUSANSKAR and MANAS ASICs were again used in TB2 at SPS beamline at CERN. There were two-fold objectives for this test beam: (1) to test the performance of the 6×6 pad sensor, developed first time in India and (2) to find out the capability of the FEE ASICs to handle large energy deposition by high-energy incident electrons.

The prototype was tested in the CERN superproton synchrotron (SPS) with a wide range of incident electron energies from 5 to 60 GeV. Moreover, response with 120 GeV pion beam was also observed to analyse the MIP signal detection capability of the detectors. Figure 9 shows the energy distribution in one of the silicon pad layers (10th layer) around the shower max region for the 20 GeV incident electron beam. The test beam data showed that the limited dynamic range of both the FEE ASICs used in the test beam restrict the performance of the prototype calorimeter and deviate it from the linear region (calibration of output vs. input energy response) beyond 30 GeV. On the other hand, this set-up meets intended calorimetric performances like MIP response, reconstruction of longitudinal shower profile, energy resolution. The test beam provides successful characterisation of the 6×6 silicon pad sensor and indicates the requirement of improved (enhanced dynamic range) readout FEE. This led to the development of the

next generation larger dynamic range ASIC ANUINDRA.

5.3 Test beam 3 (TB3): Second full-length prototype for FOCAL

A full-length (20 layer) FOCAL prototype was built in 2017 with 20 layers of silicon and tungsten, which were read out using the new ASIC ANUINDRA, and MANAS as planned depending on the maximum charge deposition of the layers. This FOCAL prototype was characterised and validated in the SPS-H6 beamline in 2017 with a wider incident energy range, from 20 GeV to 110 GeV electrons. Considering the incident energy range for incoming electrons, the expected maximum energy deposition will be around the shower maximum layers (8 to 12) and found to be about 80 MeV for 50 GeV. However, the total energy deposited will be shared among more than one 1 cm² sensors which are connected to different readout channels in the ASIC. Accordingly, the new ANUINDRA ASICs with a wide dynamic range (2.6 pC) were placed around the expected shower maximum layers (8 to 12), while the rest of the layers were read out using ASIC MANAS as FEE. The configuration was found to perform as intended, even up to 90 GeV of incident energy.

In all the test beams, the MIP signal (observed with a high-energy pion beam) was found well developed and reasonably isolated from the noise [6,7]. The results help to validate the readout methodology and FEE ASICs for their ability to detect low-energy signals with an adequate signal-to-noise ratio. On the other hand, the performance of the last prototype (TB3) with high energy deposition due to EM-shower by incident electron assures its wide dynamic range response. Figure 10 shows the chronological representation of the combination of FEE ASICs used as readout in a series of beamline experiments of the FOCAL prototype.

6. Beam line experiments – results and discussion

As the first step, the baseline response was recorded as the DC pedestal plot for all the detection channels of the prototype FOCAL. Figure 11 represents the mean pedestal response for each channel as recorded in TB3. The range of channels 256 → 416 (Layer: 8 → 12) corresponds to channels read with ANUINDRA ASIC with values ~1200 ADC count (here 1 ADC count corresponds to ~1.2 mV; a 12 bit ADC AD7476 with 5 V reference voltage), an order of magnitude higher than the rest of the channels connected to MANAS (~ 200 ADC count, here 1 ADC count corresponds to ~0.6

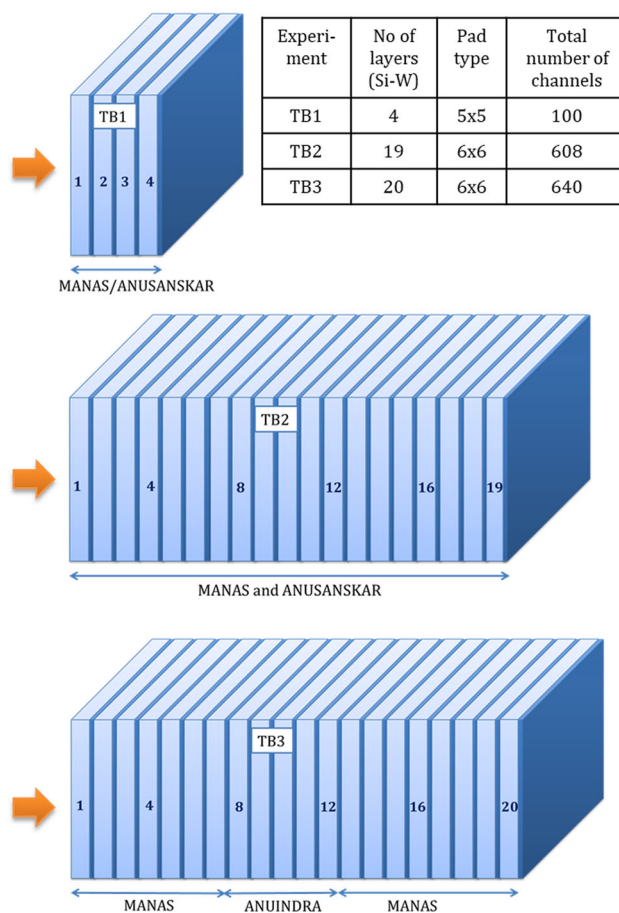


Figure 10. Combinations of FEE readout ASICs used during the three test beams at CERN. The light blue shades symbolise the tungsten layers, while the indigo coloured layers represent silicon pads.

mV; a 12 bit ADC AD7476 with 2.5 V reference voltage). This is because MANAS ASIC was designed with ±2.5 V power supply, while the ANUINDRA ASIC was designed in single polarity supply of +5 V and GND. The importance of the pedestal plot conveys three critical issues,

- the expected value of the pedestal and its uniformity over various channels,
- the RMS value should be as minimum as possible to reflect the low noise level (below that of the minimum detectable signal), and
- the stability of the pedestal over time.

The pedestal values clearly show a uniform pedestal for all the channels. The details of each pedestal response with electronics connected or not connected can be found in ref. [8].

In TB1, the electromagnetic shower response can be partially reconstructed with four layers of mini-prototype for 1 GeV to 6 GeV electrons. A conversion curve for reconstructed energy vs. simulated energy

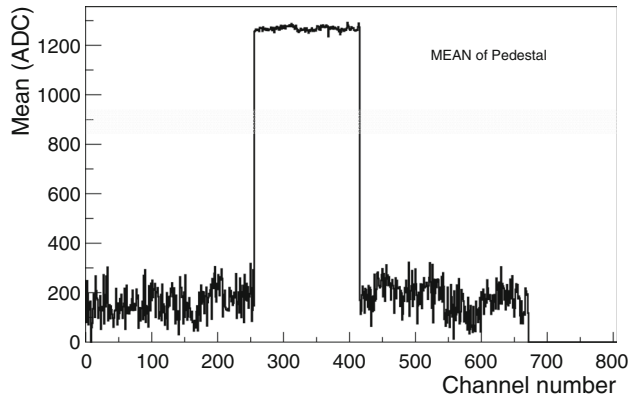


Figure 11. Pedestal mean values from TB3 prototype where both MANAS and ANUINDRA ASICs were used as FEE in combination. The plot signifies uniform mean pedestal values across the readout channels.

deposition was studied in place of the calibration curve due to the lack of substantial numbers of incident energies and layers for the prototype [6]. The first full-scale ($19X_0$ in depth) prototype was tested in TB2 at the CERN-SPS beamline. The prototype was exposed up to an incident electron energy of 60 GeV, while the response was found to be linear up to 30 GeV. The test results indicated the insufficiency of the readout ASICs (MANAS and ANUSANSKAR) to handle large energy deposition beyond 30 GeV and deviate the response from linearity [7]. More specifically, a saturation effect in energy measurement was found at and beyond 30 GeV because of the limited dynamic range of the readout electronics, leading to a scope of further improvement. The third test beam with the full-scale prototype ($20X_0$ in depth) using ANUINDRA ASIC was able to measure EM-shower signal up to 110 GeV of incident electron. The prototype response showed good linearity up to 90 GeV incident electrons and little non-linearity beyond that, thus leaving further scope for upgradation. Nevertheless, the test results were encouraging for the reconstruction of electron energy from the EM-shower for the range $20 \rightarrow 110$ GeV. The profiles were found well distinguishable from each other except in the higher end, where they start getting distorted and overlapped. The improvement in signal reconstruction can be better understood from figure 12, where the MANAS and ANUINDRA ASIC read a PAD sensor at the same transverse coordinate along with EM-shower propagation in two consecutive layers (7 and 8). There is an apparent saturation for EM-shower from 50 GeV electron at layer-7, which was read using MANAS, whereas the ANUINDRA ASIC could handle even larger energy deposition at layer-8 for the same PAD position. It effectively illustrates the efficiency of the new ASIC

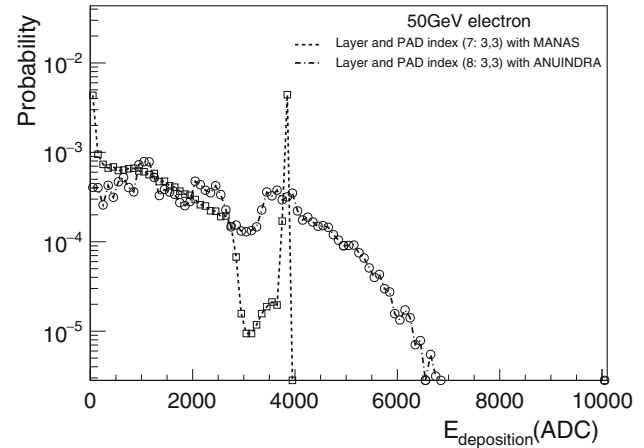


Figure 12. Response of MANAS and ANUINDRA ASIC to 50 GeV electron beam. ANUINDRA ASIC can handle much larger energy deposition than ASIC MANAS as can be seen here.

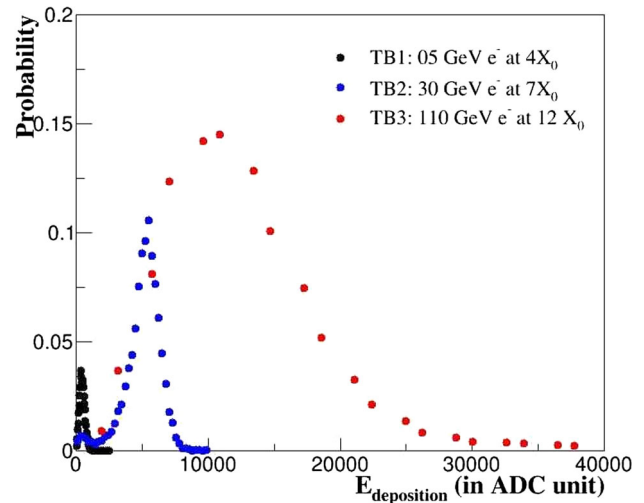


Figure 13. Energy distribution in the shower max layer with higher particle beam energy and subsequent use of MANAS, ANUSANSKAR and ANUINDRA in three test beams (TB1, TB2 and TB3).

ANUINDRA to measure higher energy accurately and to help the calorimeter to be in the linear domain.

The profile for energy deposition by EM-shower for different incident energies from three consecutive test beams is plotted in figure 13, which illustrates the chronological improvement of the detector and readout electronics and thus consistent signal reconstruction. The energy deposition at layer around the shower maximum was picked up for all three test beams, which are 4th, 7th and 12th respectively at 5, 30 and 110 GeV. All the pads are summed together to get the complete layer response which is shown with black, blue and red for TB1, TB2 and TB3, respectively. The energy deposition for a particular layer is expected to be Gaussian and

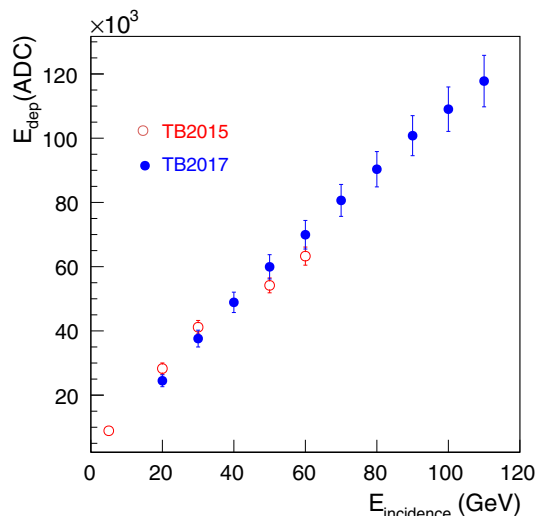


Figure 14. Calibration curve: the reconstructed energy for TB2 and TB3 is plotted against a wide range (5 → 110 GeV) of incident energy.

are nicely developed. However, the profile for 110 GeV shows an elongated tail and distorted Gaussian shape, which can be attributed to the limitation of the readout ASIC at 110 GeV and left the scope for further improvement in the dynamic range to achieve the final goal of measuring 200 GeV incident energy.

The performance of the calorimeter prototype could be better explained with figure 14, where the reconstructed energy by the prototype is plotted against a wide incident energy range (5 to 110 GeV). Figure 14, commonly known as the calibration curve, illustrates the performance improvement beyond 30 GeV in TB3 compared to TB2 with the introduction of a large dynamic range ASIC ANUINDRA. As can be seen, the energy reconstruction follows the same trend except energies beyond 30 GeV for TB2 and beyond 90 GeV for TB3 and can be attributed to limited readout capability.

7. Conclusion

The proposed FOCAL detector, as a part of ALICE upgrade, put forward a challenging requirement of low noise, low power and wide swing FEE and large area silicon pixel detector with high breakdown voltage and low leakage current. Towards that goal, a large area 6.3 cm × 6.3 cm silicon pad sensor on a 4-inch-high resistivity wafer, and two different FEE ASICs namely ANUSANSKAR and ANUINDRA were developed. Both ANUSANSKAR and ANUINDRA are 16-channel pulse processing ASICs with individual and analogue multiplexed serial output. ANUSANSKAR, designed

using 0.7 μm CMOS technology, is a low power, low noise FEE ASIC with an equal dynamic range of ± 600 fC, while ANUINDRA, designed using 0.35 μm CMOS technology, has a linear dynamic range of ~ 2.6 pC. Three different versions of prototype FOCAL detector using the silicon pad sensor as the active detection medium and ASICs as FEE have been built and characterised at CERN up to 110 GeV of electron beam energy. The prototype FOCAL exhibits a linear behaviour up to 90 GeV of electron beam energy with an energy resolution of 20% [23]. The chronological development of the indigenous instrumentation and the subsequently improved readout methodology of the prototype FOCAL detectors, along with the test beam results, have been reported in this paper.

As the motivation is to measure and distinguish the primary photons from the decay photons up to the incident energy of 200 GeV, further improvements with respect to the dynamic range of the readout FEE is required. R&D is underway to achieve the requirement. Similarly, on the detector front with the anticipated radiation load of the LHC environment, the development of a larger area silicon pad sensor on a 6-inch p-type wafer has been initiated.

The R&D work, as reported here, gave us experience on the development of the critical aspects of the sensor and instrumentation for a high-energy physics experiment, e.g., optimising detector geometry, designing the readout methodology, development of high-density low-noise low-power FEE ASICs, handling large data rate, tackling the heating/cooling issues. This has helped to evolve the final FOCAL configuration and requirements in synergy with other collaborators, and identifying our contribution areas in the development of the planned calorimeter.

Acknowledgements

The authors are thankful to Shri C K Pithawa and Prof. D K Srivastava, Dr R K Bhandari, Dr Y P Viyogi for their continuous support during these R&D activities. The authors like to thank fruitful collaboration with Bharat Electronics Limited (BEL), Bengaluru, and in particular, Y P Prabhakara Rao, Y Rejeena Rani and Ranjay Laha. The authors would like to acknowledge all the crew members of the CERN PS and SPS beamlines for the excellent beam quality for the detector test and ALICE-FOCAL collaboration for the help and coordination during the tests. The authors would also like to appreciate the fruitful discussion with Tatsuya

Chujo, Marco van Leeuwen, Thomas Pietzmann, Gert-Jan Nooren, A van den Brink (Ton) during the test beams and their constructive suggestions and help.

References

- [1] Letter of Intent: A Forward Calorimeter (FOCAL) in the ALICE experiment, CERN-LHCC-2020-009 ALICE-PUBLIC-2019-005 06 June 2020, <https://cds.cern.ch/record/2719928/files/LHCC-I-036.pdf>
- [2] Tapan K Nayak, *Nucl. Phys. A* **854**, 230 (2010), <https://doi.org/10.1016/j.nuclphysa.2011.01.026>
- [3] Radha Pyari Sandhir, Sanjib Muhuri and Tapan K Nayak, *Nucl. Instrum. Meth. A* **681**, 34 (2012), <https://doi.org/10.1016/j.nima.2012.04.023>
- [4] Motoi Inaba, Tatsuya Chujo and Masahiro Hirano, *Nucl. Instrum. Meth. A* **824**, 299 (2016), <https://doi.org/10.1016/j.nima.2015.10.055>
- [5] ALICE FOCAL Collaboration, *J. Instrum.* **13**, C03030 (2018), <https://doi.org/10.1088/1748-0221/13/03/C03030>
- [6] S Muhuri *et al*, *Nucl. Instrum. Meth. A* **764**, 24 (2014), <https://doi.org/10.1016/j.nima.2014.07.019>
- [7] S Muhuri *et al*, *J. Instrum.* **15**, P03015 (2020), <https://doi.org/10.1088/1748-0221/15/03/P03015>
- [8] S Mukhopadhyay *et al*, *J. Instrum.* **16**, P09026 (2021), <https://doi.org/10.1088/1748-0221/16/09/P09026>
- [9] Indian chips (MANAS) on track for ALICE, CERN Courier, November 24, 2004
- [10] V Chambert For Alice Collaboration, The electronics of the Alice Dimuon Tracking Chambers, ALICE Internal Note, ALICE-INT-2004-026, 2004, <https://cds.cern.ch/record/1158633/files/p242.pdf>
- [11] ALICE Collaboration, Addendum to the Technical Design Report of the Photon Multiplicity Detector (PMD), ALICE TDR 6, CERN/LHCC 2003-038, 2003, <http://cds.cern.ch/record/642177/files/cer-002399082.pdf?version=1i>
- [12] T Noulis, C Deradonis, S Siskos and G Sarra Bayrouse, *Nucl. Instrum. Meth. A* **589**, 330337 (2008), <https://doi.org/10.1016/j.nima.2008.02.048>
- [13] Technical Design Report of the Photon Multiplicity Detector (PMD), CERN / LHCC 99-32 ALICE TDR 6 30 September (1999), <http://cds.cern.ch/record/451099/files/open-2000-184.pdf>
- [14] J C Santiard *et al*, Gaspex a low-noise analogue signal processor for read out of gaseous detectors, CERN ECP/94-17 (1994)
- [15] R L Chase, A Hrisoho and J-P Richer, *Nucl. Instrum. Meth. A* **409**, 328 (1998), [https://doi.org/10.1016/S0168-9002\(97\)01291-6](https://doi.org/10.1016/S0168-9002(97)01291-6)
- [16] R P Sallen and E L Key, *IRE Trans. Circuit Theory* **2**, 74 (1955), <https://doi.org/10.1109/TCT.1955.6500159>
- [17] Sourav Mukhopadhyay, *Nucl. Instrum. Meth. A* **1028**, 166367 (2022), <https://doi.org/10.1016/j.nima.2022.166367>
- [18] Jasdeep Kaur Dhanoa, Nupur Prakash and S S Rajput, Self cascode current mirrors for low voltage analog circuits, SETIT 2009, *5th International Conference: Sciences of Electronic, Technologies of Information and Telecommunications* (Tunisia, 2009)
- [19] David Johns, Kenneth Martin, *Analog integrated circuit design* 2nd Edn (Wiley, 2011), ISBN: 978-0-470-77010-8
- [20] S Ohkawa, M Yoshizawa and K Husimi, *Nucl. Instrum. Meth.* **138**, 85 (1976), [https://doi.org/10.1016/0029-554X\(76\)90153-1](https://doi.org/10.1016/0029-554X(76)90153-1)
- [21] C H Mosher, *IEEE Trans. Nucl. Sci.* **NS-23** (1976), <https://doi.org/10.1109/TNS.1976.4328243>
- [22] <https://www.analog.com/en/products/ad7476.html#product-overview>
- [23] Sanjib Muhuri *et al*, Test and Characterization of a Prototype for Forward Calorimeter (focal) at CERN SPS Beamline, VECC Internal Note: VECC/2018/001