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Fabrication and characterization of transparent nanocrystalline ZnO thin film transistors by a sol–gel technique

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Abstract. A nanocrystalline zinc oxide (ZnO) thin film-based metal–insulator–semiconductor thin film transistor (MIS TFT) was fabricated by a facile sol–gel technique onto silicon di-oxide/indium tin oxide-coated glass substrates. The microstructural study of the ZnO thin films indicated uniform crystalline growth with typical (002) X-ray diffraction peaks for h-ZnO with a wurtzite structure. The optical transmittance of the ZnO thin films was >80% in the visible region of the electromagnetic spectrum. The field effect transistor (FET) aluminium top contacts were fabricated using suitable shadow masking. The transfer characteristics of a typical ZnO MIS FET revealed nonlinearity in a linear plot. From the slope and crossover, we obtained a first estimate of field effect mobility (μ) and threshold voltage (V_T) of 0.13 $cm^2\ V^{-1}\ s^{-1}$ and 1.03 eV, respectively. The ZnO TFT operated in enhanced mode with n-channel characteristics and the drain current on–off ratio was 10^5. The deposition parameter needs to be optimized to obtain TFTs with a higher modulation ratio and larger field-effect mobility.

Keywords. Zinc oxide; sol–gel; thin film transistor; optical; electrical.

1. Introduction

Thin film transistors (TFTs) are the basic building blocks for microelectronic components that include memory devices, optoelectronic devices and processors since the control electrodes of transistors are responsible for various useful operations like amplification, memory, logic operations, etc. The advent of transparent TFTs could potentially revolutionize the field of electronics, optoelectronics and spintronics, especially for devices with flexible displays and electronic banners, wearable electronics and microelectronic tagging, and biological and medical applications [1]. However, the marketability of transparent TFT devices would depend on the quality of the active semiconductor layer, and the related device parameter optimization. In this regard, zinc oxide (ZnO) is an excellent material of choice for the fabrication of transparent TFTs due to their higher field effect mobility as compared to a-Si and lower deposition temperatures as compared to polycrystalline Si [1]. For better performances of TFTs, both the values of the field effect mobility and on–off ratio should be higher.

Among the various techniques for producing ZnO thin films, having their own merits and demerits, this wet-chemical technique offers a facile method to obtain good quality transparent nanocrystalline ZnO thin films at a relatively low thermal budget. There are several reports of ZnO-based field effect transistor (FET) being fabricated by using a wet chemically deposited ZnO layer. Shin *et al* [2] reported the fabrication of a low temperature solution processed zinc oxide FET by blending zinc hydroxide and zinc oxide nanoparticles in aqueous medium with a field effect mobility between 0.037 and 0.201 $cm^2\ V^{-1}\ s^{-1}$. The on–off ratio was varied between 10^4 and 10^6. Hoffmann *et al* [3] also reported on the ZnO nanoparticle FET device performance. Their devices exhibited a mobility of $10^{-2}-10^{-3}\ cm^2\ V^{-1}\ s^{-1}$. There are also other reports on the ZnO nanostructured FET [4–6]. However, in general, the electrical performance of the FETs is often hindered by poor interface quality with low carrier mobility. Therefore, the deposition of a high quality ZnO thin film at a relatively low thermal budget and optimization of device parameters to optimize the performance of the TFTs are still a challenge to the researchers. In this context, we present here, the results obtained from TFTs fabricated by chemically derived ZnO thin film layers deposited on top of silicon di-oxide/indium tin oxide (SiO_2/ITO)-coated glass substrate. Nanocrystalline ZnO-based TFTs are fabricated by using these ZnO thin films, where SiO_2 and ITO act as the gate insulator and gate electrode, respectively.

2. Experimental

The nanocrystalline ZnO films were deposited on SiO_2/ITO-coated glass substrates and quartz substrates with a dimension of 1 cm^2. For deposition of the SiO_2 layer, commercially available ITO-coated glass (Sigma, Aldrich) with a surface

resistivity of 15–25 Ω per square was used. Prior to deposition, the ITO-coated glass substrates were cleaned by ultrasonicating them in pure ethanol for 30 s. The SiO_2 layer was deposited by radio frequency-magnetron sputtering of a silicon (Si) target (99.99% pure) under appropriate argon (Ar) and oxygen (O_2) atmospheres for 30 min. The films with a thickness of 40 nm were measured *in situ* by using a thickness monitor. SiO_2 deposited in this manner was slightly sub-stoichiometric as indicated by energy dispersive X-ray analysis. The indicative composition was $SiO_{1.6}$. ITO, which is a highly transparent and conducting n-type semiconductor, served as the TFT gate, while the sub-stoichiometric SiO_2 acted as the insulating layer.

To deposit the nanocrystalline ZnO layer, 0.5 M zinc acetate (ZnAc) dihydrate was mixed with 50 ml isopropyl alcohol in a beaker placed on a magnetic stirrer where the temperature could be varied up to 473 K, then 1:1 molar ratio of diethanolamine was added to it and stirring was performed for 1 h at 500 rpm, maintaining the temperature of the solution at 343 K. We then obtained a clear transparent solution. This solution was then spin-coated onto the SiO_2/ITO-coated glass substrate at 500 rpm for 30 s. The spin coating was carried out four times to obtain a transparent ZnO layer with a thickness of 200 nm. These films were then baked in an oven at 523 K under an ambient atmosphere for 1 h to yield a uniform nanocrystalline ZnO thin film layer. The average crystallite size was 24.8 nm as obtained from the X-ray diffraction (XRD) by using the Debye–Scherer formula. The Al top contacts were deposited by an evaporation technique using suitable masking to complete the TFT structure. Al was thermally evaporated in a high vacuum coating unit (HHV smart coat 3.0) where the base pressure was better than 10^{-6} mbar during deposition.

The microstructural characteristics of the ZnO thin films were determined by field emission scanning electron microscopy (FESEM) (Quanta FEG 250) operated at 25 keV, while the crystalline growth and orientation were verified by XRD patterns measured using a PANalytical X-PERT PRO diffractometer consisting of a goniometer with the ability of variation of 2θ with an angular precession of 0.001°. The transmittance measured at room temperature using a UV–VIS–NIR spectrophotometer (PerkinElmer LAMBDA 750) was used to determine the band gap of the material and its transparency in the visible range (300–800 nm). Thereafter, the electrical characteristics of the TFT were studied by measuring its gate, transfer characteristics and source–drain characteristics using a source meter (Keithley 2450). The results obtained are discussed below.

3. Results and discussion

A representative scanning electron microscopy (SEM) micrograph of the ZnO thin film is shown in figure 1a. The SEM indicated a uniform, well-dispersed nanocrystalline layer with excellent substrate coverage. The histogram (inset of figure 1a) of the particle size showed a normal distribution with a peak at ∼27.4 nm when fitted with a Gaussian distribution plot. The XRD pattern (figure 1b) of the given sample indicated an intense peak at $2\theta = 34.4°$, corresponding to the reflection from the (002) plane along with three other small peaks at 36.4, 47.8 and 63.0° which correspond to the (101), (102) and (103) planes, respectively, of h-ZnO (JCPDS card no. 4-0416). The average crystallite size (D_{av}) of the ZnO grains was estimated from the XRD patterns using the Scherrer relationship [7]:

$$D_{av} = K\lambda/\beta \cos\theta, \tag{1}$$

where the constant $K = 0.9$, β is the full-width at half maximum of the diffraction peak and θ is the corresponding Bragg's angle of reflection from the (*hkl*) planes. The average crystallite size as estimated from the diffraction peak

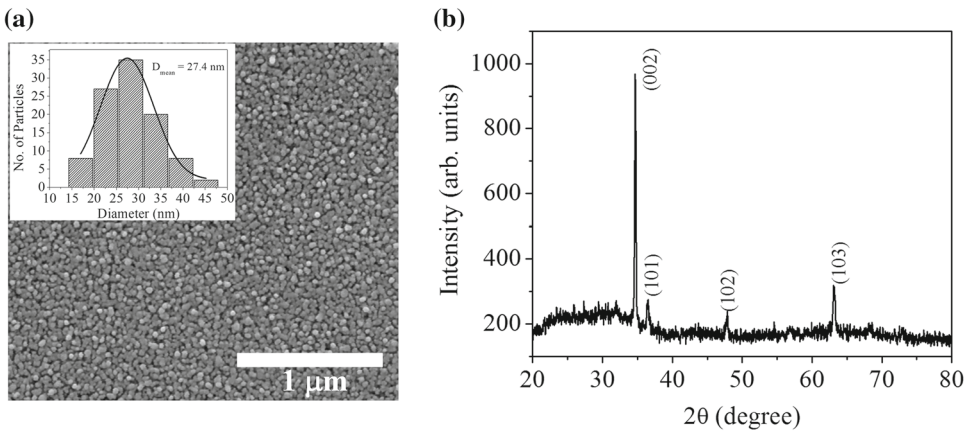

Figure 1. (**a**) FESEM image of the ZnO thin film on a glass substrate. Inset: histogram of the distribution of particle size. (**b**) XRD pattern of the ZnO thin film.

corresponds to the reflection from the (002) plane using equation (1), is ∼24.8 nm.

A representative transmittance plot (figure 2) indicates a transmittance >80% in the whole visible range (400–800 nm). This was observed for all the films, indicating that the films were highly transparent in the visible region. The optical absorption coefficient (α) may be written as a function of photon energy ($h\nu$) as $\alpha = (A/h\nu)(h\nu - E_g)^m$, where A is a constant, dependent on the material, E_g is the band gap and m is a constant indicating the nature of transition. Here, we estimated the absorption coefficient (α) from the experimentally measured transmittance (T) spectrum (T *vs.* λ) using the relationship: $\alpha(\lambda) = \ln(1/T)(1/t)$, where t is the thickness of the film. The optical band gap was calculated by extrapolating the straight-line portion of the plot of $(\alpha h\nu)^2$ *vs.* $h\nu$, to $\alpha = 0$ (inset of figure 2) [8]. The computed band gap was $E_g = 3.32$ eV (at room temperature). The thickness of the ZnO layer was estimated to be ∼200 nm from the transmittance spectrum of the ZnO thin film on a glass substrate using the theoretical model based on Kramers–Kronig theory as proposed by Bhattacharyya *et al* [9].

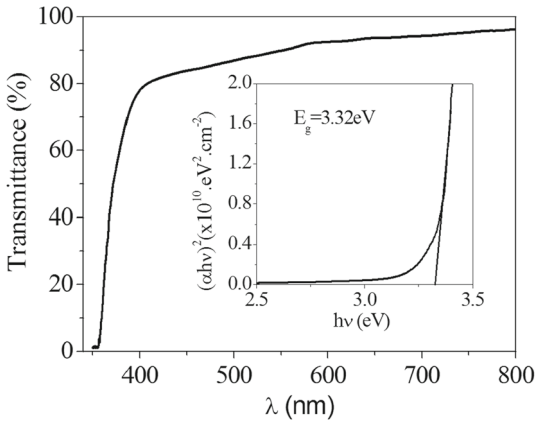

Figure 2. Transmittance spectra of the ZnO thin film. Inset: Tauc plot for the determination of the optical band gap of ZnO.

Figure 3a and b shows the direct current drain voltage–drain current ($V_{DS}-I_{DS}$) plot for a representative ZnO TFT. It exhibited a general n-channel enhancement mode operation; since, a positive gate voltage was required to obtain a conducting channel and also the conductivity of the channel increased with an increase in the positive voltage. The device operated in an enhancement mode, since the device turned off upon the removal of the applied gate bias voltage. This mode is preferred over depletion mode operation because of the ease of circuit design and minimum power consumption. This plot also indicated current saturation and small non-linearity in the linear region. The non-linear behaviour of the entire curve near $V_{DS} = 0$ V may be attributed to the non-linear source/drain contact resistance between the ZnO layer and the metal source contact and to the thermal excitation (due to the Poole–Frenkel field) originating from the deep lying states [10]. One may note that the small drain source current could simply be due to the thick insulating layer used in this MIS structure (40 nm). However, it has been reported earlier [11] that the electrical characteristics of ZnO TFTs strongly depend on the oxygen content in these thin films. It was demonstrated that the ZnO TFT deposited in a low oxygen environment during deposition yields lower current. Since, in our case, the deposition was carried out in aqueous medium, these samples could lack oxygen, which could have led to the small current observed in the source–drain and transfer characteristics. However, by increasing the channel width (Z) to length (L) ratio of the transparent TFT, I_{DS} can be increased since the drain–source current is directly related to this ratio. It was observed that with an increase in the gate voltage, V_G, the saturation region shifted toward higher drain–source voltage, and induced a non-zero I_{DS} at $V_{DS} = 0$ V. From the transfer characteristics of the ZnO TFT (figure 4a), the estimated maximum drain current on–off ratio was $\sim 10^5$ for $V_{DS} = 3$ V. The transistor transfer characteristic curve indicated a non-linearity in the linear plot. Hence, it was difficult to

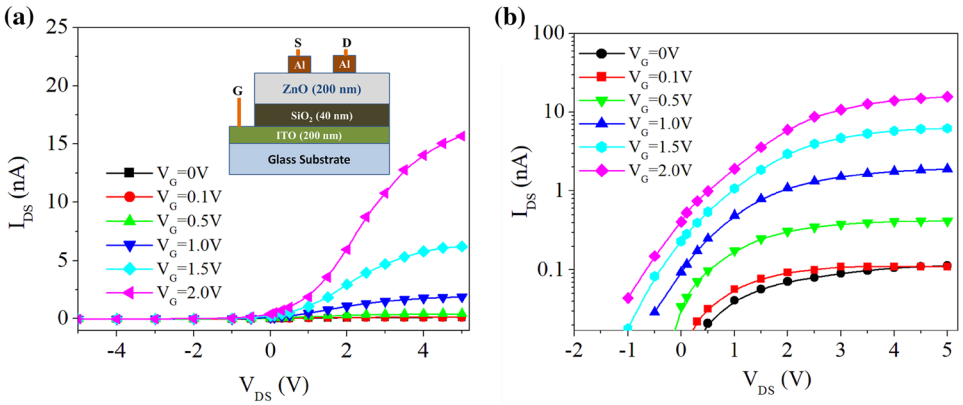

Figure 3. (**a**) Source–drain ($I_{DS}-V_{DS}$) characteristics of a representative ZnO TFT. Inset: schematic diagram of the fabricated device and (**b**) $\log(I_{DS}) - V_{DS}$ plot of the TFT device.

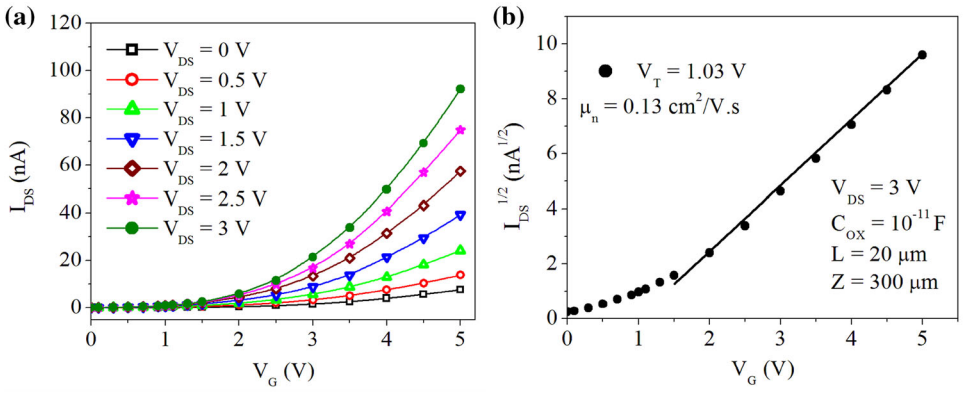

Figure 4. (**a**) Transfer characteristics of a representative ZnO TFT and (**b**) $I_{DS}^{1/2}$ *vs.* V_G plot of the same ZnO TFT.

obtain a unique slope and intercept from which the field-effect mobility (μ) and threshold voltage (V_T) can be obtained. This kind of behaviour is observed when there is a large density of trap states as compared to density of free carriers [11]. Usually, it is considered that the parametric field-effect mobility, μ increases with the gate voltage as $\mu \propto (V_{GS} - V_{th})^{\gamma}$, where V_{GS} is the gate–source voltage, V_{th} is the threshold voltage and γ is an empirical parameter defining the variation of the mobility with V_{GS}. Now, the drain current in the linear region, i.e., for small drain voltage and for $V_{GS} > V_{th}$ is then given by $I_{DS} = k(V_{GS} - V_{th})^{1+\gamma} V_{DS}$, where $k = \mu_o C_{OX} Z/L$, where μ_o is an empirical parameter and C_{OX} is the oxide capacitance per unit area [10]. The $C_{OX} = \varepsilon_{OX}/d$, where ε_{OX} being the oxide (insulator) dielectric constant with a value of 15 [12] and d is the insulator thickness. A straight line graph was obtained by plotting $I_{DS}^{0.5}$ *vs.* V_G (figure 4b) and it yields a threshold voltage, $V_G = 1.03$ V and the corresponding $\mu = 0.13$ cm^2 V^{-1} s^{-1}. The value of the field effect mobility (μ), obtained here, is consistent with the reported value for undoped ZnO-based TFT by Hoffman *et al* [12]. Here, it may be noted that the value of the threshold voltage is directly proportional to the thickness of the gate insulator and accordingly, this thickness can be varied to vary the threshold voltage desirably. Cheng *et al* [13] reported the fabrication of a thin film transistor using ZnO thin films deposited by the sol–gel technique where the gate insulator (SiN_x) layer was much thicker (300 nm) compared with our result (40 nm) that resulted in $V_{th} = 6$ V, $\mu = 0.67$ cm^2 V^{-1} s^{-1} and the on–off ratio being $>10^7$. Jung *et al* [14] reported a solution-processed flexible ZnO TFT with $V_{th} = 0.89$ V, $\mu = 0.32$ cm^2 V^{-1} s^{-1} and the on–off ratio $\sim 10^5$. The field effect mobility can be varied significantly by metal doping in the ZnO layer and using hybrid ZnO structures [15–18]. The C_{OX} was computed here to be about 10 pF m^{-2}. Interestingly, as the formation of an electron channel at the channel/gate insulator (SiO_2) controls the operation of these surface channel devices, it is not expected that the electrical properties will depend on the thickness of the ZnO layer as long as it is significantly greater than the thickness of the induced electron channel which can be of the order of few nanometres. Although the preliminary report is encouraging, further investigation is required to understand the mechanism of operation of TFTs and to optimize the parameters for the better performance of the device. The role of the trap states at the interface also needs to be studied critically. Figure 5 shows a schematic band diagram of the MIS structure of the ZnO-based TFT using a thin SiO_x insulating layer under a positive gate bias voltage. When the gate bias voltage (V_g) is positive, electrons in the n-type ZnO are attracted towards the gate, but the large potential barrier due to the insulator results in the accumulation of electrons at the semiconductor–insulator interface. As a result, the band bends downward at the interface of SiO_x/ZnO. When the applied gate voltage is sufficiently large ($>V_T$), the induced accumulated electrons create a conduction channel at the interface. With an increase in the gate bias voltage, the conduction channel width increases resulting in a higher saturation value of I_{DS} as observed in output characteristics (figure 3).

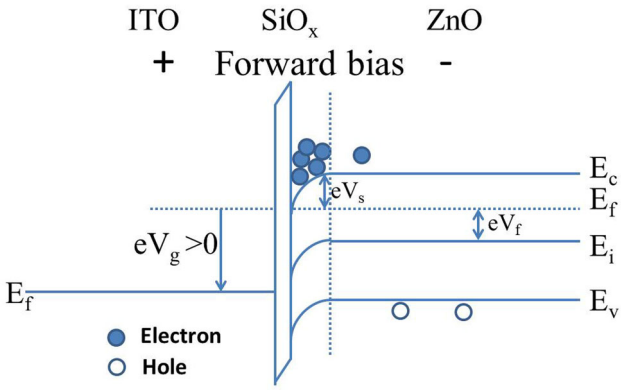

Figure 5. Schematic energy band diagram of the ZnO-based MIS TFT under a forward bias.

Finally, we must also consider the role of sub-stoichiometry and oxygen vacancy of the SiO_2 insulating layer in dictating the carrier transport through the transistor and its contribution towards the breakdown in the insulator cannot be

underestimated. *Ab-initio* studies indicate that oxygen vacancies in SiO_2 behave as electron traps [19]. When a bias voltage is applied, the electrical stress causes the injection of electrons into the oxide layer. The Kohn–Sham (K–S) trap states in the sub-stoichiometric SiO_2 film related to the oxygen vacancy (located below conduction band maxima) that traps these electrons and gradually get filled up. These electrons trapped at the K–S states are believed to aggravate the dielectric breakdown, thus, affecting the device performance [20]. Munde *et al* [21] recently reported on the diffusion and aggregation of oxygen vacancies in relation to dielectric breakdown in amorphous silica by using density functional theory observed that the oxygen vacancies could indeed trap up to two extra electrons. However, they also observed that the efficiency of the diffusion channel decreased significantly because the electrons trapped at the vacancy states ionized thermally before any effective diffusion could take place. In another recent study, Gao *et al* [22] concluded that the two electrons trapped at the intrinsic electron traps could lead to the formation of Frenkel pairs, which are made of oxygen vacancy and O^{2-} ions with a low energy barrier. The application of bias in the transistor device further reduced this energy barrier. Studies detected oxygen emission during the application of the electric field [23], leading to the oxygen vacancy and interstitial oxygen production. This phenomenon could be explained by the observation of Gao *et al* [22]. Munde *et al* [21] demonstrated that both neutral oxygen vacancies and intrinsic electron traps having a close charge transition level could contribute to the trap-assisted tunnelling in α-SiO_2, which could lead to the formation of an electron percolation path through the insulator. With the application of bias, these percolation channels could greatly assist in current flow through the oxide and formation of newer neutral oxygen vacancies thus, contributing to breakdown. Zhu *et al* [24] observed that for their AlGaN/AlN/GaN high-electron mobility transistors with the introduction of a 100 nm SiO_x layer (x between 1.10 and 1.71, both inclusive), the passivation effect led to an increase in the product of the sheet carrier concentration and electron mobility. Furthermore, both the gate and drain leakage currents first decreased before increasing again with an increase in oxygen content of the SiO_x layer. They observed the lowest gate leakage current for the device at $x = 1.23$. This value was 20 times lower than the unpassivated devices. For $x = 1.23$, the breakdown voltage of the SiO_x layer also increased from 99 to 151 V as compared with that of the unpassivated device. It will be very hard to quantify exactly the extent to which the lack of stoichiometry of the insulating layer affected the carrier transport in our device, but it may be broadly stated that it could lead to enhanced current leakage through the SiO_2 insulating layer and the effect could be more pronounced with an increase in the gate voltage, thereby leading to degradation in device performance and a lesser degree of device control. Further investigation is required in this regard and could be the subject for a detailed study in the future.

4. Conclusion

We have characterized ZnO films deposited by a simple and cost-effective sol–gel method and measured the electrical characteristics in a field-effect structure. A strong non-linearity in the transfer characteristic does not allow us to exactly compute the field effect mobility (μ). The non-linearity, characterized by an empirical γ factor, depends on the dielectric–semiconductor interface. In future, we can use the variation of the γ factor to monitor the improvement of both the interface and the zinc oxide film quality.

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