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Effect of Sintering on Grain Boundary Microstructure and Electrical Properties of $CaCu_3Ti_4O_{12}$ Ceramics

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Abstract: $CaCu_3Ti_4O_{12}$ ceramic with a giant dielectric constant was synthesized by sol-gel method and sintered in three different sintering conditions: 1 035 ℃ for 48 h, 1 080 ℃ for 3 h and 48 h. The phase of the ceramics, the element distribution, the valance state of Ti ions at grain boundaries, and the electrical properties were characterized via X-ray diffraction (XRD), energy dispersive X-ray analysis (EDAX), X-ray photoelectron spectroscopy (XPS), electrical conduction and dielectric measurement. The results demonstrate that the grain-boundary microstructure and the electrical properties are influenced by sintering conditions: ① By raising sintering temperature, the Cu-rich and Ti-poor grain boundary was formed and grain resistivity was decreased. ② By prolonging sintering time, the content of Ti^{3+} near the grain boundary increased, leading to the decrease of the grain-boundary resistivity and the increase of the activation energy at grain boundary. The ceramic, sintering at 1 080 ℃ for 48 h, exhibited a small grain resistivity (60.5 Ω • cm), a large grain-boundary activation energy (0.42 eV), and a significantly enhanced dielectric constant (close to 1×10^5 at a low frequency of 1×10^3 Hz). The results of electrical properties accord with the internal boundary layer capacitor model for explaining the giant dielectric constant observed in $CaCu_3Ti_4O_{12}$ ceramics.

Key words: $CaCu_3Ti_4O_{12}$; sintering; microstructure; electrical conduction; dielectric

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0 Introduction

$CaCu_3Ti_4O_{12}$ (CCTO) ceramic possesses an ultra-high dielectric constant (about 1×10^4-1×10^5) with a good temperature stability near room temperature [1,2]. However, unlike other oxide-based perovskite compounds, such as $BaTiO_3$ and $CaTiO_3$, a long-range ferroelectric order has not been observed in CCTO, and the related mechanism about this unusual dielectric property is still debated. For example, Subramanian *et al* [3] believe that the ultrahigh dielectric constant may originate from the distortion of TiO_6 octahedral, Zhu *et al* [4] and Delugas *et al* [5] suggest a nano-sized Ca-Cu disorder mechanism. However, most authors[6, 7] thought that the unusual dielectric behavior can be well explained by the internal boundary layer capacitor (IBLC) model.

According to the IBLC model, CCTO ceramics are composed of n-type semi-conductive grains and insulating grain boundaries. This composite structure can be reckoned as a complex circuit, which consists of two sets of parallel elements (a resistor and a capacitor) connected in series, one set of elements is contributed from grains, and the other is from grain boundaries. A giant grain-boundary polarization is formed due to this complicated structure, resulting in a giant dielectric constant[8]. Therefore, dielectric properties of CCTO ceramic are strictly related with physical properties both in grains and at grain boundaries. For example, it is reported that doping Mn^{4+} or Fe^{3+} at Cu site can greatly depress dielectric constant as a result of the reducing content of conductive Ti^{3+} [9-11], which are formed due to oxygen vacancies or cation nonstoichiometry[12]. It is also observed that the addition of some oxides, such as TiO_2[13],

ZrO_2[14], CuO[15], or Bi_2O_3[16], can form different grain-boundary phases. In addition, in our previous work[17, 18], we had found out that replacing a very small amount of Ca^{2+} by Rb^+ can also impact the grain-boundary behavior, resulting in the formation of Cu-rich and Ti-poor grain boundaries.

Besides the above methods for manipulating chemical composition, in recent years, the properties of grains and grain boundaries had been tuned through some other routes, such as the synthesis of CCTO grains using some chemical methods [19,20] and the CCTO nano-ceramics by sintering the prepared CCTO nano-grains[21-23]. Whatever routes were applied, the sintering treatment was very important to the element distribution and physical properties of grains and grain boundaries. Till now, some special sintering methods, such as spark plasma sintering[24] and microwave sintering[25] have been used to fabricate the CCTO ceramics. Besides these special sintering methods, sintering conditions can make a considerable impact on properties in grains and at grain boundaries as well. For example, it is observed that the sintering in O_2 or N_2 atmosphere can significantly change dielectric constants due to the varied oxygen vacancies in grains[26,27]. Additionally, it is reported that sintering at a high temperature for long time is good for the formation of Cu-rich grain-boundary phases and impacts dielectric properties[28-30].

It is noteworthy that besides chemical composition of grain-boundary phases, electronic structures, such as valance states of ions at grain boundaries, are also vital to electrical properties of CCTO ceramics. The investigation on the evolution of electronic structures of grain boundary phases with sintering conditions may be helpful to reveal the mechanism about the relationship between electrical behaviors and sintering conditions of CCTO ceramics. However, the related work has not been reported.

In this work, the CCTO ceramics were sintered in different conditions. We observed an interesting phenomenon that the manipulation of sintering conditions makes a great impact on the valance state and composition distribution at grain boundary. The related electrical properties are also studied in detail.

1 Experimental Procedures

1.1 Synthesis Method

The CCTO ceramic was prepared with sol-gel method followed by a sintering treatment. All the raw materials are of analytical grade.

First of all, a beaker of blue solution containing the stoichiometric amount of $Ca(NO_3)_2 \cdot 4H_2O$ and $Cu(NO_3)_2 \cdot 3H_2O$ in ethanol was prepared. Under stirring, the blue solution was added into a beaker of yellow solution that was prepared by dissolving the stoichiometric amount of tetrabutyltitanate in the mixture of absolute ethanol and acetic acid (V(tetrabutyltitanate): V(absolute ethnol) : V(acetic acid)=1 : 1.2 : 4, V means volume). Secondly, the obtained sol was put into an oven and heated at 200 ℃ for 2 h, the dry gel was then heated at 700 ℃ in air to remove residual organics, and the obtained powders were calcined at 1 035 ℃ for 48 h in air. Finally, after being well ground, the powders were pressed into disc-shaped pellets under a pressure of 20 MPa by a conventional cold-pressing technique (electric tablet machine, DY-30). All pellets are about 1 mm in thickness and 15 mm in diameter, these pellets were sintered at 1 035 ℃ for 48 h, 1 080 ℃ for 3 h and 48 h, respectively. According to the sintering conditions, the obtained ceramics were named 1035-48, 1080-3, and 1080-48, respectively.

1.2 Characterization

The phase composition of these ceramics was characterized by an X-ray diffraction (XRD) equipment (D8-Advanced, Cu K_α radiation), the lattice constants were determined by Bragg equation. A scanning electron microscopy (SEM, FEI Sirion Field Emission Gun) equipped with an energy dispersive X-ray analysis (EDAX) was used to observe the morphology of ceramic surface and to study the composition variation from a grain to grain boundary. To investigate the valance state of Ti ions at a grain boundary, the ceramics were crushed and the cleaved surfaces were detected by an X-ray photoelectron spectroscopy (XPS, VG Multilab 2000). To measure the electrical properties, the ceramics were polished and pasted with silver electrode materials on both sides, and then the ceramics were annealed at 650 ℃ for 0.5 h to form the electrode. The DC current density-electric field strength (J-E) measurement was extracted by an electrometer (Keithley 6517A) at room temperature. The complex planes of impedance were measured at different temperatures from 100 Hz to 10 MHz by a precision impedance analyzer (WK 6500B). The dielectric measurement was carried out on a precision impedance analyzer (Agilent 4294A) at room temperature from 1 000 Hz to 100 MHz.

2 Results and Discussion

2.1 Phase, Morphology and Element Distribution

Figure 1 shows the XRD patterns of samples 1035-48, 1080-3, and 1080-48. Most peaks can be indexed from the JCPDS card of CCTO (No. 75-2188). To be more specific, little second phase was detected in samples 1035-48 and 1080-3. In sample 1080-48, however, a small content of anatase-TiO_2 phase was detected (labeled as *), and the peak intensity for CCTO reduced clearly. The result of XRD reveals that sintering at a temperature as high as 1 080 ℃ for long time may result in the decomposition of a small amount of CCTO in the ceramic.

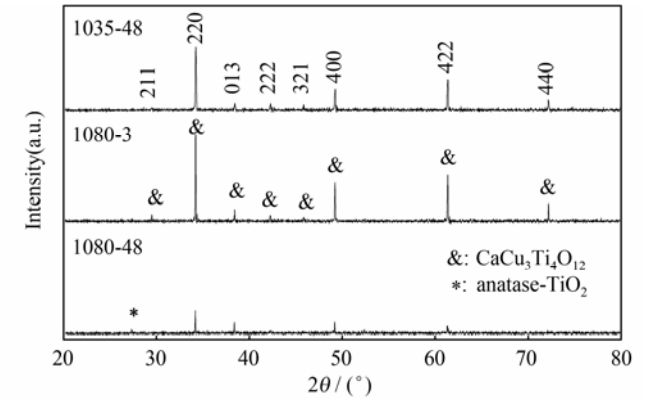

Fig. 1 XRD patterns of the CCTO ceramics sintered at three different conditions

The SEM images of surface morphologies are shown in Fig. 2. For samples 1035-48 and 1080-3, the grain sizes are between several μm and tens of μm, while for sample 1080-48, the grain sizes are larger. The SEM characterization shows that prolonging sintering time is helpful to the growth of CCTO grains.

The EDAX characterization was performed to detect the variation of element content across two neighboring grains. For the three samples, the variation of the content of Ca, Ti and Cu ions are also shown in Fig. 2(a)-2(c), respectively. For sample 1035-48, the content of Ca, Cu, and Ti ions do not show clear variation from one grain to another. For sample 1080-3, the content of Cu ions near the grain boundary is a little larger than that in the grain, but the content of Ti ions at the boundary is a little smaller. As to sample 1080-48, the Cu-rich and Ca/Ti-poor boundaries are clearly observed. Although many Cu ions are detected at the grain boundary, no second phase containing Cu was detected by XRD, which indicates the amorphous state for the grain-boundary Cu-rich phase.

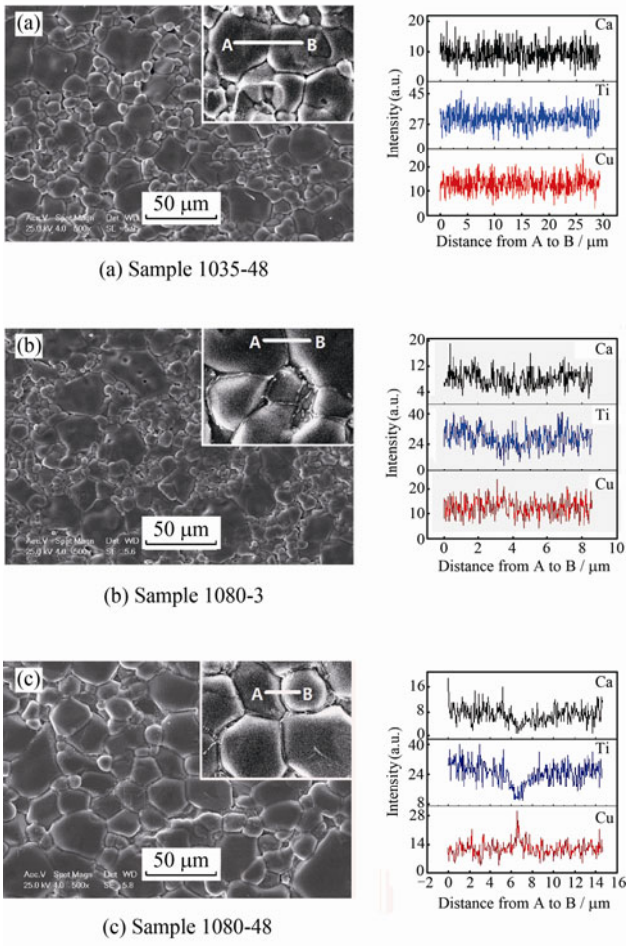

Fig. 2 SEM images(left) and EDAX characterization(right) of different CCTO ceramics

2.2 Valance State of Ti Ions at Grain Boundaries

Figure 3 shows the XPS spectra of Ti 2p level on the cleaved surfaces of the CCTO ceramics. One can see that the peaks for the Ti $2p_{3/2}$ and Ti $2p_{1/2}$ levels are located near 458 eV and 463 eV, respectively. Using the Gaussian-Lorentzian profile fitting, the Ti $2p_{3/2}$ peaks are divided into two sub-peaks near 457.8 eV and 458.6 eV. The peak at lower bonding energy is contributed from Ti^{3+}, while the other peak is attributed to Ti^{4+} [31]. The atomic ratios of Ti^{3+} to Ti^{4+} are calculated by comparing the areas of these sub-peaks. For samples 1035-48, 1080-3 and 1080-48, the atomic ratios of Ti^{3+} to Ti^{4+} are 1 : 1.10, 1 : 1.29, and 1 : 1.03, respectively. In comparison, these atomic ratios are similar to the reported ratios for CCTO[31]. Therefore, it can be concluded that prolonging sintering time is good for increasing the atomic percentage of Ti^{3+} at a grain boundary.

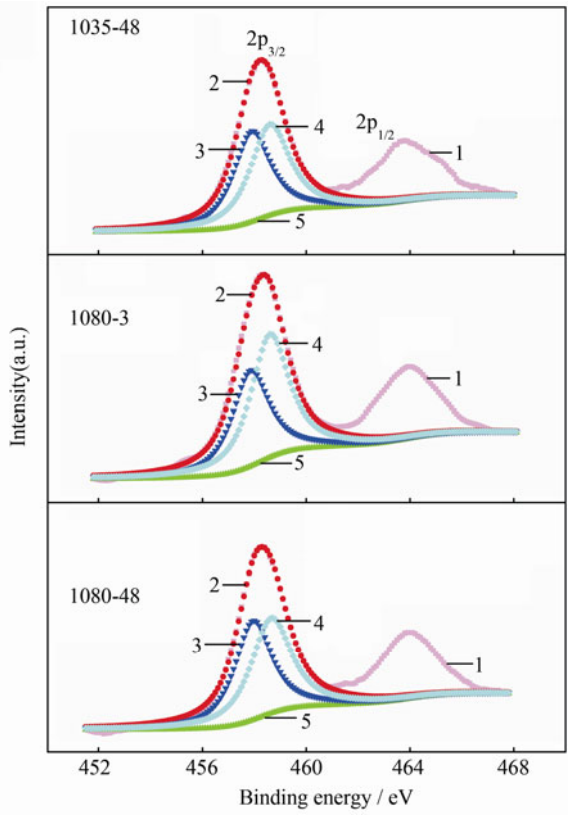

Fig. 3 XPS spectra of Ti 2p level for the surfaces of different CCTO ceramics

1: Experimental data; 2: Fitting curves; 3: Ti^{3+}; 4: Ti^{4+}; 5: Background

2.3 Electrical Properties

Figure 4 shows the direct current (DC) *J-E* curves measured at room temperature. The leakage current density of sample 1080-48 was clearly larger than that of sample 1080-3 or 1035-48. This result indicates that sintering at a high temperature for long time can significantly increase the leakage current density of the ceramic.

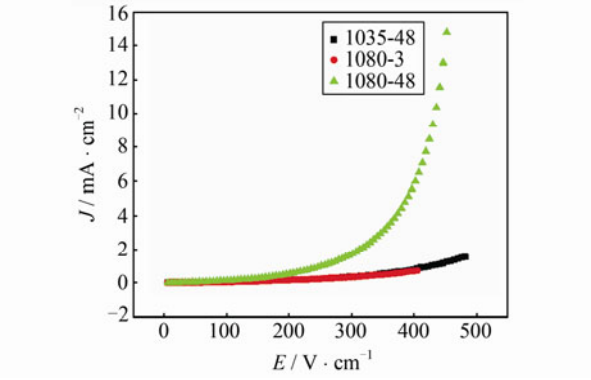

Fig. 4 DC *J-E* curves for the CCTO ceramics

J is the leakage current density; *E* represents the electric field strength

The measurement of DC *J-E* curves can only offer an average result for the DC conduction. It is known that there are electrical inhomogeneous regions in CCTO ceramics, such as semi-conductive grains and insulating grain boundaries. The complex plane of impendence (*Z**) is usually used to investigate the heterogeneous electrical structure in CCTO ceramics.

The room-temperature *Z** plots of samples 1035-48, 1080-3, and 1080-48 are shown in Fig. 5. The intercepts of these high-frequency straight lines in the inset figures, which represent the grain resistivity[32], are fitted to be 137.4 Ω•cm, 75.2 Ω•cm, and 60.5 Ω•cm for samples 1035-48, 1080-3, and 1080-48, respectively. At the low-frequency part, the arc-shaped curves are fitted according to IBLC model, and the value of grain-boundary resistivity is closely related to the diameter of the semi-circular curves. It is calculated that the grain-boundary resistivity for samples 1035-48, 1080-3, and 1080-48 are 2.3 MΩ • cm, 10.9 MΩ • cm, and 1.1 MΩ • cm, respectively. The result of *Z** is consistent well with that of the above *J-E* measurement. It can be seen that the grain resistivity of sample 1035-48 was larger than that of sample 1080-3, while the grain-boundary resistivity of sample 1035-48 was clearly smaller than that of sample 1080-3. As to sample 1080-48, both the grain resistivity and grain-boundary resistivity are much smaller than those of the other two samples, leading to the obvious enhancement of current leakage in a strong electric field.

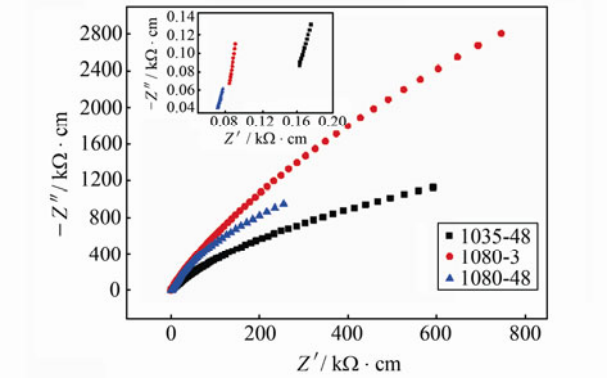

Fig. 5 Complex plane of impedance plots *Z measured at room temperature for the CCTO ceramics**

The inset figure is the plots near the high-frequency limit (1×10^7 Hz)

The electronic transport in CCTO ceramics is contributed from conductive Ti^{3+}, which, in general, are formed due to the issue that Ti^{4+} can accept electrons released from oxygen vacancies. Additionally, the cationic nonstoichiometry may introduce Ti^{3+} as well. For example, when the content of Cu ions is smaller than the stoichiometric value, some excess Ti ions may occupy Cu sites. As a result, some Ti^{3+} may form to compensate

the loss of low-valance Cu ions [9]. In the present work, the small grain resistivity of samples 1080-3 and 1080-48 may be attributed to the formation of large amount of oxygen vacancies at higher sintering temperature. In addition, as shown in EDAX, Cu-rich and Ti-poor grain boundaries are formed in both samples, leaving Cu-poor and Ti-rich grains. This nonstoichiometry of cation can also induce the increase of Ti^{3+} in grains. At grain boundaries, according to the estimated atomic ratios of Ti^{3+} : Ti^{4+} by XPS, the difference of grain-boundary resistivity between samples 1080-3 and 1080-48 was also related to the different content of Ti^{3+} in both samples.

Figure 6(a)-6(c) show the Z^* plots measured at different temperatures for samples 1035-48, 1080-3 and 1080-48, respectively. The increase of temperature led to the bending of the curves, which was attributed to the decrease of resistivity at higher temperatures. Through the fitting procedure mentioned above, the resistivity (ρ) values were all determined. As shown in the inset figures, as to both the grain resistivity (ρ_g) and the grain boundary resistivity (ρ_{gb}), the relationship between ln ρ and $1/T$ satisfied good linearship. This indicates that the electric conduction both in grains and near grain boundaries is attributed to the thermal activation mechanism:

$$\rho = \rho_0 \exp(E_a / k_B T) \quad (1)$$

where ρ_0 is the resistivity at infinite high temperature, k_B is Boltzmann constant, and E_a represents activation energy. According to Eq. (1), E_a is determined by the slope of the fitted linear equation of ln ρ *vs.* $1/T$. The fitted E_a values are also listed in the inset figures. It can be seen that the E_a values in grains were all close to 0.1 eV, and the change of sintering conditions did not make a clear impact on E_a. While at grain boundaries, the E_a of sample 1080-3 was about 0.1 eV smaller than those of the other two samples. This means that prolonging sintering process can enhance the activation energy at grain boundaries.

For CCTO ceramics, it is considered that a Schottky potential barrier exists at grain boundaries, and the E_a of grain boundaries reflects the height of this barrier. The formation of the grain-boundary Schottky potential barrier is attributed to the different electronic structures of grains and grain boundaries [32]. The Fermi energy at grain boundaries is lower than that in grains. Moreover, some impure ions, such as those absorbed oxygen molecules, can introduce vacant discrete levels in the energy gap of grain boundaries. Therefore, the conducting electrons near grain boundaries can be trapped by these levels till. Fermi energies in grains and at grain boundaries become identical. In this process, grain boundaries catches negative charges while some regions near grain boundaries lose electrons and carry positive charges. The separation and accumulation of charges produces a depletion layer near the interface between a grain and grain boundary. The inner electric field in the depletion layer forms the potential barrier. In the present work, sintering for long time is good for producing a large content of carriers near grain boundaries. In that case, more charges are captured at grain boundaries, causing the enhanced grain-boundary potential barrier.

Figure 7(a) shows the room-temperature spectra of dielectric constants. Among these three samples 1080-3, 1080-48 and 1035-48, sample 1035-48 exhibits the smallest dielectric constant in the full range of frequency of measurement. In addition, between 1×10^6 Hz and 1×10^7 Hz, the dielectric constants of all samples drop rapidly, which is a typical Debye-type dielectric relaxation. Figure 7(b) depicts the room-temperature spectra of dielectric loss. The dielectric loss of these samples all reach the peak value near the frequency of 1×10^7 Hz,

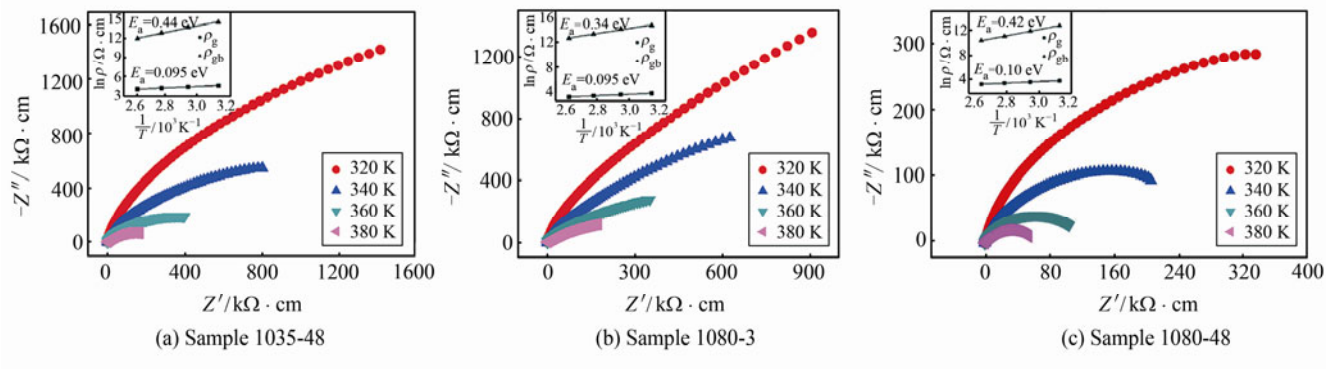

Fig. 6 Complex plane of impedance plots Z^* of different CCTO ceramics measured at 320, 340, 360 K and 380 K

The inset figures show the fitting results of activation energy in grains and at grain boundaries

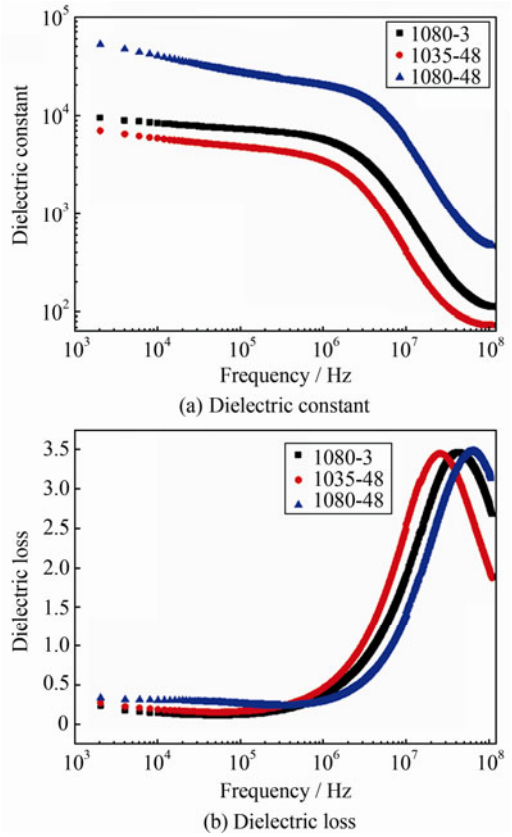

Fig. 7 Frequency dependence of electrical properties for the CCTO ceramics at room temperature

meanwhile, the frequency of the peak for sample 1080-48 is the highest, while that of sample 1035-48 is the lowest. When the frequency is lower than 1×10^5 Hz, the dielectric loss of sample 1080-48 is the largest comparing with that of samples 1035-48 and 1080-3. Meanwhile, a weak peak is also observed near 1×10^4 Hz from these three curves.

According to IBLC model, the giant dielectric constant of CCTO ceramics can be explained as below: In an alternating current (AC) electric field, electrons in grains will migrant to grain boundaries and be inhibited by a large grain-boundary potential barrier. As a result, a giant boundary polarization is formed, resulting in the giant dielectric response. Therefore, a large content of grain carriers and a large boundary potential barrier are two conditions for observing the giant dielectric constant in CCTO ceramics. In the present work, even though a strong boundary potential barrier is established in sample 1035-48, because the content of carriers in grains is very little, the dielectric constant is small. While, for the ceramics sintered at 1 080 ℃, the grain resistivity reduces, and the low-frequency dielectric constants significantly increase. Particularly, the grain resistivity of sample 1080-48 is much smaller than those of samples 1035-48 and 1080-3, and a strong boundary barrier is also established. The combination of both factors results in the large increase of dielectric constants.

3 Conclusion

In summary, the CCTO ceramics were prepared by sol-gel method and sintered at different temperatures for different duration. The results show that a Cu-rich and Ti-poor grain boundary is formed in the CCTO ceramic and the grain resistivity of the CCTO ceramic is reduced at a high sintering temperature (1 080 ℃). When the sintering time increases to 48 h, a large content of Ti^{3+} form at grain boundaries of CCTO ceramic, resulting in a small grain-boundary resistivity and a large grain-boundary activation energy. As to the ceramic sintering at 1 080 ℃ for 48 h, the dielectric constant was greatly increased due to the small grain resistivity and large grain-boundary activation energy. This result is firmly consistent to IBLC model which can explain the origin for the giant dielectric constants in CCTO ceramics.

References

[1] Ramirez A P, Subramanian M A, Gardel M, *et al.* Giant dielectric constant response in a copper-titanate [J]. *Solid State Communications*, 2000, **115**(5): 217-220.

[2] Kolev N, Bontchev R P, Jacobson A J, *et al.* Raman spectroscopy of $CaCu_3Ti_4O_{12}$ [J]. *Physical Review B*, 2002, **66**: 132102-132102-4.

[3] Subramanian M A, Li D, Duan N, *et al.* High dielectric constant in $ACu_3Ti_4O_{12}$ and $ACu_3Ti_3FeO_{12}$ phases [J]. *Journal of Solid State Chemistry*, 2000, **151**: 323-325.

[4] Zhu Y, Zheng J C, Wu L, *et al.* Nanoscale disorder in $CaCu_3Ti_4O_{12}$: A new route to the enhanced dielectric response [J]. *Physical Review Letters*, 2007, **99**: 037602-037602-4.

[5] Delugas P, Alippi P, Fiorentini V, *et al.* Reorientable dipolar Cu_{Ca} antisite and anomalous screening in $CaCu_3Ti_4O_{12}$ [J]. *Physical Review B*, 2010, **81**: 081104-081104-4.

[6] Li M, Shen Z J, Nygren M. Origin(s) of the apparent high permittivity in $CaCu_3Ti_4O_{12}$ ceramics: Clarification on the contributions from internal barrier layer capacitor and sample-electrode contact effects [J]. *Journal of Applied Physics*, 2009, **106**(10): 104106-104106-8.

[7] Kwon S, Huang C C, Subramanian M A, *et al.* Effects of cation stoichiometry on the dielectric properties of $CaCu_3Ti_4O_{12}$ [J]. *Journal of Alloys and Compounds*, 2009, **473**(1-2): 433-436.

[8] Adams T B, Sinclair D C, West A R. Characterization of grain boundary impedances in fine- and coarse-grained $CaCu_3Ti_4O_{12}$ ceramics[J]. *Physical Review B*, 2006, **73**: 094124-094124-9.

[9] Li M, Feteira A, Sinclair D C, *et al.* Influence of Mn doping on the semiconducting properties of $CaCu_3Ti_4O_{12}$ ceramics [J]. *Applied Physics Letters*, 2006, **88**(23): 232903-232903-3.

[10] Li M, Feteira A, Sinclair D C, *et al.* Incipient ferroelectricity and microwave dielectric resonance properties of $CaCu_{2.85}Mn_{0.15}Ti_4O_{12}$ ceramics [J]. *Applied Physics Letters*, 2007, **91**(13): 132911-132911-3.

[11] Yang Z, Zhang Y, You G , *et al.* Dielectric and electrical transport properties of the Fe^{3+}-doped $CaCu_3Ti_4O_{12}$ [J]. *Journal of Materials Science & Technology*, 2012, **28** (12): 1145-1150.

[12] Wang C C, Zhang L W. Oxygen-vacancy-related dielectric anomaly in $CaCu_3Ti_4O_{12}$: Post-sintering annealing studies [J]. *Physical Review B*, 2006, **74**: 024106-024106-4.

[13] Lin Y H, Cai J, Li M, *et al.* Grain boundary behavior in varistor-capacitor TiO_2-rich $CaCu_3Ti_4O_{12}$ ceramics [J]. *Journal of Applied Physics*, 2008, **103** (7): 074111-074111-5.

[14] Patterson E A, Kwon S, Huang C C, *et al.* Effects of ZrO_2 additions on the dielectric properties of $CaCu_3Ti_4O_{12}$ [J]. *Applied Physics Letters*, 2005, **87** (18): 182911-182911-3.

[15] Fang T T, Mei L T, Ho H F. Effects of Cu stoichiometry on the microstructures, barrier-layer structures, electrical conduction, dielectric responses, and stability of $CaCu_3Ti_4O_{12}$ [J]. *Acta Materialia*, 2006, **54** (10): 2867-2875.

[16] Luo F C, He J L, Hu J, *et al.* Electric and dielectric properties of Bi-doped $CaCu_3Ti_4O_{12}$ ceramics [J]. *Journal of Applied Physics*, 2009, **105**(7): 076104-076104-3.

[17] Yang Z, Zhang Y, Lu Z H, *et al.* Electrical conduction and dielectric properties of the Rb-doped $CaCu_3Ti_4O_{12}$ [J]. *Journal of the American Ceramic Society*, 2013, **96** (3): 806-811.

[18] Yang Z, Zhang Y, Zhang K, *et al.* Effect of grain-boundary behavior on the dc electric conduction in Rb-doped $CaCu_3Ti_4O_{12}$ [J]. *Journal of Materials Science*: *Materials in Electronics*, 2013, **24** (3): 1063-1067.

[19] Zhao Y H, Gao R J, Su G , *et al.* Effect of dispersant on $CaCu_3Ti_4O_{12}$ powders synthesized by oxalate co-precipitation method [J]. *Materials Letters*, 2013, **91**: 187-190.

[20] Sangwong N, Yamwong T, Thongbai P. Synthesis, characterization and giant dielectric properties of $CaCu_3Ti_4O_{12}$ ceramics prepared by a polyvinyl pyrrolidone-dimethylfor mamide solution route [J]. *Journal of Electroceramics*, 2013, **31**(1-2): 181-188.

[21] Ahmad M M. Giant dielectric constant in $CaCu_3Ti_4O_{12}$ nanoceramics [J]. *Applied Physics Letters*, 2013, **102**(23): 232908-232908-4.

[22] Swatsitang E, Niyompan A, Putjuso T. Giant dielectric, low dielectric loss, and non-ohmic properties of nanocrystalline $CaCu_3Ti_4O_{12}$ [J]. *Journal of Materials Science*: *Materials in Electronics*, 2013, **24** (9): 3514-3520.

[23] Kumar R, Zulfequar M, Sharma L, *et al.* Growth of nanocrystalline $CaCu_3Ti_4O_{12}$ ceramic by the microwave flash combustion method: structural and impedance spectroscopic studies [J]. *Crystal Growth & Design*, 2015, **15** (3): 1374-1379.

[24] Ahmad M M, Yamada K. Grain size effect on the giant dielectric constant of $CaCu_3Ti_4O_{12}$ nanoceramics prepared by mechanosynthesis and spark plasma sintering [J]. *Journal of Applied Physics*, 2014, **115** (15): 154103-154103-6.

[25] Jesurani S, Kanagesan S, Velmurugan R, *et al.* A comparative study of conventional sintering with microwave sintering of high dielectric calcium copper titanate nano powder synthesized by sol-gel route [J]. *Transactions of the Indian Ceramic Society*, 2011, **70** (2): 79-85.

[26] Yang Z, Zhang Y, Xiong R, *et al.* Effect of sintering in oxygen on electrical conduction and dielectric properties in $CaCu_3Ti_4O_{12}$ [J]. *Materials Research Bulletin*, 2013, **48** (2): 310-314.

[27] Wang B, Pu Y P, Wu H D, *et al.* Influence of sintering atmosphere on dielectric properties and microstructure of $CaCu_3Ti_4O_{12}$ ceramics [J]. *Ceramics International*, 2013, **39**: S525-S528.

[28] Prakash B S, Varma K B R. The influence of the segregation of Cu-rich phase on the microstructural and impedance characteristics of $CaCu_3Ti_4O_{12}$ ceramics [J]. *Journal of Materials Science*, 2007, **42** (17): 7467-7477.

[29] Schmidt R, Stennett M C, Hyatt N C, *et al.* Effects of sintering temperature on the internal barrier layer capacitor (IBLC) structure in $CaCu_3Ti_4O_{12}$ (CCTO) ceramics [J]. *Journal of the European Ceramic Society*, 2012, **32**(12): 3313-3323.

[30] Zhang L, Tang Z J. Polaron relaxation and variable-range-hopping conductivity in the giant-dielectric-constant material $CaCu_3Ti_4O_{12}$ [J]. *Physical Review B*, 2004, **70** (17): 174306-174306-6.

[31] Adams T B, Sinclair D C, West A R. Giant barrier layer capacitance effects in $CaCu_3Ti_4O_{12}$ ceramics [J]. *Advanced Materials*, 2002, **14**: 1321-1323.

[32] Clarke D R. Varistor ceramics [J]. *Journal of the American Ceramic Society*, 1999, **82** (3): 485-502.

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